Understanding and comparing datasheets for high-speed ADCs

By Eduardo Bartolome (Email: e-bartolome1@ti.com)
High-Speed ADC Systems and Applications Manager

Introduction

As with any other aspect of a product, datasheets can always be improved, and manufacturers work hard to clarify them.[1] Nevertheless, there is already a legacy of many products/datasheets in the market, and even for those recently released or under release, different criteria may have been selected depending on different factors. Even given the existence of a few published standards such as Reference 2, convergence is still far away.

The purpose of this article is to highlight the differences between the criteria for writing datasheets applied by different manufacturers or even by the same manufacturer of different high-speed analog-to-digital converters (ADCs). Table 1 is a quick checklist that can be used to select the right device.

dB versus dBc versus dBFS

One of the main criteria for evaluating high-speed-ADC performance shown on a datasheet is the dynamic or ac set of specifications like SNR, SINAD, THD, and SFDR. As an example, let's consider the SINAD (also called SNDR or SNRD), which is the ratio of signal power to the power of all other spectral components (distortion and noise) combined. Usually, such a ratio is transformed into logarithmic scale and expressed in dB. In this particular case,

$$\text{SINAD} = 10 \times \log\left(\frac{P_S}{P_{N+D}}\right).$$

One of the biggest discrepancies between datasheets arises in the selection of units, specifically in the criteria used to select the power of the signal. Without going into the details that lead to this disparity, let's note that the power of the signal could be simply the power of the signal being used on the measurement,[3] or it could be the extrapolated power of the signal as if it was full-scale. To avoid confusion, Texas Instruments (TI) indicates the units in the first case as dBc (dB to the carrier), and in the second case as dB in older datasheets or as dBFS (dB to full scale) in the most recent datasheets. Although there is no major issue between the two and one can be obtained from the other as will be explained later, the confusion arises when the manufacturer specifies only "dB." In the datasheets of two TI competitors, "dB" is equivalent to dBc, while in the datasheet of a third competitor, "dB" is equivalent to dBFS.

What impact does this have on the final comparison? Let's imagine that two converters from different manufacturers have been measured with an input amplitude of –1 dBFS. This means that during the test, the input was a sinusoidal tone 1 dB below full scale or, in other words, had an amplitude (A) about 90% of the ADC's full dynamic range. Let's also assume that both converters have the same performance and, as such, the noise plus distortion power is the same. In the first case ("dB" is equivalent to dBc), the manufacturer computed the SINAD_1 as the power of the input (A) divided by the power of noise plus distortion (N+D). In the second case ("dB" is equivalent to dBFS),

Table 1. Quick checklist for selecting high-speed ADCs

SPECIFICATION	CONSIDERATION
Power consumption	Make sure that output supply is included and is specified under the same conditions in which you are going to use the device.
Input clock amplifier	If you are going to sample high-input frequencies, look for differential clock inputs and an input clock amplifier.
SNR, SINAD, SFDR, THD	Be careful with dB units. They may mean dBc or dBFS.
Output timing	Make sure output timing is properly specified and has enough window to capture the data. Some devices offer an output clock with a better timing window for easier interface.
Input bandwidth	Device performance is not necessarily guaranteed up to the frequencies specified.
General specifications	• Since the manufacturer will ensure only minimum values, look for those rather than typical values. • Check for specifications under the same conditions in which you are going to use the device. • Look for plots showing device robustness, like performance variation over different temperatures or supply voltages. • Verify the performance versus the input amplitude graph if required.

the manufacturer extrapolated the power of the signal to the full scale, which in this case resulted in an increase of the final number by 1 dB (as the input was –1 dBFS). So, $SINAD_2 = SINAD_1 + 1$. The first manufacturer's device looks 1 dB worse but is actually as good as the one from the second manufacturer. The dBc value can be extracted from the dBFS value by adding the input amplitude (in dBFS):

Specification (in dBc) = Specification (in dBFS) + A_{IN} (in dBFS).

Another point to take into account when we compare two devices whose specifications are expressed in dBc is the input amplitude, which also changes from device to device. Obviously, as the input amplitude decreases, the signal level (in dBc) will most likely become smaller (as the signal power becomes smaller while some components of the noise floor stay the same). So, for the comparison to be meaningful, both input amplitudes should be the same. A good extrapolation can be done by just adding the difference between both input amplitudes to the specification obtained with the smaller input amplitude.

Observe that as most of the converters are specified with signals close to the full scale, the difference in the final signal level, depending on the units being used, will usually not be bigger than 2 dB, although that can actually represent a considerable difference in some applications, affect the yields of the final design in production, or even force a whole redesign.

The final question is how to distinguish whether the dB in the ADC datasheet is dBc or dBFS. One of the easiest ways is to ask the vendor directly; but, if that is not possible, the designer can look at the typical-performance graphs section of the datasheet. There vendors will usually have different graphs in dBc and dBFS whose numbers can be compared to the ones specified in the datasheet tables.

Power specifications

Power is another point where datasheets usually show discrepancies. TI has traditionally listed on the first page of its datasheets the total power of the converter under typical operating conditions. These conditions are at full sample rate with an input different than the low frequency or dc, and, on the digital side, with a 10-pF load on each pin. However, TI has started separating core (analog, AV_{DD}) power and digital (output, DV_{DD}) supply consumptions. This is mainly because almost every other vendor specifies only the analog consumption and does not include the interface power. Some vendors list the interface power inside the datasheet; but users should pay attention to the conditions of such a measurement, as input frequency, output load per pin, and output voltage affect that value significantly.

Also, special attention should be paid to special modes that the ADC may have. Although such is not the case with TI datasheets, some vendors' converters have a mode A under which the power is measured and listed in the datasheet, while all the other dynamic specifications are actually given under a mode B. Or, for instance, for converters that accept wide digital supply voltages, the datasheet gives the specification of the timing under the highest DV_{DD} but provides the power consumption numbers under the lowest DV_{DD}.

Finally, pay attention to what the converter offers for that power. Some converters may save power at the expense of missing internal blocks such as the reference or clock amplifier that could be needed for things like accepting differential clocking (for lower noise/jitter), small swing clock levels like PECL or LVDS, or squaring a filtered clock (sinusoidal). More on this topic follows.

Clocking

Clocking is a fundamental care-about to obtain the best ADC performance[4]; and, although all ADCs have a clock input, some are easier to use than others. Specific concerns are clock jitter, duty cycle, and required clock levels, mainly to obtain good performance numbers when high input frequencies are sampled.

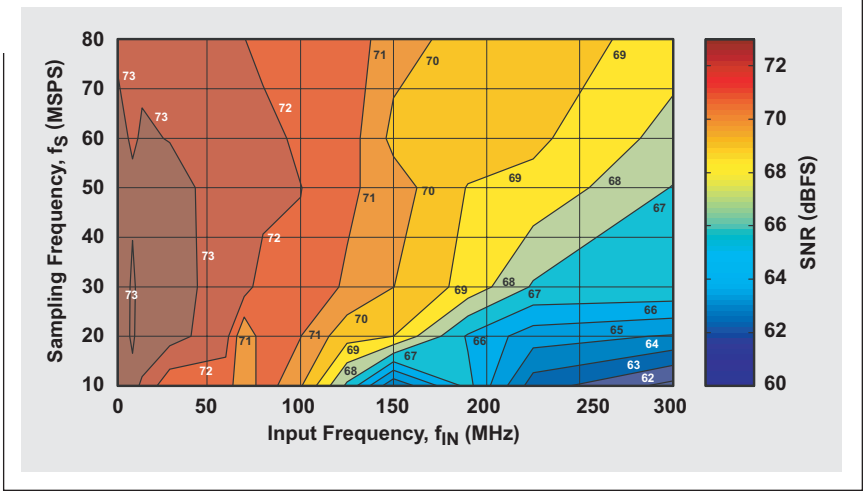
To obtain low jitter, users usually bandpass filter the clock. This will produce a 50% duty cycle, which is usually close to the best condition for many ADCs. Nevertheless, the clock amplitude will be affected due to the insertion loss of the filter; and the shape will become sinusoidal, not square. To be able to accept this high-quality clock, TI and some other manufacturers include a clock amplifier at the input of the ADC. Its functions, among others, is to square the sinusoidal clock and provide the necessary gain to clock the internal circuits. The clock amplifier will, moreover, present a differential interface that will make it less susceptible to noise coupling in the clock lines, reducing jitter. Of course, this will come at the expense of some increased ADC power consumption.

Nevertheless, some ADCs may not be so friendly and will require a square CMOS-level clock. The input on these types of ADCs will be single-ended, with zero rejection of external noise sources coupling to the clock path. Most of these ADCs are targeted to the sampling of low (below 50 MHz or so) input frequencies and yield a good performance there. Medical ultrasound would be a typical application for these ADCs. Nevertheless, users targeting high (greater than high 60s) SNR at higher input frequencies (like on communication applications) should know that they will need to provide external components to square the clock, effectively increasing the power and the board area. Even with those extra components, there is nothing that the user can do with respect to the single-ended interface, and the final design most likely will not obtain the optimized performance that ADCs with an internal clock amplifier provide.

In the effort to provide consistent datasheets, TI actually uses all the plots and performance numbers on the same datasheet that share the same clock conditions. For devices with a differential input clock, usually a sinusoidal is used, which is usually not the best condition for the ADC (due to the limited slew rate of the clock edges). To cover all possible applications of the converter, TI started

introducing 3D contour plots (Figure 1) in its datasheets, which allow the customer to find the typical performance under a given set of input and sampling frequencies. As just noted, all the conditions of the input clock are kept constant during the experiment except, obviously, when its sampling frequency is changed. This means that if a sinusoidal clock is used, reducing the sampling frequency will make the edges of the clock become slower, increasing the effective jitter. This is a common phenomenon in every ADC,[4] but TI's ADCs are designed to minimize it as much as possible. Although this is a worst-case situation and there are techniques to minimize jitter, it would not be fair to change the clock conditions during the experiment; and, as such, they are kept constant and show the SNR degradation due to the increased jitter. Users should be aware that without the clock amplifier, the performance degradation would actually be much worse. They should also be aware that if a very low-jitter square clock could be provided, the performance of the ADC would actually be much better.

Figure 1. SNR vs. input and sampling frequencies[5]



Output timing

To be able to capture the output data with the FPGA, ASIC, DDC, or any other logic device following the ADC, users need to know the window where the output data is stable. Nevertheless, this is a point where most of the manufacturers struggle to provide a consistent and complete set of datasheet limits. This is because the final test solution being used in production is affected by several factors such as precision of the automated test equipment, no direct access to the outputs (data being buffered), difficulty setting the same conditions (like digital load) as the datasheet, etc. To bypass these limitations, TI set these numbers by design and characterization—i.e., statistically—which usually forces us to set wider guardbands, as the devices are not going to be tested in production. The same type of limitations apply to other manufacturers, many times resulting in incomplete or poorly specified datasheets.

Designers should specifically question devices that do not have any guarantees at all; do have guarantees but under unrealistic conditions (like 0-pF load); do not specify all the parameters necessary for the capture (for instance, set-up time is given but not hold time); do not explain what V_{OH} and V_{OL} levels are used with the specifications (for example, giving information from 50% to 50%, which is very cumbersome to extrapolate to V_{IH}/V_{IL} logic levels); or do not specify a parameter over the full operating temperature range.

Also, to improve the window for data capture, TI and other manufacturers provide an output clock that has better tracking with the output data than the input clock. Using the output clock will alleviate the timing constraints on the application.

Finally, notice that set-up and hold times are defined as the counterparts of the set-up and hold times defined for latches. In a latch, set-up time indicates how early the data has to be ready at the input of the latch before the clock edge is provided to latch it. The longer this time is, the harder it is to use that latch. On the ADC, the set-up time indicates how early the data is stable before the input or output ADC clock edge. The longer the set-up time is, the easier it is to capture the data. The same applies to the hold times.

Process gain

When comparing two SNR numbers, users should take into account the sampling rate of the ADC. The SNR is computed by integrating the total noise floor all the way to Nyquist. Nevertheless, the user's signal will occupy only a certain bandwidth; and only the noise on that bandwidth will affect the signal, as the rest can be removed with a digital filter. For the same SNR, the ADC with a higher sample rate will have a lower noise floor. For example, a 200-kHz-bandwidth sigma-delta with 90-dBFS SNR would look better on paper than the ADS5424, a 14-bit ADC running at 100 MSPS with a 75-dBFS SNR on its datasheet. If, however, after using the ADS5424 to sample the 200-kHz bandwidth (clearly oversampling at 100 MSPS), we use a digital filter to remove the out-of-band noise (from 200 kHz all the way up to 50 MHz), the equivalent SNR of the ADS5424 on that bandwidth will be

$$\begin{aligned} SNR_{200\ kHz} &= 75 + 10 \times \log10(50 \times 10^6/200 \times 10^3) \\ &= 99\ dBFS >> 90\ dBFS. \end{aligned}$$

The SNR of the ADS5424 would clearly be much better than that of the sigma-delta (assuming, for the sake of this example, that the noise is evenly distributed over Nyquist; i.e., there is no significant flicker contribution). The second term of the preceding equation is called process gain. As the oversampling ratio increases, for every time the user doubles the sampling rate for the same SNR, the noise

floor will decrease by 3 dB. In other words, the equivalent resolution on the bandwidth of interest will be increased by 0.5 bit.

Conditions and guaranteed minimums

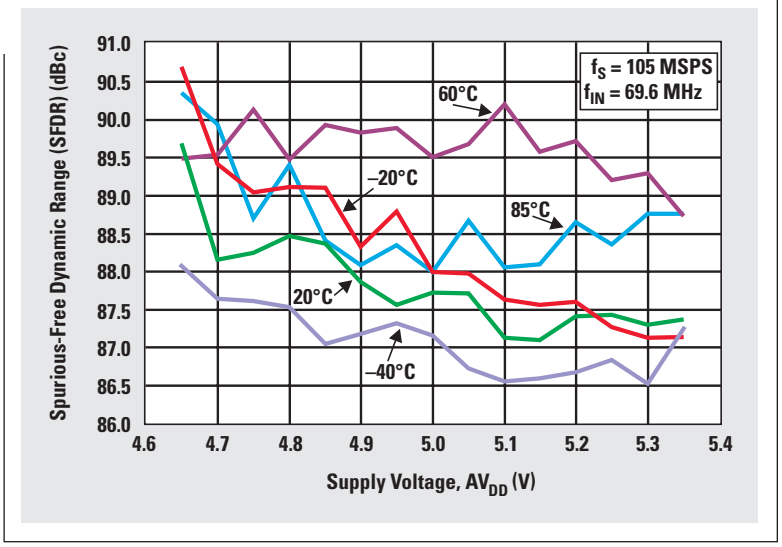
A value/specification is meaningless if the conditions are not expressed. This is especially important when we look at advertisements, marketing materials, and selection tables, which tend to simplify the more complete information presented in a datasheet and, in some cases, do not mention the conditions of the measurement.

At the same time, typical values usually represent the average of a distribution. Nevertheless, users should look at the minimum values, especially if the device is going to operate over a certain range of conditions like varying temperature. Having a wide spread between the typical and minimum numbers should raise questions. Is the spread due to a limitation of the final test solution? If so, maybe the device will fit the application but with a certain risk that only the minimum values are guaranteed. The worst case would be if the limitation was due to the device itself. A process variation (from device to device) could point to a weak design. A good way to look for the robustness of the device and screen for these types of problems is to look at the datasheet graphs of typical performance variations versus supply voltage or temperature, similar to the example in Figure 2.

Just as with the power numbers, when looking at different parameters (for instance, SNR and SFDR) in the same datasheet, make sure they are all given under the same conditions. For instance, some devices have an SFDR mode where the SFDR improves at the expense of the SNR; or they have different input ranges, which can affect both the SFDR (better at the smaller input range) and the SNR (better at the bigger input range).

Finally, be aware that most of the specifications are given close to full-scale range. Nevertheless, the SFDR (in dBFS) may get better or worse as the input amplitude is decreased. Manufacturers cannot screen many conditions on the final test, as that would increase the test time and thereby the cost; but they usually include typical graphs that show the effects of various conditions.

Figure 2. ADS5424 SFDR vs. analog supply and temperature range[6]



Input bandwidth

Usually the input bandwidth is representative of the flatness of the ADC response versus input frequency. It is not an indication that the device will hold the performance up to those input frequencies. Users should look for graphs that verify performance; and, if none exist, they should request support from the vendor or evaluate the device themselves.

Conclusion

A detailed summary of the main differences between criteria that manufacturers use to write datasheets for high-speed ADCs has been presented. Early consideration of these differences will help designers avoid surprises further down the road.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

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1. Joshua Israelsohn, "High-speed ADCs: preventing front-end collisions," *EDN Magazine*, May 13, 2004.	—
2. IEEE Standard 1241, "IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters."	—
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4. Eduardo Bartolome et al., "Clocking high-speed data converters"	slyt075
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6. "14-Bit, 105-MSPS Analog-to-Digital Converter," ADS5424 Datasheet, p. 14	slws157

Related Web sites

dataconverter.ti.com
www.ti.com/sc/device/ADS5424
www.ti.com/sc/device/ADS5500

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