PCB layout for the TPA005D1x and TPA032D0x Class-D APAs

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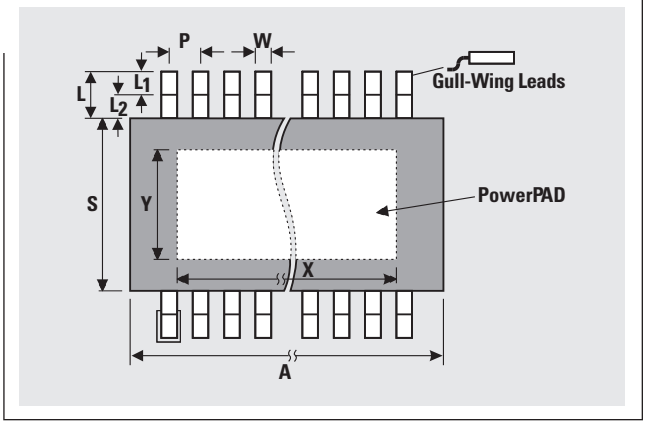
Following good, sensible printed circuit board (PCB) layout practices will ensure peak performance and reliability from Class-D audio power amplifiers. A good thermal and mechanical bond between the device pins and PowerPAD™ and the PCB landings (pads) will provide the necessary electrical and thermal pathways for the amplifier to operate efficiently and dissipate the heat generated during peak operation. This can be achieved with an understanding of the basic manufacturing process and a proper layout of the IC and PowerPAD footprint. Once the device is in place, the power and ground connections must be made. A solid ground plane is recommended when possible as it provides a low-impedance ground return path, connects to the device PowerPAD to serve as a heat sink, and reduces crosstalk between channels. Routing and decoupling of the power traces provides the proper paths for return currents and minimizes the fluctuations of the voltage at the power pins. The routing of the signal path wraps up the device layout, with only a few sensitive nodes in the Class-D and headphone amplifier circuits to consider. Some miscellaneous considerations, when employed, will improve the quality of the end product and facilitate the production of the circuit, improving reliability and providing a much less stressful environment for the engineer and PCB manufacturer.

Figure 1. 48-pin HTSSOP package



PCB footprint for the device

The TI TPA005D1x and TPA032D0x Class-D devices come in the 48-pin HTSSOP (TSSOP with a PowerPAD) package. A small portion of the package is shown in Figure 1, with the maximum and minimum lengths for the dimensions provided in Table 1 in both millimeters (mm) and thousandths of an inch (mils). The PowerPAD is a leadframe die pad located on the bottom of the package that serves as a thermal path between the silicon die of the amplifier and the ground plane of the PCB.[1] It is approximately 5.4 mm (210 mils) long and 2.3 mm (90 mils) wide and is centered on the bottom of the package. The device pins are bent downward in what is called a "gull wing" shape and have a constant pitch of 0.5 mm (19.7 mils).

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Table 1. Dimensions of the device and PCB footprint for the 48-pin HTSSOP package

ITEM	MEASUREMENT	SYMBOL**	DIMENSIONS*			
			MAXIMUM		MINIMUM	
			(mm)	(mils)	(mm)	(mils)
HTSSOP package (Figure 1)	Pitch, IC pins	P	0.5	19.7	0.5	19.7
	Width, IC pins	W	0.27	10.6	0.17	6.7
	Length, IC pin	L	1.05	42	0.95	37.4
	Length, IC pin, package to foot	L_2	0.55	21.7	0.2	7.8
	Length, IC pin, foot	L_1	0.75	29.5	0.5	19.7
	Width, package	S	6.2	244	6.0	23.6
	Length, package	A	12.6	496	12.4	488
	Width, PowerPAD	Y	2.3	90	N/A	N/A
	Length, PowerPAD	X	5.45	215	N/A	N/A
PCB footprint (Figure 2)	Pitch, pin lands	P_1	0.5	19.7	0.5	19.7
	Width, pin lands	W_1	0.32	12.7	0.25	9.8
	Length, pin lands	L_3	0.75	29.5	0.56	22
	Spacing, pin lands	S_1	6.75	266	6.2	244
	Width, PowerPAD land	Y_1	3.2	126	2.3	90
	Length, PowerPAD land	X_1	6.35	250	5.85	230

*Dimensions are in millimeters (mm) and thousandths of an inch (mils). 1 mil = 0.001 inch.
**See Figures 1 and 2.

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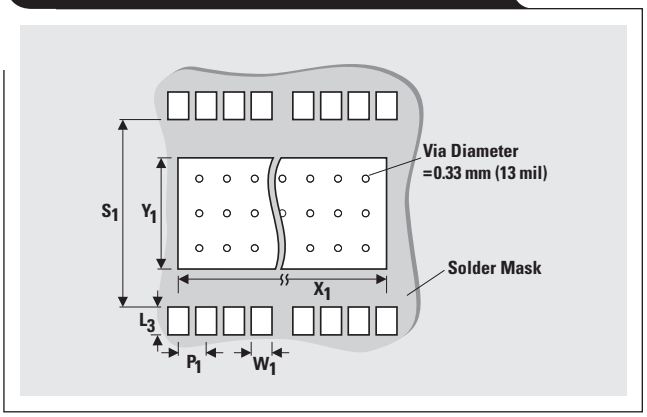
Figure 2 shows the pattern of IC pin and PowerPAD landings, called the IC footprint. These are the PCB pads that have been effectively used on the Class-D evaluation module (EVM). The PCB pad that serves as the landing for the PowerPAD should be at least the same size as the PowerPAD, but can be larger. If it is larger, the excess copper should be covered with solder mask to prevent wicking of the solder away from the PowerPAD area during assembly. The number of vias to be placed within the landing directly under the PowerPAD is determined by looking up the particular package in the *Package Outlines Reference Guide*.[2] In this case it is 21 vias spaced evenly in 3 rows of 7 vias each. These vias should be 13 mils in diameter to allow solder to be wicked into them during assembly. This serves two purposes: It vents out any air or gases that may otherwise be trapped under the package and form bubbles that reduce the contact between the PowerPAD and ground plane, potentially limiting the heat transfer; and it completely fills the vias, increasing some of the heat transfer to the ground plane. Since these vias are connected directly to a large ground plane, thermal relief such as webs or spokes should not be used. The idea is to draw the heat out, not keep it in. Additional, larger vias may be placed outside of the PowerPAD area and are not restricted to 13 mils.

Experimentation has revealed that during the assembly process, a solder paste stencil that is 6 mils thick and covers approximately 60% of the PowerPAD landing area (for a landing that is 125 mils by 250 mils) and 90% of each of the landings of the surface mount components creates an effective contact between the PowerPAD, IC pins, components and the PCB landings during the solder reflow process. Figure 1 does not show that the seating plane (distance between the foot of the IC pins and the bottom of the package) will be approximately 3 mils and that the package is approximately 43 mils in total height. The assembly, if automated, should be programmed such that it will not press down on the package too far, displacing the solder paste for the PowerPAD and possibly bending the leads.

The PCB landings for the amplifier pins should meet the minimum guidelines as set forth by the Institute for Interconnecting and Packaging Electronic Circuits (IPC) in the standard IPC-A-610[3] and as derived from the standard IPC-SM-782.[4] According to IPC-A-610, the IC pin may overhang the PCB land, both to the sides and toward the outside edge of the pads, as long as there is proper solder wetting evident on the heel and the side contacting the pad. This is acceptable because the solder is present mainly to form a mechanical bond between the PCB and the device rather than as a conductive path for current flow. Such requirements set the minimum, and the current manufacturing techniques set the maximum, size of the footprint for the device as shown in Table 1.

During the reflow soldering process, the PowerPAD landing on the PCB acts as a heat source due to the large amount of copper attached to it. This heat source will draw, or wick, toward the center of the device footprint any solder that is on the traces or landings of nearby IC pins or components. This reduces the solder available to form the joint between the IC pins and the corresponding PCB landings and can be a real problem when a high-current

Figure 2. 48-pin HTSSOP land pattern



pin is involved. A smaller joint means greater resistance and therefore more power dissipated in the joint, and this can quickly cause the connection to fail as it is heated and reheated during repeated use.

Several steps can be taken to ensure that a good solder joint is made.

First, ensure that each landing is isolated from adjacent landings through the use of a pocket-type solder mask window rather than a gang window. A pocket window is where the mask completely surrounds each pad, effectively creating a pocket (see Figure 2). This should be done even if two pads are electrically connected to ensure that the solder properly wicks onto each pin of the device. Photo-imaged solder masks now allow solder mask back-off (swell)—the distance the mask must be from the edge of the copper to avoid bleeding onto the landing—of as little as 1 mil and mask thickness between lands of 3 mils. This type of mask leaves no residue on the surface of the lands and traces.

Second, cover the traces that connect to a pad with solder mask, especially if they extend under the chip toward the PowerPAD. This is especially true if these traces terminate at the other end in a via or pad for another component. The solder paste stencil will cover all the areas that are exposed with solder, and the mask will reduce the chance of a solder bridge forming or solder migrating down the trace away from the desired location. A swell of 1 mil can be used here also.

Third, provide directions in a text file to the PCB manufacturer that indicate the desired swell, paste stencil thickness, and area of coverage for each location (such as 90% for components, 60% on the PowerPAD). This will prevent errors introduced by the manufacturer applying "good manufacturing practices" and resetting the swell to a 15-mil back-off, which could prove troublesome.

Power and ground connections

The TPA005D1x and TPA032D0x devices all have the same general power and ground structure. The amplifier is divided into three major sections: analog circuits, power output circuit, and charge-pump/headphone circuit. Figure 3 shows a general schematic for the Class-D audio power amplifiers that may vary slightly from device to device. The upper portion of the IC contains the sensitive analog circuits for the device. The powerful H-bridge output

section is located in the middle, and the lower section consists of the charge-pump circuit for Class-D mode of operation and the headphone circuit for Class-AB mode of operation. The figure clearly shows how the ground plane should be subdivided to minimize ground loops.

The analog circuit ground is pin 47, and all the analog section capacitors and grounds should terminate as close to this pin as possible. The charge-pump and headphone circuits are not operational at the same time and thus are considered one section. Their ground pins (27 and 20, respectively) can each be considered ground for this section. The power circuit grounds are pins 12 and 13 for the left channel and pins 36 and 37 for the right channel. It is particularly important to terminate the decoupling capacitors of the power section close to these grounds and have the ground plane close to and along the entire length of the power input traces for return currents to flow back easily to the power source. This is also true for the analog input section since it has an outside source supplying the signal. The same holds true for the power pins of each of the other amplifier sections.

It is a simple matter to keep these three grounds separated when multi-layer PCBs are used for the circuit. Single-layer PCBs represent a different challenge. In this case, be sure to keep the ground return paths and ground loops of the analog section out of the path of the other two sections, primarily the output section. High currents flow through the output traces and should have a path for easy flow of the return currents. Placing the ground plane underneath these traces or alongside them will provide such a path. Figure 4 illustrates how the ground loops and return currents flow in the ground plane.

The headphone section is not as critical since it is inactive when the Class-D circuit is active. The same considerations for current return paths and ground loops still apply, however, in order to keep distortion in the circuit to a minimum.

The actual ground area should be as large as possible, no matter how many layers the PCB has. This will reduce the trace inductance of the ground plane, reducing the disturbances between amplifier sections created by current flow. The large area of the ground plane also acts as a heat sink for the device. The area required will depend upon the application and the desired thermal resistance from the sink (ground plane) to the ambient (θsa).

Sensitive nodes

All sensitive nodes for the amplifier are shown as bold lines in Figure 3. The most sensitive nodes in the Class-D circuit are the amplifier inputs and outputs. The inputs are AC coupled, and any trace between the input of the amplifier and the capacitor acts as an antenna, picking up any radiated signals that are then increased by the total gain of the audio amplifier. These capacitors should be placed as close as possible to the input pins.

The inductors in the output filter should be placed as close as possible to the IC to reduce any radiated emissions

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Figure 3. TPA032D04 Class-D audio power amplifier circuit

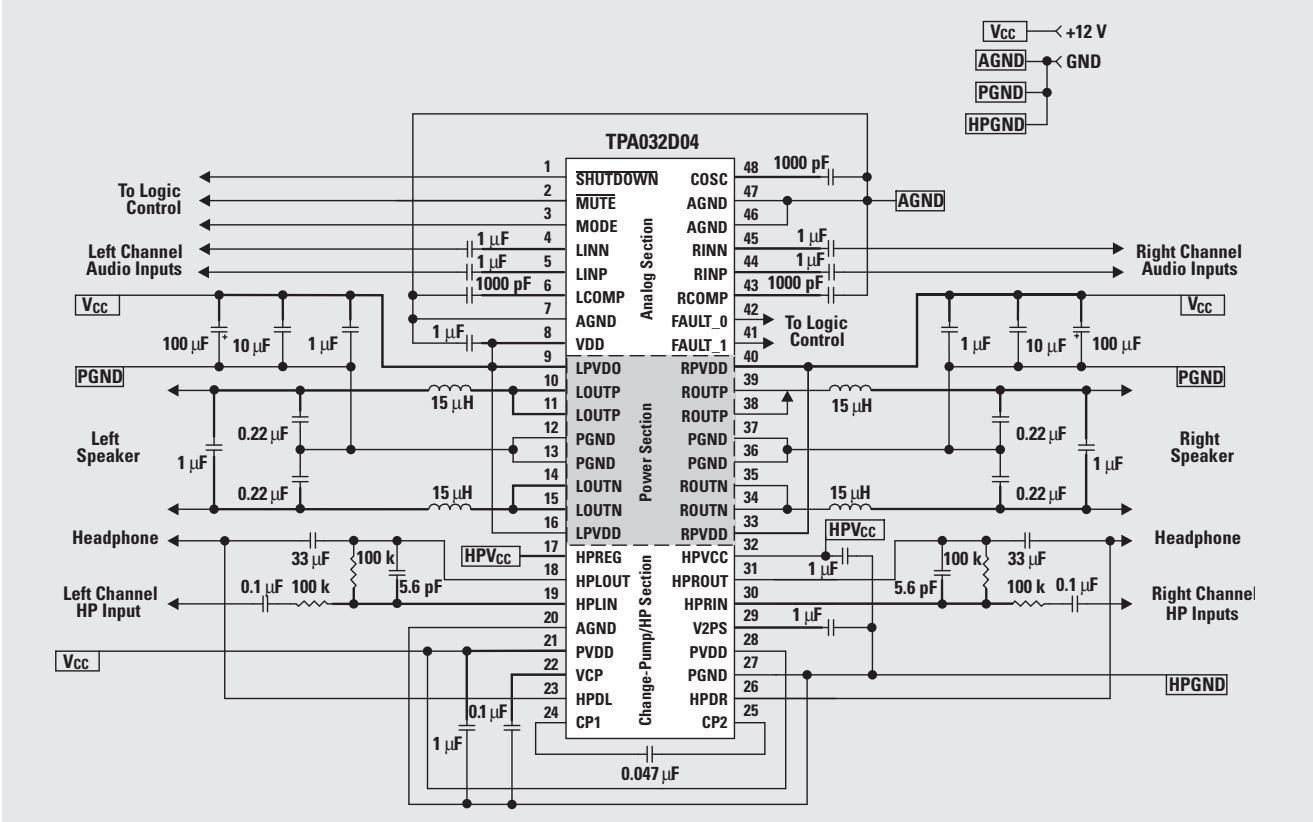

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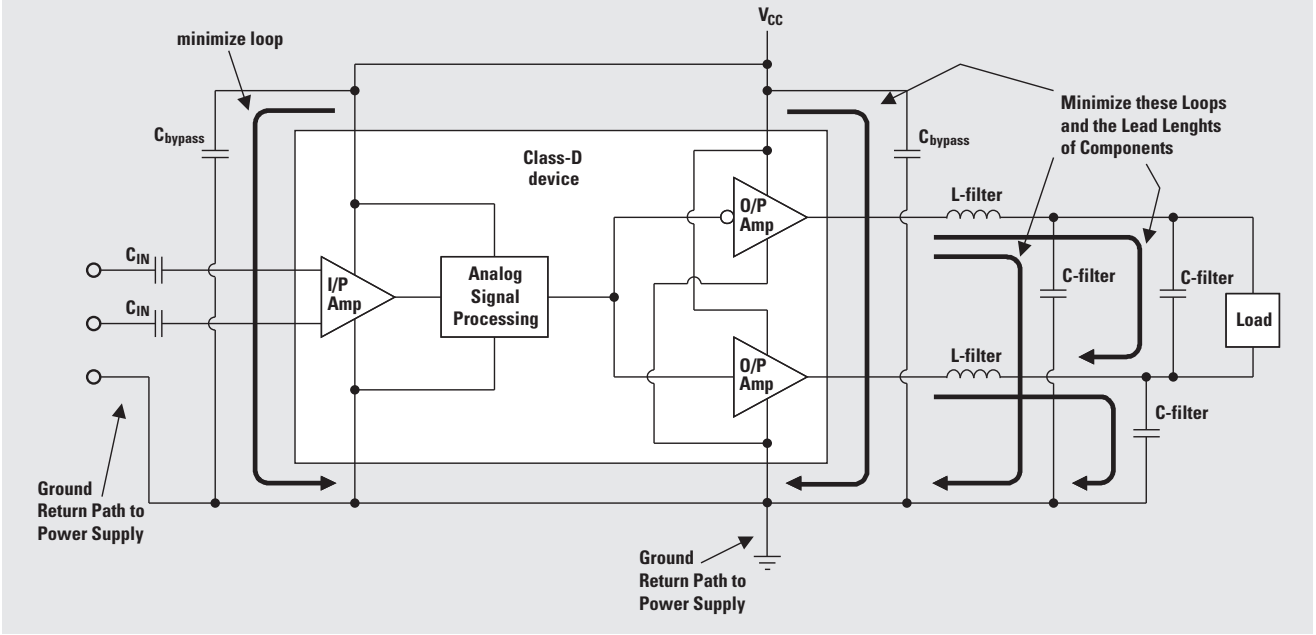
Figure 4. Output ground loops and return paths

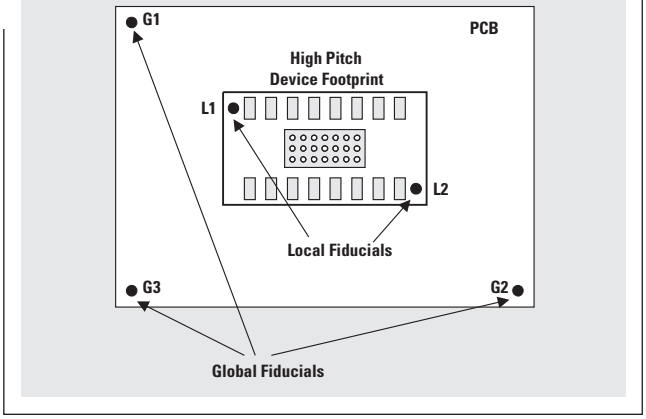


created by the rail-to-rail 250-kHz switching waveform. The signal on the load side of the inductor is mostly 20 kHz, with some 250-kHz ripple present. The output filter capacitors provide paths for the ripple and other high-frequency signals to bypass the load. These capacitors should be placed as close as possible to the inductors and should have a clear ground path back to PGND and the power-supply ground return paths.

The charge pump circuit supplies the charge for the MOSFET gates and is not particularly susceptible to distortion. It is still good practice to keep the traces to the capacitors in this circuit as short as possible.

The headphone circuit requires more consideration. The traces from the input pins for the left and right channels to the input capacitors and feedback components should be kept short to reduce noise pickup and amplification. This is due to the high input impedance of the amplifier inputs and the stray capacitance at these nodes that combine to allow signal from one channel to be injected into the other. Reducing the size of these resistors and decreasing the gain both can lower the amount of crosstalk.[5]

Figure 5. Two types of commonly used fiducials



Fiducials

The use of fiducials is recommended to increase the accuracy of part placement, particularly on boards using small-pitch surface-mount components and devices. The fiducial is a mark that is placed on a PCB during the etching process, and it can be bare copper or copper covered with various protective coatings or platings. The fiducial provides an optical reference to the manufacturing equipment that is used to align the boards properly during assembly. The information in this section can be obtained in greater detail from Reference 4.

Two types of fiducials, global and local, are commonly used, as shown in Figure 5. The global fiducials are placed on the corners of the PCB and serve to align the entire board. The number of fiducials required depends upon the type of accuracy needed. One fiducial is used to correct horizontal and vertical offset errors. Two fiducials will, in addition, correct any rotational errors. Three are used when it is also necessary to correct errors introduced by nonlinear distortions of the PCB that occur during assembly. These fiducials can be placed on any corner except when using two fiducials, in which case they should be placed in diagonally opposing corners.

The local fiducial is used when a fine pitch device is being placed on the PCB to ensure that it is accurately

positioned. A maximum of only two local fiducials is used, and they provide the same information as for the global fiducials mentioned earlier. The only differences are that these fiducials must fall within the land pattern of the device and, if only one fiducial is used, it should be placed toward the center of the land pattern if possible.

The diameter of fiducials should be between 1 mm (39.4 mils) and 1.5 mm (59 mils), with all of the fiducials the same size on a given board. A zone of at least twice the radius from the center of the fiducial should be kept clear of any other objects. They should not be any closer to the edge of the board than 5 mm (200 mils) plus the radius of the fiducial. The solder mask must be kept far enough away from the fiducial to prevent any solder mask from bleeding onto and obscuring it. If components are placed on both sides of a PCB, then fiducials can be placed on both sides. It is a good idea to keep the internal layers underneath the fiducials the same so that the appearance of the fiducials is identical to the optical device.

Trace thickness

The traces of the PCB should be wide enough so that they neither create any large voltage drops due to large trace resistance nor create large trace inductance. This will mostly impact the traces that carry larger currents, such as the power supply and output traces. The trace resistance will depend upon the thickness of the copper, given in ounces per square foot of board, and the length and width of the trace. One-ounce and two-ounce copper is commonly used in EVMs, with one-ounce copper being approximately 0.035 mm (1.4 mils) and two-ounce copper being approximately 0.07 mm (2.8 mils) thick. Table 2 shows the amount of current that can pass through a specified trace area for a given temperature rise (ΔT). This information was derived from IPC 2221[6] and has already been derated by 10% to allow for variations due to processing.

The resistance of a trace may be calculated for one-ounce copper based on the formula $R = 0.00502\Omega xL/(WxT)$, where R is the resistance in ohms, L is the length of the trace in mils, W is the width of the trace in mils, and T is the weight of the PCB copper in ounces.

Summary

PCB design can limit the performance and/or reduce the reliability of the Class-D circuit if some basic layout concepts are not followed. Modern PCB manufacturing techniques allow good, thorough isolation of the IC and component pads and vias through the accurate placement of solder mask. This in turn allows the area to which the solder paste is applied on the board to be reduced, focusing the flow of the paste during reflow soldering on the desired areas. This forms a stronger mechanical bond between the device or component and the PCB. This is particularly important when using PowerPAD devices to help counter the tendency of solder to be wicked from the IC pins toward the PowerPAD.

The reduction of ground loops and provision of current return paths for inputs and outputs enhance the isolation of these two sections, maintaining quality performance from the amplifier. The consideration of the more sensitive nodes of the TPA005D1x and TPA032D0x devices reduces noise pickup and crosstalk between the channels. The addition of a few fiducials then ensures that the parts will be where they need to be during the assembly process. See Reference 7 for more information on the Class-D audio power amplifiers.

Table 2. Current and trace area impact on temperature rise, resistance for external conductors

MAX CURRENT (A)	MAX ΔT (°C)	MINIMUM TRACE WIDTHS (in.)			1-in. TRACE RESISTANCE (mΩ)		
		0.5 oz.	1.0 oz.	2.0 oz.	0.5 oz.	1.0 oz.	2.0 oz.
1	10	0.030	0.015	0.007	335	335	359
	20	0.020	0.010	0.003	502	502	837
	30	0.014	0.007	0.002	717	717	1255
2	10	0.080	0.040	0.020	126	143	126
	20	0.050	0.025	0.014	201	201	179
	30	0.040	0.018	0.008	251	295	314
3	10	0.120	0.120	0.030	84	42	84
	20	0.080	0.080	0.020	126	63	126
	30	0.060	0.062	0.014	167	81	179

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