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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as “how-to” instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Amplifiers: Op Amps
- General Interest

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

SHDSL AFE1230 application

By Hui-Qing Liu
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Introduction

Symmetric high-bit-rate digital subscriber line (SHDSL) was defined by the new ITU international standard G.991.2 in February 2001. This digital subscriber line uses advanced line coding and error correction technology, baseband Trellis-coded pulse amplitude modulation (TC-PAM), and symmetric power spectral density (PSD) to achieve symmetrical bit rates up to 2.3 Mbps at distances of over 12,000 ft. It provides full-duplex transmissions with multiple rates from 192 kbps to 2.3 Mbps over a single twisted-pair copper wire with extended transmission reach. SHDSL was developed to replace older DSL technologies such as HDSL, SDSL, ISDN, and IDSL. It is often used to provide symmetrical T1 and E1 service.

The implementation of SHDSL technology is based on a VLSI chipset including a digital signal processor (DSP) and an SHDSL analog front end (AFE). The DSP performs the functions of framer, encoder, decoder, and PAM engine under the control of an on-chip or off-chip microprocessor. The AFE provides the necessary interface between the DSP and the telephone line, which includes A/D converter, D/A converter, shaping filter, gain control, and line driver. With the chipset, a minimal but necessary external circuit is needed to provide the best speed, power, linearity, and signal-to-noise ratio (SNR) for the system. In this article a new Texas Instruments SHDSL analog front end, the AFE1230, and its basic application design are described to enable users to take full advantage of AFE1230 for DSL applications. This article includes details of both the external digital interface configuration and the analog interface circuit design.

AFE1230 function

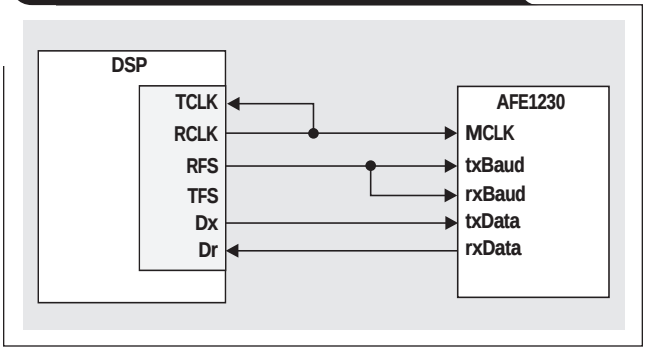
The AFE1230 provides upstream and downstream data conversion over a wide range of speeds from 64 kbps to 2.5 Mbps, so that it covers a range of bit rates beyond that of standard SHDSL. As a transceiver, it consists of a transmitter and receiver. The transmitter section includes a digital interpolation filter; a 16-bit ΣΔ D/A converter; a user-selectable fifth- or seventh-order, switched-capacitor (SC) low-pass filter; and a differential output line driver. The receiver section includes a digitally programmable gain amplifier, a 16-bit ΣΔ A/D converter, and a digital decimation filter. Via the digital serial interface, the AFE1230 receives a 24-bit word including a 16-bit data word and an 8-bit control byte. The received 16-bit word is upsampled by 2 through a digital interpolation filter to remove out-of-band images in the signal; it is then oversampled by the ΣΔ modulator with a factor of 12 and processed by the multi-level DAC section to facilitate the D/A conversion. The quantization noise from the ΣΔ D/A is then filtered by the on-board tx filter (the fifth- or seventh-order, SC Butterworth low-pass filter). At the same time, the signal is shaped by the tx filter to meet the SHDSL PSD requirements. Depending on the particular response desired, the tx filter can be programmed for three different corner frequencies as well as two filter (fifth- or seventh-order) configurations. The subsequent analog signal is sent to the on-chip line driver with an appropriate line transformer to provide up to 14.5-dBm power to a 135-Ω line for SHDSL. In addition, the on-chip line driver can be used as an output buffer to generate 17 dBm into a 135-Ω line via an external line driver such as the OPA2677 or OPA2607 for HDSL2 and DMT signal. The transmit power is controlled by the digital input.

In the receiver section, a differential input amplifier sums the signals from the line and hybrid path to perform first-order analog echo cancellation and programmable gain control. A fourth-order cascaded ΣΔ A/D converter with an oversampling ratio of 24 digitizes the resultant signal. The subsequent signal is processed by a fifth-order sinc filter and a programmable IIR filter for additional quantization noise reduction and downsampling as well as droop compensation. The resulting digital signal is then sent to the digital serial interface for processing by the DSP. The receiver section also can be set in Line Receiver Only mode (hybrid input is internally connected to common-mode voltage) or Hybrid Receiver Only mode (line input is internally connected to common-mode voltage) for different applications.

Digital interface configuration

The AFE1230 uses a standard four- or five-line digital serial interface operating in the slave mode. It can easily communicate with DSPs specifically designed for DSL applications or with general-purpose DSPs, such as TI's TMS320C5x™ or TMS320C6x™ series or analog devices SHARC series. Figure 1 shows a digital interface configuration of the AFE1230 connected to the serial port of a general-purpose DSP.

Figure 1. AFE1230 digital interface with general-purpose DSP



The AFE1230 has five digital interface lines: MCLK (master clock), txBaud (transmit baud clock), txData (input data), rxBaud (receive baud clock), and rxData (output data). The AFE1230 pins—MCLK, txBaud/rxBaud (txBaud is connected with rxBaud), txData, and rxData—are connected to the DSP pins—RCLK (receive clock), RFS (receive frame sync signal), Dx (transmit data), and Dr (receive data), respectively. The 32-bit DSP is set in multichannel mode to achieve 48-bit word serial communication required from the AFE1230. The DSP generates clocks of RCLK and RFS. The RCLK drives both TCLK (transmit clock) in the DSP and MCLK in the AFE1230. The RFS drives both txBaud and rxBaud in the AFE1230. The TFS (transmit frame sync signal) is open due to multichannel-mode configuration in the DSP. Following is a description of the five lines used for serial communication. Their timing is shown in Figure 2.

MCLK

The master clock of AFE1230, generated by the DSP, can vary from 1.28 MHz to 40.8 MHz (37.12 MHz for E1), with a 50/50 duty cycle required. It runs at 48 times the txBaud rate.

txBaud

The transmit data baud clock, generated by the DSP, can vary from 26.7 kHz to 850 kHz (517.33 kHz for T1 and 773.33 kHz for E1). One period of txBaud consists of 48 periods of MCLK. The pulse width of txBaud, t_w, should not be smaller than one period of MCLK. The txBaud is a frame sync signal that indicates the beginning of each serial word transfer. When txBaud is high, the rising edge of MCLK detects this signal; and the next rising edge of MCLK will sample the first bit of the serial word. After the txBaud is asserted, it is not checked again until the entire word has been received. The falling edge of txBaud can occur any time, t_f, during the txBaud period. txBaud and rxBaud must be the same frequency and synchronous with MCLK; however, the phase of these two signals may be different. For example, the DSP can generate both RFS and TFS separately to interface to the AFE1230. In the case of a phase jump (i.e., when the rxBaud or txBaud symbol clocks move one MCLK period forward or backward, resulting in 49 or 47 MCLK cycles per rxBaud), the receive data will be invalid for six symbol periods while the data settles to final value.

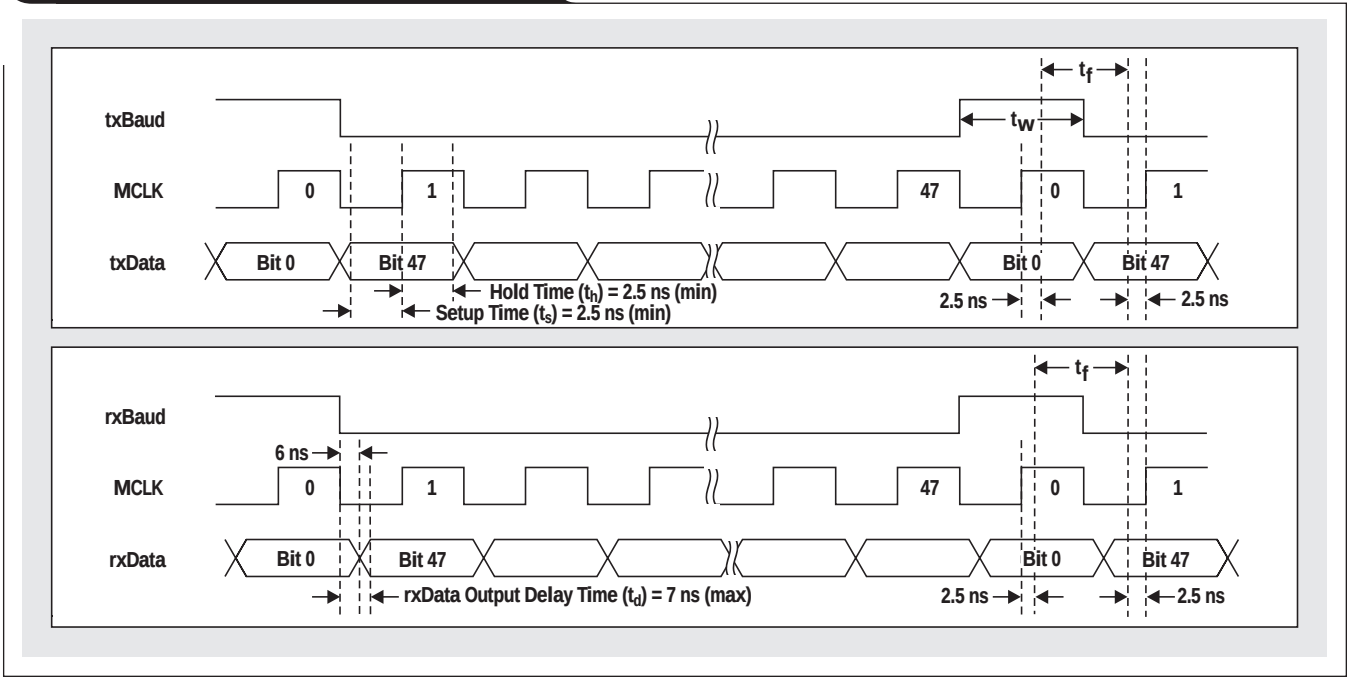
txData

The input digital data of AFE1230 comes from an external DSP with 48 bits per txBaud period. The 48 bits include two 16-bit words of DAC input data and two 8-bit control bytes. The DAC is updated two times per symbol period, and data is latched by AFE1230 on the rising edge of MCLK. txData must be stable at least 2.5 ns before and after the rising edge of MCLK (see Figure 2). The data is coded in two's complement with 16 bits.

rxBaud

The receive data baud clock, generated by the DSP, can vary the same as txBaud, from 26.7 kHz to 850 kHz (517.33 kHz for T1 and 773.33 kHz for E1). A period of rxBaud consists of 48 periods of MCLK. The pulse width of rxBaud, t_w, should not be smaller than one period of MCLK. The rxBaud is a frame sync signal that indicates the beginning of each serial word transfer. When rxBaud is high, the rising edge of MCLK detects this signal; and the next rising edge of MCLK will sample the first bit of the serial word. After the rxBaud is asserted, it is not checked again until the entire word has been transmitted. The falling edge of txBaud can occur any time, t_f, during the rxBaud period. The rxBaud and txBaud lines can be activated independently or at the same time.

Figure 2. AFE1230 digital interface timing



rxData

The output digital data of AFE1230 is sent to the external DSP as 48 bits per rxBaud period. The 48 bits include two 16-bit ADC data words and two 8-bit control data words (reserved). The ADC is read two times per rxBaud period, and rxData is updated by AFE1230 at the falling edge of MCLK. The maximum delay of the rxData is 7 ns (see Figure 2). The data is coded in two's complement with 16 bits.

Digital loop-back

AFE1230 provides a digital loop-back function that tests the DSP signal and the AFE digital interface. With bits 2 and 1 set as "01" in the digital input frame, the AFE1230's txData will connect with rxData internally to form digital loop-back.

Analog interface circuit

Two basic application analog circuits of AFE1230 are introduced here. The first circuit is for SHDSL as shown in Figure 3. This circuit has an on-chip line driver capable of providing 14.5-dBm power directly to the 135-Ω line. The other circuit is for HDSL2, shown in Figure 4 (next page). It has an off-chip external line driver, the OPA2677, to provide 17-dBm power to the 135-Ω line. Some of the design issues involved in these external analog circuits are transmitter power, power spectral density, output noise, input noise, input dynamic range, echo cancellation, and power dissipation. These issues are important and necessary to address here.

Figure 3. AFE1230 on-chip driving circuit for SHDSL

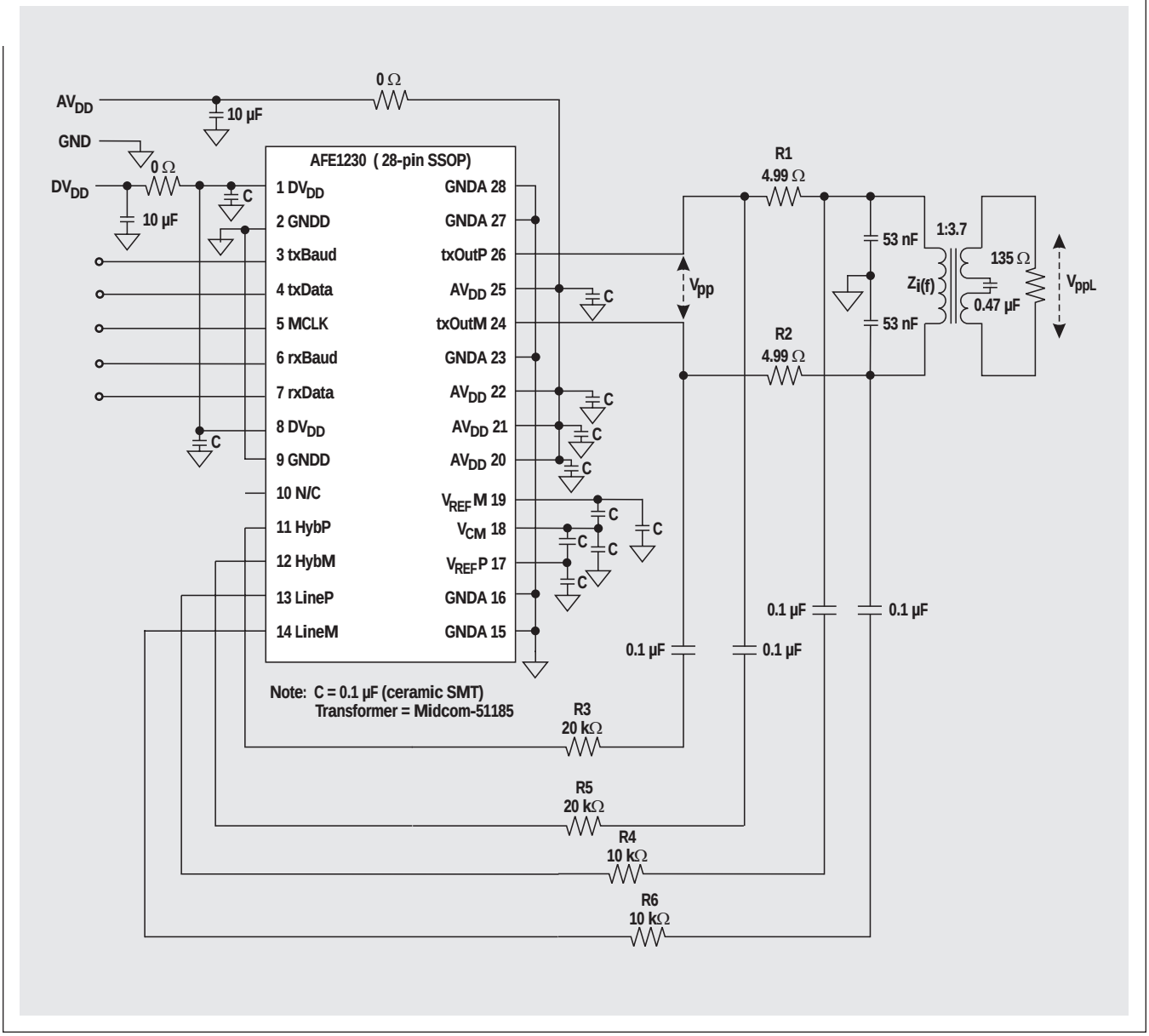
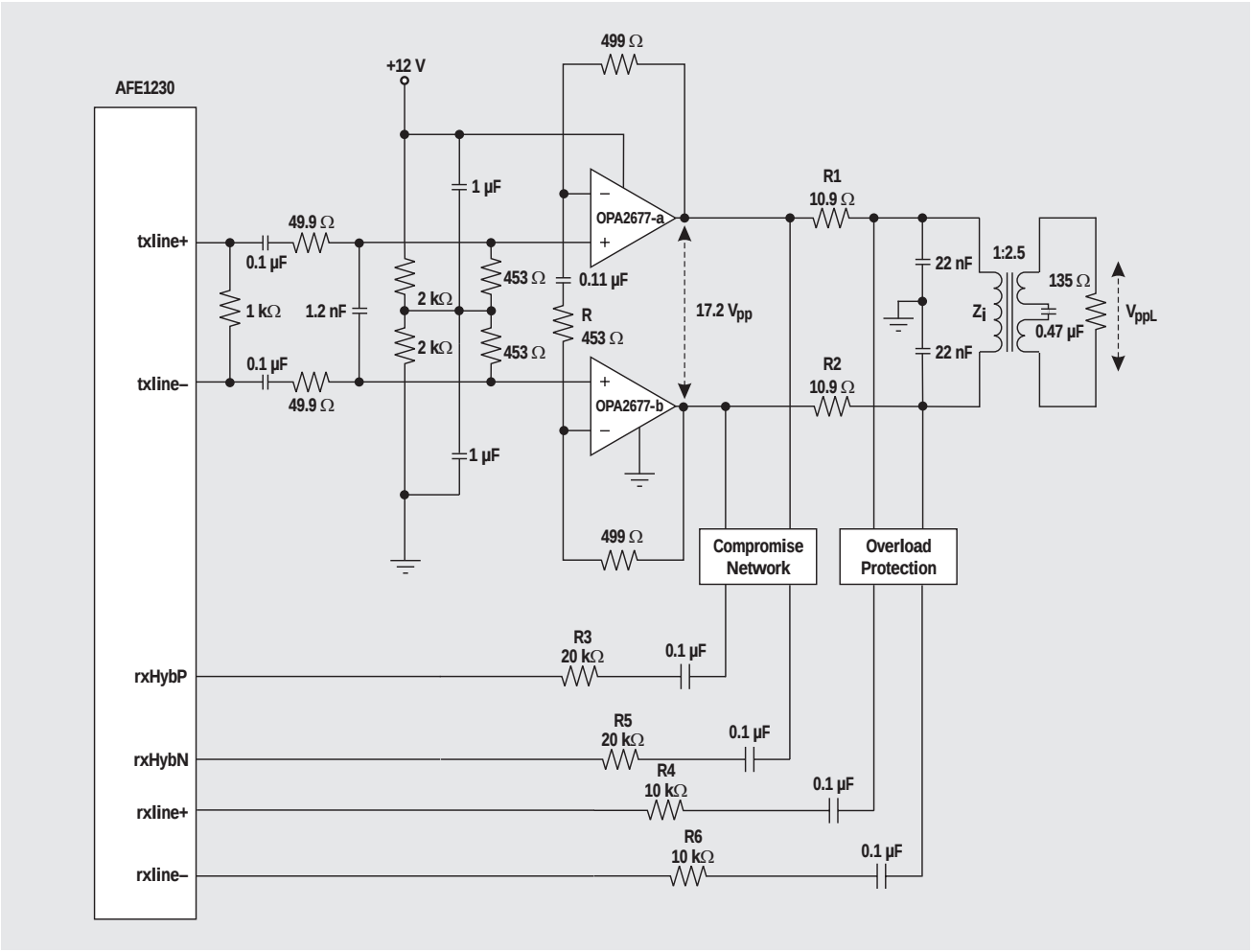


Figure 4. AFE1230 off-chip driving circuit for HDSL2



Transmitter power

To provide the power required by the specific line, it is necessary to consider the critical factors of output voltage swing of the AFE, maximum peak current of the on-chip driver, turns ratio of the transformer, peak-to-average power ratio (PAR) of the signal, and line impedance. These factors are directly related to circuit components; for example, the matching resistances R1 and R2 in Figure 3 and the transformer turns (device/line) ratio, n, directly affect the voltage on the line impedance and the load current to the driver. R1 and R2 are used to control far-end reflection and maximize the energy exchange between the AFE and the line. The turns ratio, n, is used to step up the voltage required by the line; however, if n is too high, it will create too much load for the driver and step down too much received signal voltage.

According to the SHDSL standard, the total power and power spectral density are measured with a load impedance of 135 Ω within a specific frequency range. If in Figure 3 we assume that the total power is 14.5 dBm, the PAR is 3.0, and the differential peak-to-peak output voltage from the AFE1230 is 6.2 V, then n is 3.7, and R1 and R2 are each 4.99 Ω. Such a design requires peak current of 158 mA, which is well within the AFE1230 on-chip driver's peak current capability of 230 mA.

The calculations for these values are determined by the following equations.

$$P_{dBm} = 10 \times \log(1000 P_w),$$

where P_{dBm} is the line power in dBm and P_w is the line power in watts.

$$P_w = V_{rms}^2 / R_L,$$

where V_{rms} is the voltage on the line and R_L is the impedance of the line (load impedance).

$$V_{ppL} = 2 \times PAR \times V_{rms},$$

where V_{ppL} is the peak-to-peak voltage on the line and PAR is the peak-to-average ratio of the power. PAR is 3.0 for SHDSL and 4.0 for HDSL2.

$$n = 2V_{ppL} / V_{pp}$$

(for matching line impedance), where V_{pp} is the output peak-to-peak voltage of AFE1230.

$$R1 = R2 = 135/(2n^2).$$

If these equations are used for the higher power of HDSL2, the matching resistances R1 and R2 in Figure 4 are 10.9 Ω each, and the transformer turns ratio, n, is 2.5. The external line driver must provide differential output peak-to-peak voltage of 17.2 V and peak current of 199 mA to deliver 17.3-dBm power to the HDSL2 line. TI's OPA2677 is suggested as the external line driver with a single +12-V power supply. Since the AFE1230 output differential, peak-to-peak voltage is 6.2 V, the ac gain of the external driver should be 2.8 V/V. With a 12-V supply, the dc offset (common-mode voltage) is 6 V. The ac gain, G, is estimated by the equation

$$G = 1 + (2R_F / R),$$

where R_F is the feedback resistance on OPA2677. In Figure 4, R_F is 499 Ω and R is 453 Ω.

Output noise

The AFE1230 has an on-chip, digital-interpolation, low-pass filter and a fifth- or seventh-order SC low-pass filter to remove the images from the digital input signal and D/A quantization noise. However, other sampling images appear at frequencies of multiple MCLK in the transmit output PSD due to the internal sample and hold function of the SC filter. The power of these images is relative to signal power, speed, and external low-pass filter cutoff frequency.

During normal operation, the output matching resistors and capacitor form a low-pass filter that reduces the power of these images to well below the PSD requirements of the SHDSL and HDSL2 standards. However, if the sampling rate (MCLK) is reduced while the low-pass filter cutoff frequency remains high, the first image will, of course, appear at a correspondingly lower frequency that may be within the SHDSL or HDSL2 signal band. At some point, lower sampling rates will produce an image, which can violate the appropriate PSD requirements. To reduce the power of these images, it is necessary to increase the sampling rate or improve the external analog low-pass filter.

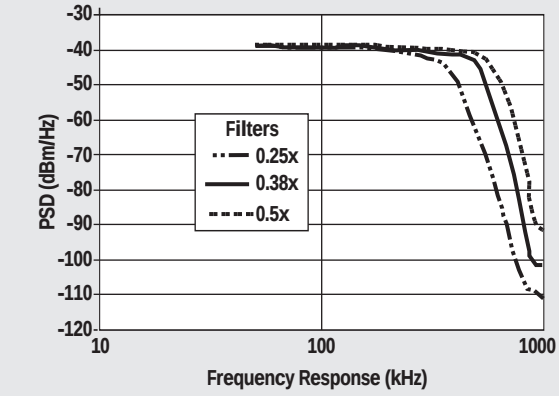
As an example, in Figure 3, the matching resistance and a capacitance of 53 nF contribute such a low-pass filter with cutoff frequency at about 650 kHz; in addition, the transformer acts as another first-order low-pass filter with cutoff frequency at about 2 MHz. These filters will greatly reduce the images. As a result, when the MCLK is 3 MHz, the power of the first image on the 135-Ω load can be reduced below –110 dBm/Hz; and, when the sampling rate of AFE1230 is fairly high, the power of the first image on the 135-Ω load can be limited below –120 dBm/Hz. These filters can also reduce high-frequency noise. The test shows that with a sampling rate of 1.25 MHz, 0.38× tx filter, and a full-scale, single-tone input with a 135-Ω load through the transformer, the circuit in Figure 3 can provide a transmit SNR of about 80 dB within the Nyquist band. If no signal is transmitted on the 135-Ω load, a transmit noise floor measured by HP spectrum analyzer is below –112 dBm/Hz in wide-frequency range.

Power spectral density

The transmit PSD provided by AFE1230, of course, should not exceed the PSD masks for all data rates; and total power into a 135-Ω line should fall within the range specified in the G.991.2 ITU standard for SHDSL. The spectral shaping is performed by appropriate DSP processing and by the transmit filter in AFE1230. However, the external filter and transformer will affect the spectral shape and are important factors in spectral shaping design.

With the circuit shown in Figure 3 and the input of a white noise generated in DSP, a transmit PSD can be measured. Figure 5 describes a PSD with white noise at a MCLK sampling rate of 30 MHz. These curves show the spectral shaping from the three user-selectable on-chip transmit filters (0.25×, 0.38×, or 0.5×) and external passive filters. If an appropriate FIR filter is applied to the white noise in the DSP before it is sent to the AFE1230, then the resulting PSD complies with the standard for the SHDSL PSD mask.

Figure 5. AFE1230 transmit PSD with white noise at MCLK of 30 MHz



Transformer

The key parameters of a line transformer are its turns ratio, primary inductance, leakage inductance, dc resistance, and total harmonic distortion. These parameters affect overall performance of the system. In practice, the transformer acts like a bandpass filter. The high-pass cutoff frequency is determined by the primary inductance, and the low-pass cutoff frequency is determined by the leakage inductance.

If the primary inductance is too high, the low-frequency components included in the signal will create a long tail in the impulse response of the echo path, which the equalizer in the DSP cannot remove. However, if the primary inductance is too low, it will reduce the signal bandwidth with a subsequent loss of information. This is particularly important in the case of low data rates. On the other hand, higher data rates require lower leakage inductance and better total harmonic distortion. A recommended transformer for AFE1230 G.SHDSL applications is the Midcom 51185,

which provides a turns ratio of 3.7, primary inductance of 2 mH, leakage inductance of 26 µH, dc resistance of 1.6 Ω, and total harmonic distortion of 80 dB.

Receiving signal and noise

Because SHDSL is a full-duplex data transmission system with overlapping spectra, the AFE1230 receives both line receive signal and transmit signal at the same time and in the same bandwidth. In Figure 3, the received line signal is reduced by a factor of 3.7 by the transformer and has a dynamic range of about 35 dB due to different line attenuation. The line signal includes delay distortion due to the limitation of the channel bandwidth. The received transmit signal is the transmit signal reduced through the voltage-dividing effect of the matching resistance and the line impedance. Since the line impedance changes with frequency, the voltage divider changes with frequency. This means that the total received signal is also a function of the frequency.

The AFE1230 also receives noise from a number of sources, which include thermal noise from random electron motion, impulse noise from power spikes, echo signals from terminal impedance mismatch, reflections from bridged taps, and crosstalk from inductive and capacitive coupling between two wires in the same cable. If not controlled, this noise can cause the failure of signal detection in some cases. To limit the noise, a band-limited low-pass filter is necessary even though there is an on-chip anti-alias (AA) filter included on the AFE1230.

In Figure 3, an FFT measurement of this circuit for the AFE1230 operating at a 30-MHz sampling rate (MCLK) shows that for a full-scale, single-tone signal through the filter, the SNR of the digital output is about 86 dB with a PGA gain of 0 dB, and 76 dB with a PGA gain of 21 dB within the Nyquist band.

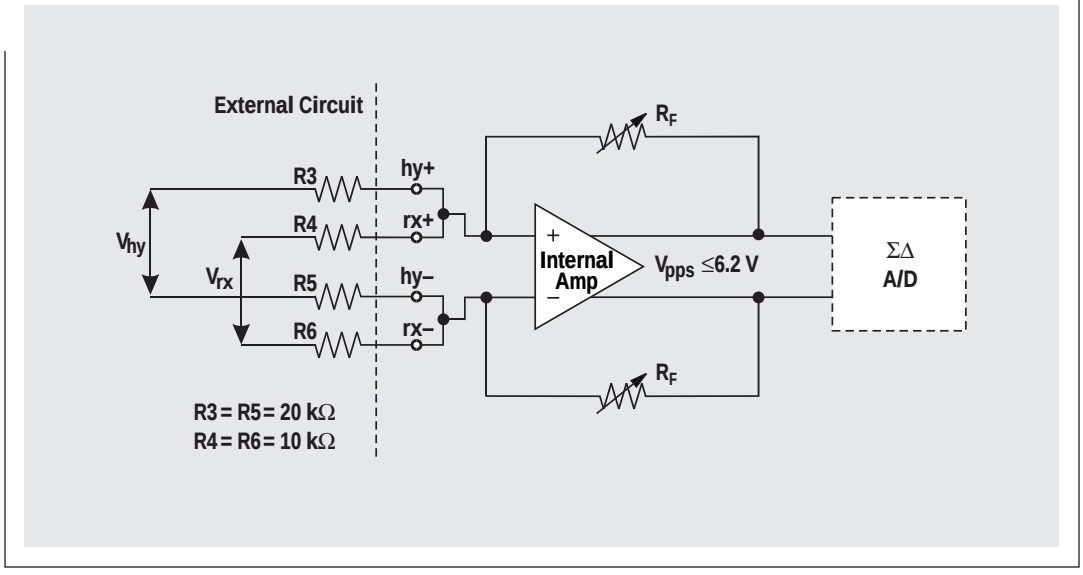
Echo cancellation

Echo cancellation is used in full-duplex data transmission systems to remove the transmit signal from the receiver signal. This is typically realized partially in an analog hybrid circuit and partially in the DSP. The hybrid circuit is actually an electrical bridge, formed by the line impedance, transmit matching resistance, receiver input impedance, and hybrid input impedance. When the bridge is perfectly balanced, the far-end reflection, near-end reflection, and trans-hybrid reflection will be zero. However, since the line impedance changes with frequency and line condition as well as with limitations of the hardware, an unbalance in this analog electrical bridge always exists.

In general, analog echo cancellation between the line transformer and the receiver input is the first step to remove the majority of the echo signal and reduce the dynamic range requirements of the receive channel A/D converter. Digital echo cancellation in the DSP is the final, precision step to remove the rest of the echo.

Figure 3 shows a basic hybrid circuit configuration with a resistor-only network. If line impedance is assumed to be a constant of 135 Ω, only resistors need to be inserted in the transmit path, receiver path, and hybrid path. A resistance of 10 kΩ is required for each receiver input, and 20 kΩ for each hybrid input. These four resistors are connected to the virtual ground inputs of the on-chip differential input amplifier to form a differential summing amplifier. This is shown in Figure 6. Since the receiver and hybrid paths have a phase difference of 180° from each other, the input amplifier subtracts their voltages to create

Figure 6. Echo cancellation with R network and internal receive amplifier



a first-order analog echo canceller. The output voltage of the summing amplifier, V_{pps}, is then digitized by the A/D converter. The analog echo cancellation can be determined by the following equations.

$$V_{pps} = (R_F / R4)V_{rx} - (R_F / R3)V_{hy},$$

$$V_{rx} = V_{line} + (1/2)V_{tx}, \text{ and}$$

$$V_{hy} = V_{tx},$$

where V_{line} is the signal from the line and V_{hy} or V_{tx} is the transmit signal from the AFE1230. The common-mode voltage of the receiver amplifier is half of the analog power supply and is set internally.

Unfortunately, in practice, the line impedance is not constant and changes with line condition and frequency. This change can be modeled by an RC or RLC network. A common way to match the line impedance is to insert an RC or RLC compromise network into the hybrid path to track the line impedance change (Figure 4). The RC components for different loops can be determined with line simulation models that include a line transformer equivalent circuit. When the compromise network is inserted in the hybrid path of the external circuit, the resistors R3 and R5 on the hybrid path and the dc block capacitors (0.1 µF) on both the hybrid and receive paths will be determined by the compromise network.

Conclusion

TI's analog front end, the AFE1230, provides an SHDSL transceiver interface function between a DSP and the local loop. With an appropriate external circuit, it will handle upstream and downstream data transmission over the telephone line. The AFE1230's standard 5-wire serial digital interface supports full-duplex communication with the serial port of a DSP. A 6-pin analog interface with simple passive external filters, a transformer, and a hybrid circuit insures power delivery and reception as well as echo cancellation in the DSL application. The fundamental external circuit design procedure, using either an on-chip line driver for SHDSL or an off-chip driver for HDSL2, is also described in this article. The main factors for the design are signal PAR, line power, driver, transformer, receiver dynamic range, PGA, and analog echo cancellation. For optimum system performance with good PSD and SNR, the transformer effect, receiver band-limited filter, and line impedance matching need to be considered in the external circuit design.

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Related Web sites

www.ti.com/sc/device/*partnumber*
Replace *partnumber* with AFE1230, OPA2607 or OPA2677

Synchronizing non-FIFO variations of the THS1206

By Tom Hendrick
Data Acquisition Applications

Introduction

The THS1007, THS1009, THS1207, and THS1209 are non-FIFO variations of the popular THS1206, four-channel, 6-MSPS, simultaneous-sampling ADC. These devices are used in high-speed, cost-sensitive systems that do not require the ADC to furnish an interrupt to the host processor. This article explains the steps required to synchronize the data output from these 10- and 12-bit, two- and four-channel, simultaneous-sampling data converters.

Part details

The THS1007 and THS1207 are 6-MSPS parallel devices with four analog inputs. The inputs can be configured for either two-channel differential or four-channel single-ended operation. The THS1009 and THS1209 are 8-MSPS parallel devices with two analog inputs that can act as one differential channel or two single-ended channels. As their names imply, the resolution of these devices is 10 and 12 bits.

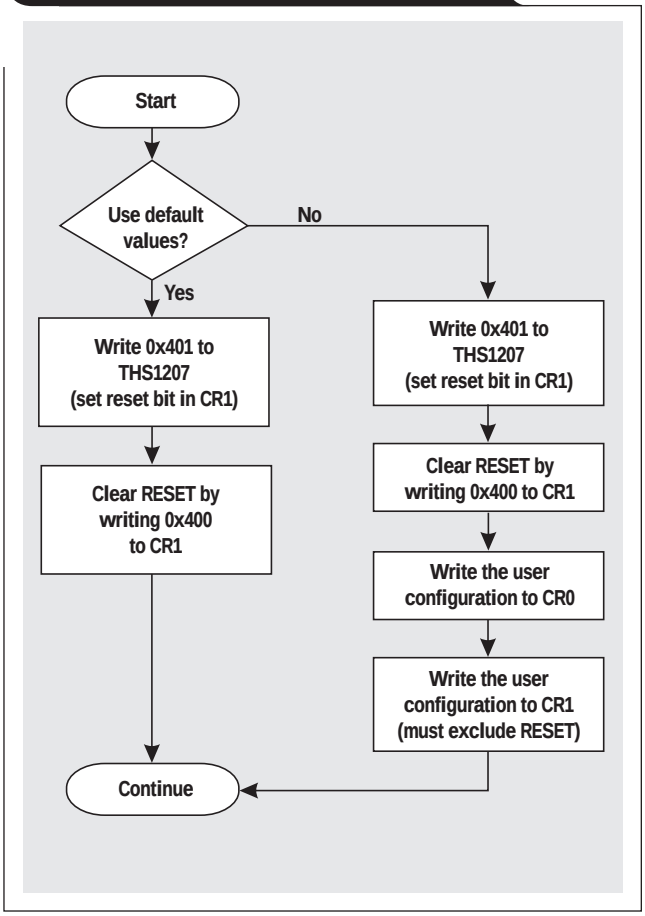
All four devices offer Auto-Scan modes, low-power operation, and a 3- to 5-Vdc digital interface for direct connection to digital signal processors. One of the major differences between these devices and their FIFO-enabled counterparts is that they operate only in continuous conversion mode. The conversion clock signal (CONV_CLK) cannot act as a conversion start pulse (CONVST) as it can in the THS10064, THS1206, THS10082, and THS12082 devices. The CONV_CLK signal needs to be maintained at a 50% duty cycle with a minimum frequency of 100 kHz.

Another major difference is that the data available (DATA_AV) signal found in the THS10064, THS1206, THS10082, and THS12082 devices is replaced with a signal referred to as "SYNC." The DATA_AV pulse on the FIFO devices acts as an interrupt source to the host controller. This allows the controller to perform other functions while the ADC is gathering data. The user has the ability to set a trigger level on the internal FIFO so that, when the trigger level is reached, the DATA_AV pulse is issued and the host processor reads out the acquired data from the ADC.

The SYNC output signal from the non-FIFO devices is not intended to act as an interrupt source to the host processor. The SYNC signal is merely an indication that data from channel 1 is available. The SYNC signal is active only in multi-channel modes; SYNC is disabled when single-channel operation is selected.

When two or more channels of the ADC are selected for operation, the SYNC signal indicates when channel 1 data is available to the data bus by bringing the SYNC pin low for an entire CONV_CLK cycle. To ensure that the SYNC pulse is properly aligned with channel 1, the "SYNC generator" within the device must be reset.

Figure 1. Example configuration flow



Resetting the SYNC generator

Bit 1 of control register 1 (CR1) can be considered the SYNC generator reset bit (SRST). This is similar to the THS1206's use of this bit to reset the FIFO. Writing a 1 to CR1, bit 1, during the configuration sequence of the THS1007, THS1009, THS1207, and THS1209 resets the SYNC generator and aligns the SYNC signal with channel 1.

Figure 1 shows the initialization sequence of the THS1207. After power-up, it is necessary to perform a device reset by writing hex values 0x401 and 0x400 to the device. If the default configuration values are desired, there is no need to perform any additional writes to the ADC. On the non-FIFO devices, the default value for control register 0 (CR0) is 0x020. The default value for CR1 is 0x030.

Table 1. Bit definitions for control registers CR0 and CR1 of the THS1207

REG	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CR0	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	RES	VREF
CR1	RBACK	OFFSET	BIN/2's	R/W	RES	RES	RES	RES	SRST	RESET

Because the default configuration values select single-channel operation, the SYNC pulse is disabled and there is no need to reset the SYNC generator.

If multiple-channel operation is desired, it is necessary to set the SRST bit as part of the user configuration write to CR1 (CR1 bit 1 = 1). It is not necessary to clear the SRST bit once it has been set.

A popular debug feature of the 12-bit ADCs in this device family is the register readback function. It allows the user to verify the contents of both the CR0 and CR1 registers (see Table 1) by performing two successive reads from the data bus. Shown as "RES" in the 10-bit data sheets, bit 9 of CR1 provides the same functionality on the THS10xx devices when combined with some simple software intervention. The 10-bit parts perform an internal "shift right by two" that requires the user to shift the resultant data 2 bits to the left. Bit 4 will appear set on register readback, indicating that the SYNC signal is at an active-low, static level. Note that the SYNC pulse is not available during register readback operations.

Reading data

Proper data readings depend on the proper application of the read signal. As with their FIFO-enabled counterparts, the THS1007, THS1009, THS1207, and THS1209 can be configured with independent, active-low read-and-write strobes. Active-low CS0 and active-high CS1 provide chip selection to the device and can be tied to static levels if desired.

With the non-FIFO devices, it is necessary to issue a read strobe after each CONV_CLK. As mentioned earlier, it is not appropriate to consider the SYNC pulse as an interrupt source to the host processor. The SYNC pulse is merely an indication that data currently available is the data acquired from channel 1.

Recall that the SYNC pulse is not available when the device is configured for single-channel operation. This is true for the two-channel THS1009 and THS1209 as well as for the four-channel THS1007 and THS1207. The SYNC pulse is active only when two or more channels are selected for conversion.

Data setup times are listed in the data sheets as "t_{SU}(CONV_CLKL_READL)." The read strobe should be applied after this setup time but before the subsequent falling CONV_CLK edge. Failure to read the data bus within each conversion cycle, or multiple reads during the same conversion cycle, can cause the SYNC pulse of the THS1007, THS1009, THS1207, and THS1209 to behave erratically. Setting bit 1 of CR1 will clear erratic SYNC pulse behavior.

Figures 2 and 3 show the result of setting the SRST bit. In both cases, a THS1207 was configured for three single-ended analog inputs, using SCAN mode to read the data. The /RD strobe was disabled. The conversion clock is intentionally stretched when channel 1 is active to indicate where the SYNC pulse should be. Figure 2 shows the results of writing 0x090 to CR0 and 0x4C0 to CR1. Figure 3 shows the results of writing 0x090 to CR0 and 0x4C2 to CR1.

As shown in Figure 2, the SYNC signal appears erratic. By setting SRST = 1 in CR1, the SYNC signal goes active low on the falling edge of the conversion clock, indicating the position of channel 1 conversion data.

Figure 2. SRST = 0

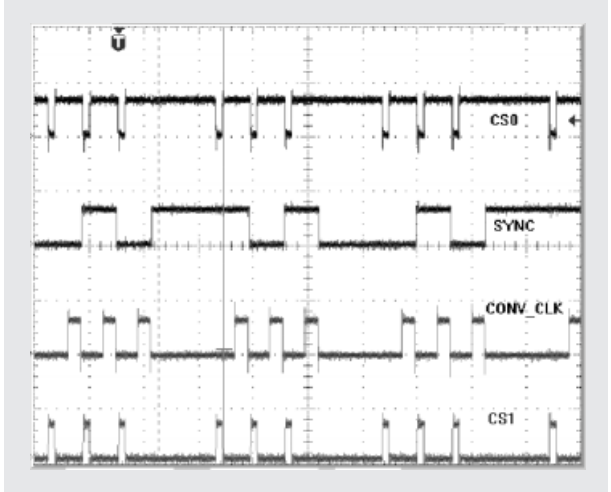


Figure 3. SRST = 1

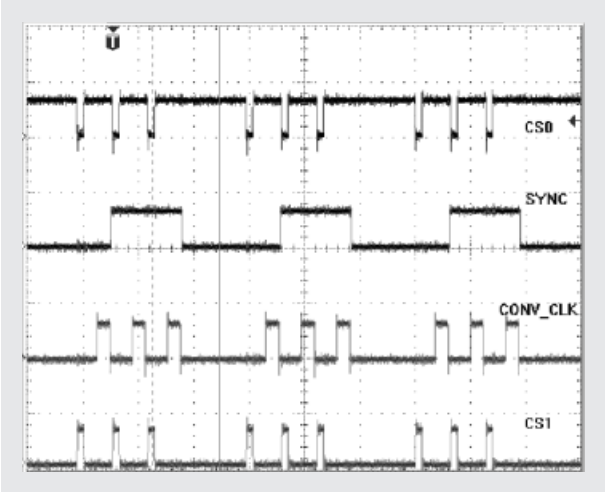


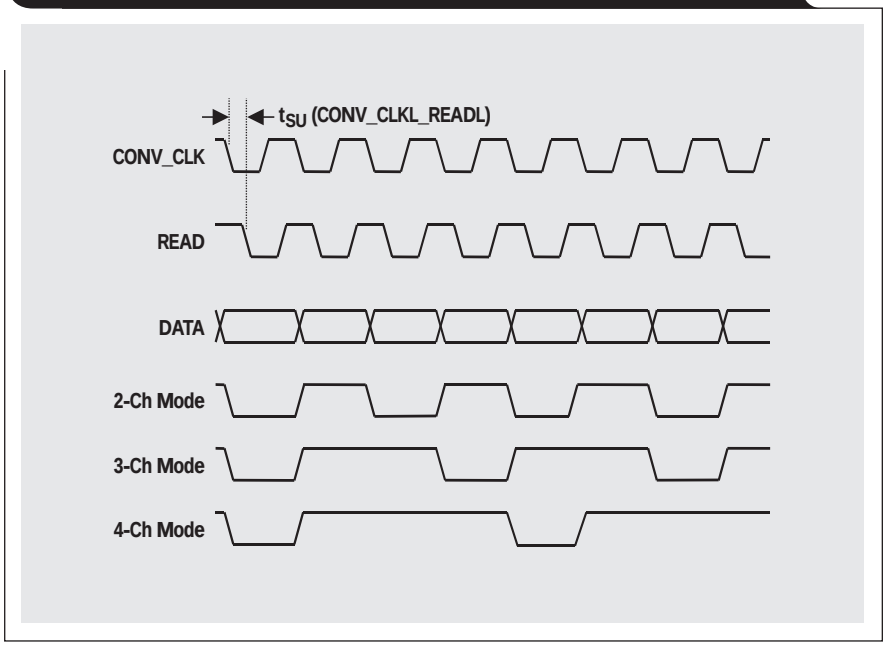
Figure 4 shows the relative timing of the SYNC signal in two-, three-, and four-channel modes. The SYNC signal will appear at half the CONV_CLK frequency in two-channel mode, one-third the CONV_CLK frequency in three-channel mode, and one-quarter the CONV_CLK frequency in four-channel mode. As related to Figures 2 and 3, the READ strobe shown in Figure 4 is the logical combination of CS0 and CS1 (valid chip select conditions).

Understanding the behavior of the SYNC signal plays a vital role in the development of a low-cost data acquisition system using the THS1007, THS1009, THS1207, and THS1209. The same 32-pin TSSOP package and common pinout throughout the two- and four-input converters provide the ability to upgrade to the FIFO-enabled THS10064, THS10082, THS1206, and THS12082 devices without costly hardware changes. For the latest data sheets and additional application information, please visit the Texas Instruments Web site.

Related Web sites

www.ti.com/sc/device/*partnumber*
Replace *partnumber* with THS1007, THS1009, THS1206, THS1207, THS1209, THS10064, THS10082 or THS12082

Figure 4. SYNC pulse in two-, three-, and four-channel modes



SWIFT™ Designer power supply design program

By Philip Rogers, *Applications Specialist, Power Management Products,*
and John Bishop, *Applications Specialist, High-Performance Linear Products*

Introduction

The SWIFT Designer power supply design program enables both novice and experienced designers to produce single-output, step-down converter designs with ease. This program uses the Texas Instruments TPS54xxx family of internal-MOSFET power-switch controllers for minimal parts count.

What is SWIFT Designer?

SWIFT Designer is a tool developed to do many of the tasks you may not have time to do. It can reselect all the parts with each change you make.

The design can be optimized for size or efficiency. The program will select all of the controllers that will work for the selected design, load them into a selection box on the schematic, and choose the one best suited.

You may override the program and select any of the controllers in the selection box. Other user-selectable components include the input capacitor, output capacitor, and output inductor.

The design may be saved for future use and/or printed. Documentation includes a complete schematic, bill of materials, loop response plot, efficiency plot, design specifications and parameters, and stress analysis of the major components.

An estimated size for the design on a printer circuit board is given. Note that this is a relative measurement that is greatly dependent upon the layout rules for your particular requirements.

To obtain the SWIFT Designer program, go to www.ti.com/sc/analogmsp and, under POWER MANAGEMENT, click on Engineering Design Utilities. Choose the appropriate program window to start the download menu. If you want to check program version information before downloading, click on the SLVC002 link first.

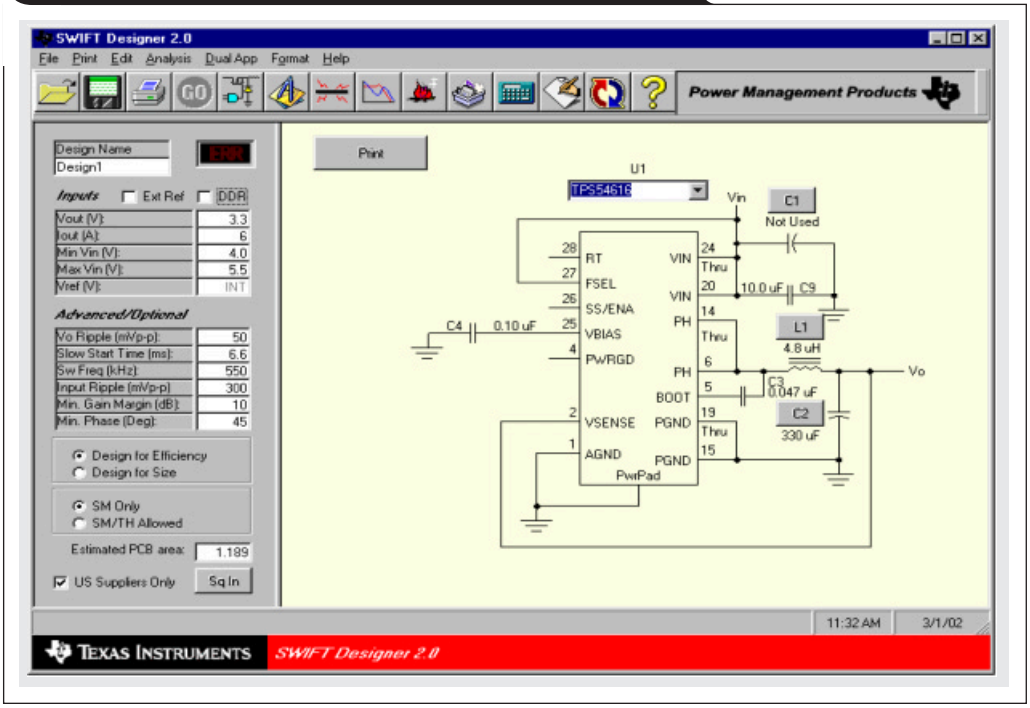
Installation instructions

To install SWIFT Designer, it is recommended that you first download the file to your hard drive, then unzip the file, and finally run 'SLVC001x.exe with no other programs running.

If you are installing this software on Microsoft® Windows® 9x or Windows NT® 3.5 operating systems, you will probably be asked to reboot the system after the installation of Windows Installer. This is normal for systems without the Installer service previously installed and is a one-time installation. The installation of SWIFT Designer will continue after the reboot. SWIFT Designer itself does not require a reboot.

If you are installing a newer version of the software, perform an uninstall first; then install the new version. Otherwise, Windows Installer looks for the old version and reinstalls it for you. This is a feature of Installer and is not related to SWIFT Designer. Versions 2.00, build 169 or later, can be updated by downloading the update file (which contains three zipped files) and copying these files to the TI\SWIFT subdirectory. Note: Versions 1.xx have a completely different database than Version 2.00 and are not compatible.

Figure 1. SWIFT Designer showing the default design



Running SWIFT(ly)

The installation program places an icon onto your desktop called “SWIFT Designer.” This icon may be used to launch the program. The first window that opens contains program-input fields and a schematic (Figure 1). To complete your first design using default parameters, click on the “GO” power button on the toolbar.

To generate a design specific to your needs, enter new inputs and again click the "GO" button. The program will automatically select the devices for the new design.

Supported devices

Table 1 indicates the parts supported by SWIFT Designer according to the output voltage and current.

Table 1. Supported devices

OUTPUT VOLTAGE (V)	CURRENT	
	3-AMP	6-AMP
Adj.	TPS54310	TPS54610
0.90	TPS54311	TPS54611
1.20	TPS54312	TPS54612
1.50	TPS54313	TPS54613
1.80	TPS54314	TPS54614
2.50	TPS54315	TPS54615
3.30	TPS54316	TPS54616
Ext. Ref.		TPS54672

When voltage or current values are entered in the corresponding input field and the "GO" button is clicked, the program places all applicable devices into the "U1" list box. Clicking the down arrow at the right displays the possible devices. Selecting one of these devices causes the program to respond with a new design based on the selected device.

File menu

The File menu has four submenu options: Open Design, Open EVM Design, Save Design, and Exit.

The Open Design submenu opens a file that has been saved. This is especially useful for updating or making changes to a previous design. The resulting design can then be either saved under the same file name or given a new name.

The Open EVM Design submenu provides designs developed around four EVM types: Fixed Voltage 6A (SLVP183), Adj. Voltage 6A (SLVP192), Fixed Voltage 3A (SLVP204), and Adj. Voltage 3A (SLVP201). This feature saves time when an EVM is used in the development of a product.

The Save Design submenu allows you to save a complete design. This is a very important task to perform and should be done "early and often."

Print menu

The Print menu has four options: All, Inputs, Schematic, and Setup.

The All submenu prints the following information: Schematic, Design Inputs, Worst-Case Stress Analysis, Bill of Materials, Loop Response Graph, and Efficiency Graph.

The Inputs submenu prints the desired specifications, the calculated values, and worst-case stress analysis information.

The Schematic submenu prints the schematic as it is shown on the schematic window.

The Setup submenu triggers a printer setup dialog box.

Edit menu

The Edit menu allows you to select changes to the Input Capacitor, Output Capacitor, Output Inductor, or Max Current Multiplier.

The Input Capacitor, Output Capacitor, and Output Inductor submenus open the appropriate database dialog box so you can select a different component or add, edit, or delete components in the database.

The Max Current Multiplier submenu allows you to select 2X, 3X, 4X, or 5X. This selection limits the rated current that the program looks for when it selects an inductor while in Design for Efficiency mode. If the 5X selection were made (in this mode) with an I_{OUT} input of 6 A, the program would look for an inductor with maximum efficiency but would ignore inductors above a 30-A rating. Since the highest current rating is likely to be the largest, it may select an inductor that is unrealistically large and heavy. For this reason you may want to change the current multiplier to a lower value. This would cause an inductor of a more practical size to be selected.

Analysis menu

The Analysis menu contains the following five options: Specs, Efficiency, Loop Response, Stress, and Bill of Materials.

The Specs submenu displays each of the inputs and the calculated specifications.

The Efficiency and Loop Response submenus cause appropriate graphs to be plotted on-screen.

The Stress submenu displays the Worst-Case Stress Analysis screen.

The Bill of Materials submenu displays a list of all components in the design.

Dual App menu

An application design requiring dual outputs is available by selecting the Dual App menu (see Figure 2 on the next page). The resulting form shows the connections required to implement a dual-output voltage design with synchronized ramp times.

The Core (main) supply is the lower of the two voltages. To use this form, you should design the core supply first, then enter the inputs for the interface between the two outputs on this form. The I/O supply is then designed next. Either a fixed output or variable output controller can be used for the core supply, but a variable-output controller must be used for the I/O controller.

The values for the resistors are calculated when the "Calc" button is clicked.

Format menu

The Format menu allows you to change the background color of the schematic, analysis, bill of material, plot, or stress screens. The Default Colors submenu option sets all the background colors back to the default color.

Help menu

The Help menu contains three submenus: About, Disclaimer, and Help. The About submenu displays information about SWIFT Designer, and the Disclaimer displays the Texas Instruments legal disclaimer. Program help can be obtained by clicking on the Help submenu. A standard Windows Help window is opened, and help topics are available. In addition, clicking on the Index button and selecting the Find tab provides the ability to search.

Smart power buttons

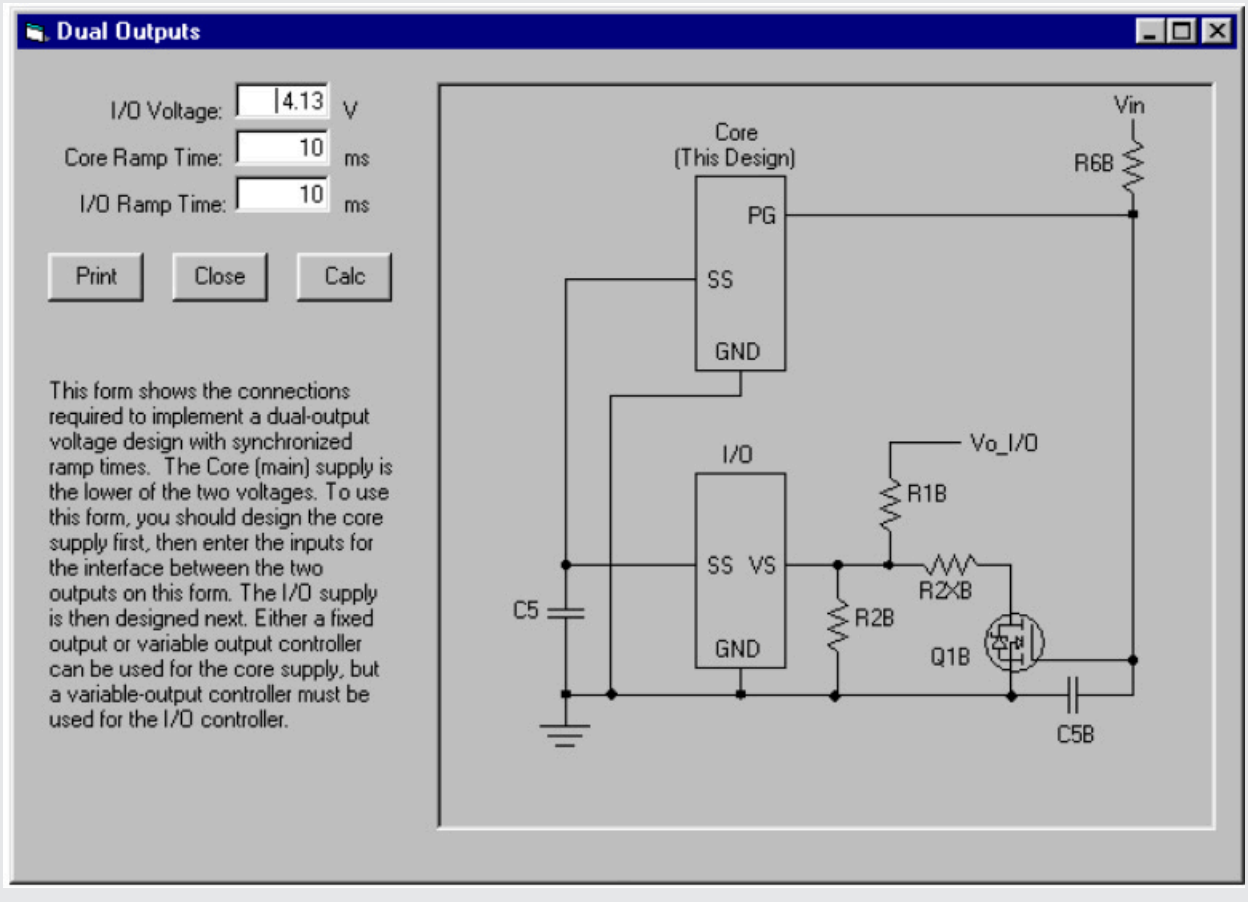
Before you start a design, only selected buttons on the toolbar are available due to lack of current information for the disabled buttons. When you change the input parameters, the same buttons and the component values on the schematic are disabled again to prevent you from viewing invalid data.

Entering a new design

Enter the desired parameters of the new design in the input boxes to the left of the schematic section. All parameters must have a value within the range given in the ToolTip that is displayed when the mouse is stopped over the box. An explanation of the parameter is shown on the status bar at the bottom of the input window. The parameters may have a reduced input limit due to factors in other input boxes that the program determines when you start a design.

Click the "GO" button on the toolbar. This will start the design process and check all input limits for the given conditions. When the design is complete, the values will be displayed on the schematic, and the toolbar options that were grayed out at startup will be enabled and available for use.

Figure 2. Dual-output design



The database

The database is a list of all components available to complete the circuit (Figure 3). You may have different devices available than those in the default database; therefore, you will need to add them.

To add a component to the database, click on the buttons in the schematic; for instance, "C1," which will open the Input Capacitor selection form. (The input capacitor will be used for further examples.) Click on the Add New Capacitor menu to add a line at the bottom for the new component. After adding the desired component, click the "Update" button below the table to update the database, or click the "Cancel" button to abort the addition.

All fields are important in the program; if a component with empty fields is selected, a runtime error may occur. The "Size" field is used by the PCB area subroutine to calculate estimated board area. The "Area" field of each component is the area of a rectangle (in mm^2) that totally encloses the component.

This database is written in Microsoft® Excel 97 format for ease of use. If you modify the database and later want to download the latest Texas Instruments version, you may use Excel to merge the two databases without losing the added components. See Excel Help for additional information on merging the databases.

Important note: The actual files used in SWIFT are record-type binary files (*.bin) that are exported from an Excel file in the proper format for SWIFT Designer to use. Changing the database from within SWIFT will not change the Excel file (but will change the binary files). Editing the Excel file is easier and is recommended. After editing the Excel database, click on the "Save *.Bin" command button in the upper left of each page to save that page's components. The Excel save macro also checks each field to verify that the entry is within parameters before it writes to the binary file. Any error will abort the save macro and take the user to the cell location of the error.

Editing the database

To edit a component in the database, open the desired component selection form, scroll down to the desired component, click on the gray selection button to the left of the item, and click the Edit Highlighted Capacitor menu. After completing the desired changes, click the "Update" button below the table to update the database, or click the "Cancel" button to abort the changes.

Deleting components from the database

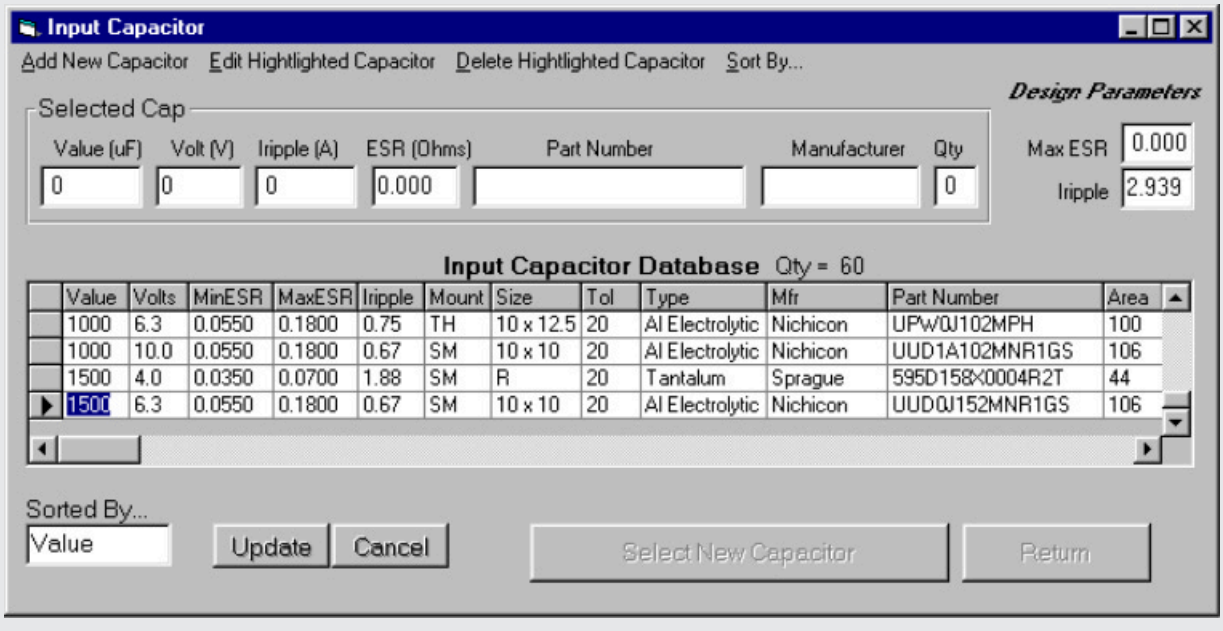
To delete a component from the database, open the desired component selection form, scroll down to the desired component, click on the gray selection button to the left of the item, and click the Delete Highlighted Capacitor menu.

Sorting the database

The Input Capacitor, Output Capacitor, and Output Inductor databases can be sorted from their respective forms by clicking on the Sort By... menu. The Sort By form will open and display the available fields. Any of the fields can be used for sorting, and the chosen field is shown on the component selection form in the lower left corner.

An alternate way to sort is available by clicking on the database table headers on the component selection form. When initially opened, each component selection form will be sorted by value and show all components in the available table, not just components that will work in the current design.

Figure 3. Database form showing capacitors

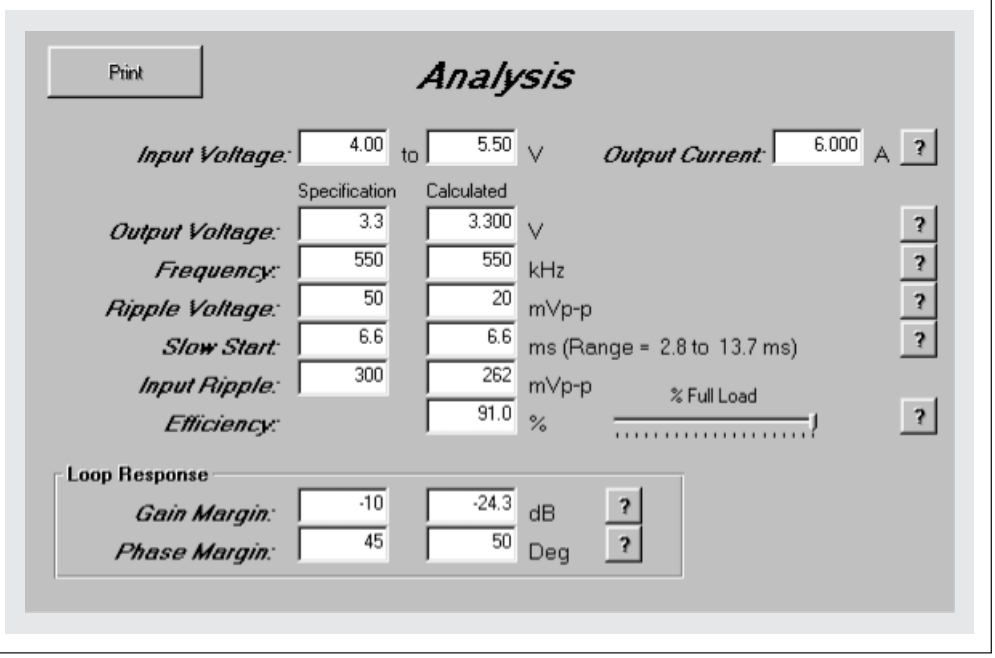


Analysis form

To open the Analysis form, click the "Analysis" button on the toolbar. The Analysis form (Figure 4) shows the specified and calculated parameters of the design. The output voltage will be calculated with 1% resistors when external compensation is used. If the operating frequency is not one of the default values, the actual nominal frequency is shown in the calculated value. Ripple voltage, efficiency, and loop response calculations are shown at full load and nominal input voltage. Efficiency may be viewed at any load value by moving the slider bar to the desired load percentage. Any out-of-spec condition on the Analysis form is highlighted in bold red type and will cause the "Err" LED on the input window to flash.

This form contains multiple help buttons, each with a question mark on it. These buttons may be clicked for additional information.

Figure 4. Analysis form



Application log file

An application log file (applog.txt) is generated each time the program is started. This file logs the steps and subroutines used during the previous run and records all process variables and values. In case of a program error, this log can be used to locate the process that was running at the time of the error. The log also shows why each component in the database (that is not selected) was rejected for the design.

Bill of Materials

The Bill of Materials shows a complete listing of all parts used in the design (Figure 5). Critical components are listed with specific part numbers and descriptions that readily allow you to purchase or substitute the parts.

Non-critical components are listed with only descriptions and sizes. The Bill of Materials is generated from information included in the parts database; therefore, when adding to or editing the database, you should include complete information.

Figure 5. Bill of Materials

11-Apr-01

Bill of Materials

Print

Ref Des	Part Number	Description	Manufacturer	Size
C1	94SV477X06R3F	Capacitor, OSCON, 470-uF, 6.3-V, 20%	Vishay	F12
C2	595D108X0004R2T	Capacitor, Tantalum, 1000.-uF, 4-V, 20%	Sprague	R
C3	Std	Capacitor, Ceramic, 0.01-uF, 16-V, 10%	Std	603
C4	Std	Capacitor, Ceramic, 0.1-uF, 16-V, 10%	Std	603
C5	Std	Capacitor, Ceramic, 3300 pF, 25-V, 10%	Std	603
C6		Not Used		
C7		Not Used		
C8		Not Used		
C9	Std	Capacitor, Ceramic, 0.1-uF, 16-V, 10%	Std	603
L1	CTX10-5-52	Inductor, 10.-uH, 8.7-A, 10-millohms	Coiltronics	CTX10
R1		Not Used		
R2		Not Used		
R3		Not Used		
R4		Not Used		
R5		Not Used		
U1	TPS54616	IC, IFET Controller, 3.3-V, 6-A	TI	PWP28

Bode plot

A Bode Loop Response Graph (Figure 6) is generated to show the closed-loop bandwidth and phase margin for the current design. A detailed review of Bode parameters is beyond the scope of this article; but, in general, the gain response should fall at a 20-dB/decade rate as the curve crosses 0 dB with a crossover frequency that is less than 20% of the switching frequency. The phase should be at least 30° above 0 at the crossover frequency. More bandwidth indicates a faster transient response, while more phase margin indicates less ringing during transients. These two parameters are usually opposed to each other.

Option buttons at the top of the plot area allow you to view worst-case conditions for the Bode plot. When you print this form, the option buttons control the plot that is printed.

A marker function has been added that allows you to scan the plot and verify the gain and phase at any point. To use this function, click on the command button in the lower left labeled “Marker On.” This will enable the marker and place it at the left side of the plot. Click anywhere between the left and right extremes of the graph to move the marker to that location. The frequency, gain, and phase can then be read on the status bar at the bottom of the window. This marker can be used to find the magnitude of the plots that are off the scale of the graph. To disable the marker, click on the same command button that is now labeled “Marker Off.”

The advanced user can get the worst-case loop response with different inductor and capacitor parameters by using the “Characteristics” button in the lower right corner of the plot. This function works only for externally compensated devices and shows the loop characteristics (poles, zeros, gain, etc.) at the given conditions. The plot form will update when the “Recalc” button is clicked. Note that this form does not change the design parameters; all parameters will be reset when this form is closed.

Figure 6. Loop Response Graph

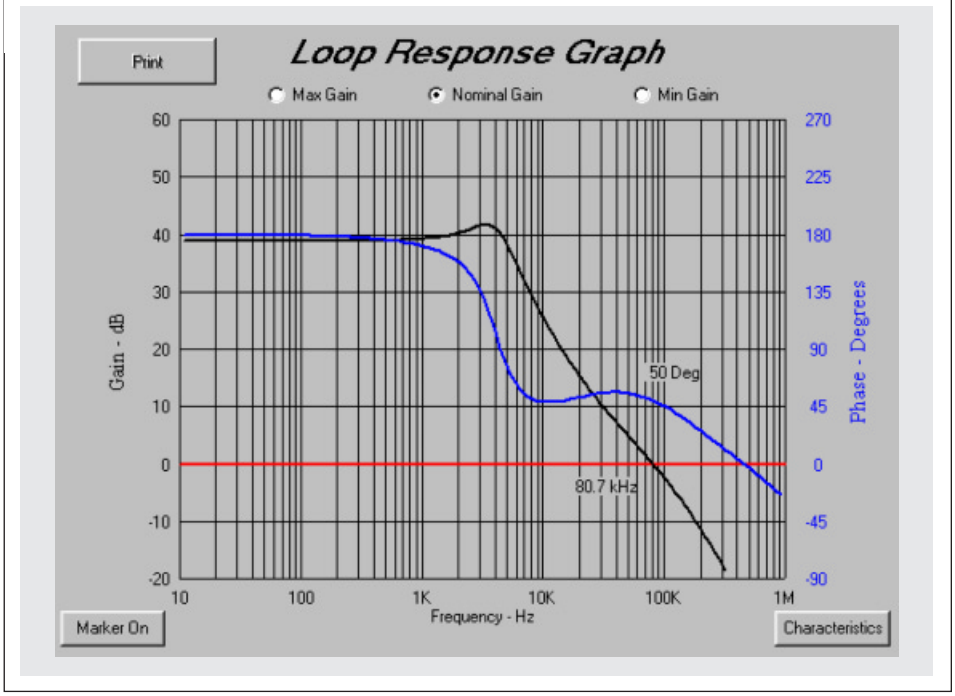
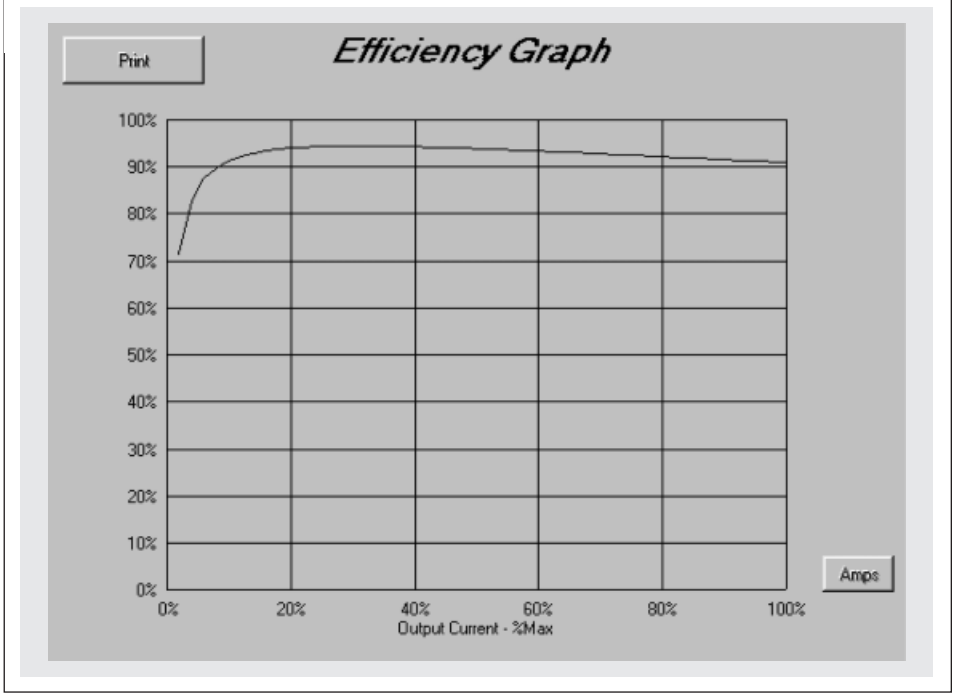


Figure 7. Efficiency Graph



Efficiency Graph

Efficiency is plotted over the full load range and is displayed as a percentage (Figure 7). The x-axis can be viewed as a percentage of full load or in absolute current by clicking the “Amps/Percent” button in the lower righthand corner

of the Efficiency Graph form. Either view shows worst-case efficiency at nominal input voltage using the component parameters in the database. Actual efficiency should be higher under normal conditions.

Estimated PCB area

The estimated PCB area calculation shows a relative size for the current design. You can display this measurement either in square mils (thousandths of an inch) or in square millimeters by clicking the units button under the area box. This calculation is an absolute minimum measurement based upon actual component area (plus 5 mil clearance all around) and a fixed multiplier factor (1.875 × total component area) to allow for connection traces. This method will show the smallest design that can be implemented but may not meet your layout or parameter guidelines. Power dissipation requirements also may require more area for the controller and/or inductor.

Saving a new design

Each design can be saved for reference or future use by clicking File>>Save Design on the menu bar or by clicking the "Diskette" button on the toolbar. A "Save Power Design File" dialog window will open and prompt you for the file's location and name (if the file has not already been named). The default extension for these files is .pdr (power design record). This file will save all design parameters and components used for the current design.

Note that actual design results are saved with parts from the current database. If the database is not the same as the one used for the saved design, redoing the design (clicking "GO" again) may not give the same results. If this is critical, a copy of the current database should be saved with the design file.

Loading a previous design

A previously saved design can be reloaded by clicking File>>Open Design on the menu bar or by clicking the "Load File" button on the toolbar. An "Open Power Design File" dialog window will open and prompt you for the location and name of the file. The default extension for these files is .pdr (power design record). This file will load all design parameters and components used for the saved design.

Overriding the design parameters

When selecting output filter components, you may choose parts that will not work in the current design. The program allows this; however, it will notify you with a message box that all of the design parameters have not been met. This usually indicates that the loop response or ripple voltage is out of tolerance. You should verify that these specifications will be satisfactory for the given application. The "Err" LED on the input window will flash when any of the design parameters is out of tolerance. Additionally, the out-of-tolerance parameters will be highlighted in red on the Analysis or Stress Analysis forms.

Printer setup

A standard Windows Printer Setup window will open when you click Print>>Setup on the menu bar. You can select any of the available printers on the list. The program sets the printer orientation to landscape mode due to the layout of the forms within the program.

Printing a form

Any of the currently viewed forms can be printed individually by clicking the "Print" button on the form. The settings or schematic also may be printed by clicking Print>>Inputs or Print>>Schematic on the menu bar.

Print the complete design

The complete design, including the schematic, loop response, efficiency plot, input parameters and specifications, stress analysis, and bill of materials, can be printed to the current printer in one operation by clicking Print>>All on the menu bar. Another way is to click the "Print Complete Design" button on the toolbar. To print selected forms, see "Printing a form" in the previous paragraph.

Restoring default input parameters

Clicking the "Restore Defaults" button on the toolbar restores the default input parameters. Default values are always reloaded at program start. The range of input values and units allowed for each input is shown in the ToolTip for each input box. A brief explanation of the parameter is shown in the status bar at the bottom of the input window.

Selecting a different controller

After the design has been completed, you can change the controller to any of the controllers listed in the selection box shown in the schematic form over the controller symbol. This box will contain 1, 2, 4 or 5 controllers that will work for this design depending on the parameters selected.

Device numbers ending in "10" indicate an externally compensated controller (requiring external divider resistors and compensation network components). Externally compensated controllers require more parts but can be used for non-standard output voltages and for tailoring the output loop response to specific requirements.

Internally compensated controllers require fewer external components but are limited to preset output voltages and have a limited ability to tailor the output loop response.

Both types of controllers come in 3-A and 6-A versions. The 3-A version comes in a 20-pin TSSOP package, while the 6-A version comes in a 28-pin TSSOP package. For high-efficiency requirements (such as a battery-powered application), you may select the 6-A version instead of the 3-A version on a lower-current design to reduce power switch and commutating switch losses.

Selecting a different input capacitor

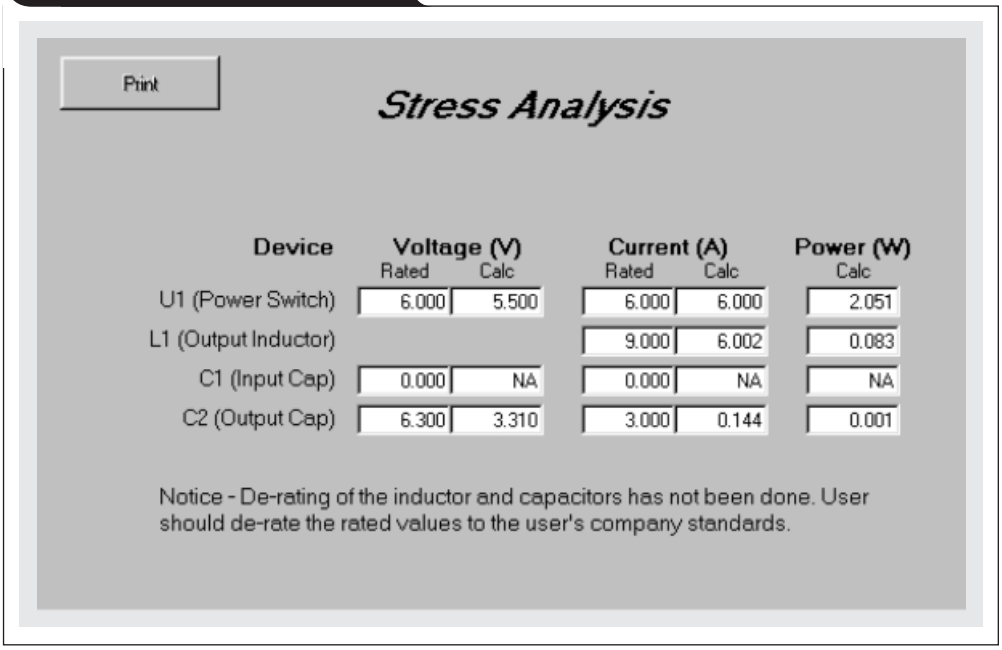
When the Input Capacitor selection form is opened, the input capacitor database will be sorted by value and show all capacitors in the table, not just capacitors that will work in the current design. The currently selected capacitor is shown in the text boxes at the top of the form, and the design parameters used to select the capacitor are shown in the boxes to the right of the current selection. To select a capacitor shown in the table, click on the gray selection button to the left of the desired capacitor and then click the "Select New Capacitor" button. The program will show the required number of the selected capacitors to meet all design parameters and will ask for the desired number of input capacitors to be used in parallel (thus allowing you to use multiple, smaller caps). If the capacitor(s) meet the design requirements, the form will close

automatically and update the schematic. If the desired capacitor is not in the database, it may be added as previously described.

Selecting a different output capacitor

When the Output Capacitor selection form is opened, the output capacitor database will be sorted by value and show all capacitors in the table, not just capacitors that will work in the current design. The currently selected capacitor is shown in the text boxes at the top of the form, and the design parameters used to select the capacitor are shown in the boxes to the right of the current selection. To select a capacitor shown in the table, click on the gray selection button to the left of the desired capacitor and then click the "Select New Capacitor" button. A window will appear that shows the required number of capacitors needed to meet the voltage and current ripple requirements and asks you how many to use. If the capacitor(s) meet the design requirements, the form will close automatically and update the schematic. If the capacitor(s) will not work for the currently selected inductor, you are given the options of letting the program find a compatible inductor, using the capacitor(s) anyway, or canceling the operation. If the desired capacitor is not in the database, it may be added as previously described.

Figure 8. Stress Analysis form



Selecting a different output inductor

When the Output Inductor selection form is opened, the inductor database will be sorted by value and show all inductors in the table, not just inductors that will work in the current design. The currently selected inductor is shown in the text boxes at the top of the form, and the design parameters used to select the inductor are shown in the boxes to the right of the current selection. To select an inductor shown in the table, click on the gray selection button to the left of the desired inductor and then click the "Select New Inductor" button. If the inductor meets the design requirements, the form will close automatically and update the schematic. If it will not work for the currently selected capacitor, you are given the options of letting the program find a compatible capacitor, using the inductor anyway, or canceling the operation. If the desired inductor is not in the database, it may be added as previously described.

Stress Analysis form

The Stress Analysis form (Figure 8) shows the worst-case voltage, current, and power stresses applied to the major components for the current design. These stresses can be used to verify the safety and quality standards for the selected components. Any out-of-spec condition on the Stress Analysis form is highlighted in bold red type and causes the "Err" LED on the input window to flash. Note that all specifications given in this form are maximum ratings with no de-rating.

Conclusion

A novice or an experienced designer can produce single-output, step-down converter designs with ease using the SWIFT Designer power supply design program. Multiple optimization and override features can be used to generate a complete design that best uses available components and satisfies the designer's desires and need for differentiation. This solution comes complete with save, load, and print capability.

SWIFT Designer steps you through the entire (external) component selection process and analyzes the power supply design. The program supports both internally and externally compensated versions to quickly achieve high-performance power supply designs.

Reference

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. SWIFT Designer Install Instructions	.slvc002

Related Web sites

www.ti.com/sc/analogmsp
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with TPS54310, TPS54610, TPS54611 or TPS54672

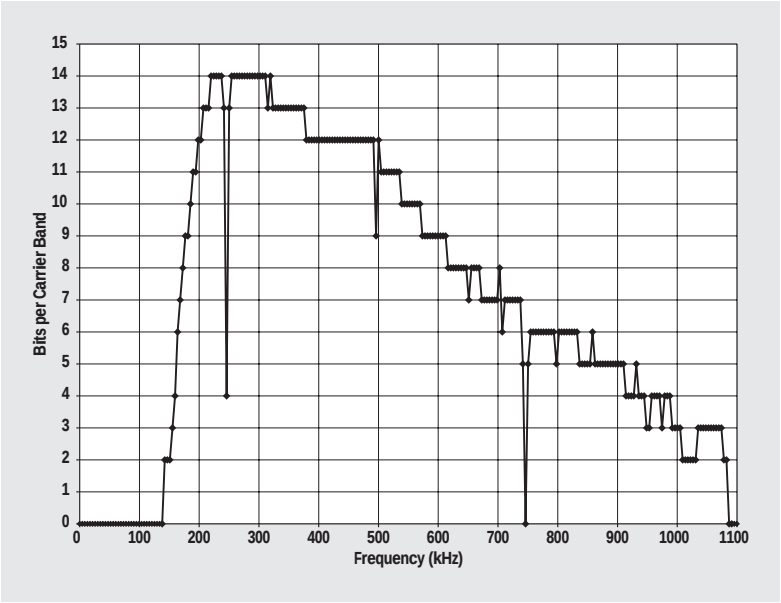
Optimizing the switching frequency of ADSL power supplies

By John Betten, *Applications Engineer, Member Group Technical Staff,*
and Michael Day, *Applications Manager, Portable Power Products*

Introduction

DSL modems send their signals through a twisted-pair telephone line. As the length of this copper line increases, the high-frequency signal becomes attenuated. The modem bit rate starts decreasing after just a few thousand feet. It continues to decrease with loop length, out to a maximum loop length of about 3 miles, where the connection becomes marginal. Data rates as high as 8 Mb/s are achievable with short loops but drop off to around 100 kb/s with the longest loops. As the line length exceeds 3 miles, the bandwidth decreases and data throughput drops off quickly. Transmission signal attenuation of 80 to 90 dB is possible at these line lengths, forcing the modem to implement noise reduction techniques that produce high signal-to-noise ratios (SNRs), minimize crosstalk and interference, and have large dynamic signal ranges. The SNR measurement of the modem has a trough at the power supply's switching frequency. This trough negatively affects the modem's performance by reducing the number of data bits transmitted, thereby reducing the modem's overall data transfer rate. If attention is not given to the power-supply noise, modem performance suffers and customers are forced to accept a lower data transmission rate.

Figure 1. 250-kHz power-supply frequency and its harmonics reduce bit rate throughput



An ADSL modem uses a 25-kHz to 1.1-MHz frequency spectrum for data transmission. The downstream direction (server to client) uses the 138-kHz to 1.1-MHz band. The upstream direction (client to server) uses the 25-kHz to 138-kHz band. The modem divides this spectrum into 256 equally spaced carrier bands, or "bins," each having a 4.3125-kHz bandwidth. The carrier bands are allocated to voice transmission, upstream and downstream data, and buffer zones. The number of bits assigned to each carrier band depends on the level of noise and interference present. Figure 1 shows how the switching noise from a power supply affects the number of data bits per carrier band on an ADSL client modem. An 80-mV_{pp}, 250-kHz square wave imposed on the 3.3-Vdc voltage significantly reduces the available bits at the 250-kHz carrier band, its 750-kHz harmonic, and to a lesser extent the 500-kHz harmonic (due to distortion present on the square wave signal). The harmonics of a square wave follow a sin(x)/x function, which has peaks at multiples of the odd harmonics. The data in Figure 1 represents 11,000 ft of transmission line length.

Table 1 shows the reduction in the overall modem bit rate versus power-supply switching frequency and ripple amplitudes. The data shows that both the amplitude and the frequency of the ripple affect the overall modem data rate. Increasing the ripple voltage amplitude reduces the overall modem data rate. The increase in ripple reduces the SNR in the carrier bands corresponding to the ripple frequency and its harmonics, which lowers transmission rate in the affected bands. Higher power-supply switching frequencies have less effect on the overall modem

Table 1. Power-supply ripple voltage reduces ADSL modem data rate

INJECTED SQUARE WAVE AMPLITUDE (mV_{pp})	DATA TRANSFER RATE			
	100-kHz POWER-SUPPLY SWITCHING (Mb/s)	250-kHz POWER-SUPPLY SWITCHING (Mb/s)	500-kHz POWER-SUPPLY SWITCHING (Mb/s)	1-MHz POWER-SUPPLY SWITCHING (Mb/s)
2	6.8	6.8	6.8	6.8
10	6.7	6.7	6.7	6.7
20	6.5	6.6	6.7	6.7
60	6.4	6.5	6.6	6.6
80	6.2	6.3	6.5	6.6

data rate for two reasons. First, higher switching frequencies affect higher-frequency "bins," which already have lower bit rates. Second, the harmonics are spaced farther apart so that fewer "bins" are affected. Power-supply switching frequencies greater than 1.1 MHz typically have minimal or no impact on the modem data rate because the fundamental of the switching frequency is above the frequencies used to transmit data. Reducing the switching frequency below 100 kHz will move the fundamental below the first downstream modem carrier band; however, the harmonics will affect many carrier bands up to 1.1 MHz.

The effects of switching frequency

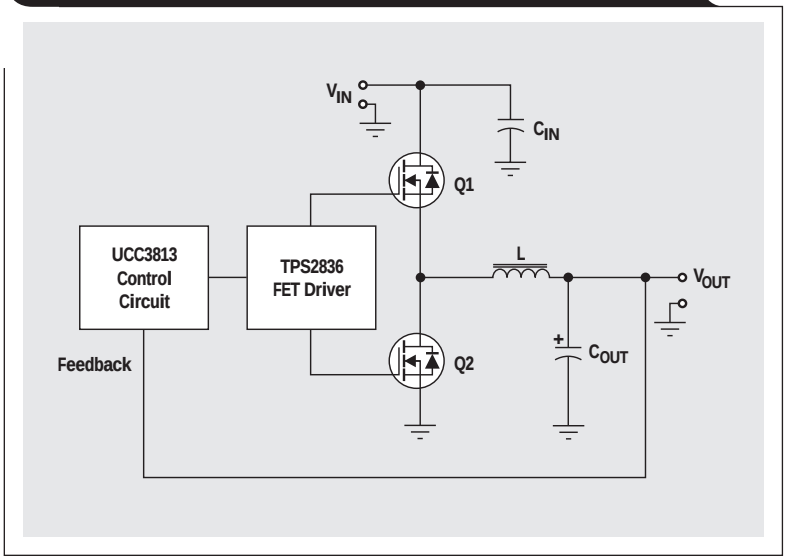
Based on throughput only, a power-supply switching frequency greater than 1 MHz is desirable. However, there are other power-supply factors that are affected by the switching frequency. Some of these factors include overall supply cost, size, efficiency, and reliability. None of these factors can be optimized independently of the others; and, in many cases, optimizing only one supply parameter leads to a less than optimal overall solution.

A typical power-supply requirement for the client modem core consists of a 3.3-V at 3.6-A output that is generated from an input voltage ranging from 10 to 14 V. Figure 2 shows a simple block diagram for a synchronous buck topology that is easily implemented using a Texas Instruments UCC3813 controller with a TPS2836 synchronous buck MOSFET driver. The supply was operated at 100 kHz, 250 kHz, 500 kHz, and 1 MHz. The output ripple of the supply was adjusted at each switching frequency to keep a constant data transfer rate of 6.7 Mb/s, per Table 1.

Increasing the switching frequency of an ADSL power supply reduces the overall volume for two reasons: smaller passives and higher allowable ripple. Table 1 shows that lower switching frequencies require a lower output ripple to maintain a data rate of 6.7 Mb/s. For example, at 100 kHz, the allowable ripple for 6.7 Mb/s is 10 mV_{pp}; while at 1 MHz, the allowable ripple is 80 mV_{pp}. Power-supply filter components are inversely proportional to switching frequency. Not only is more filtering needed at lower frequencies, but filtering a lower-frequency signal requires larger components. The 100-kHz circuit requires a 22-µH inductor, while the 1-MHz circuit requires only a 2.2-µH inductor. Inductor volume is proportional to inductor value; therefore, the 100-kHz inductor is significantly larger than the 1-MHz inductor. The decrease of inductor volume with size is not linear. At some point, an additional increase in switching frequency does not significantly decrease the inductor volume. As the inductor becomes smaller, the packaging and solder pads take up an increasing percentage of overall volume, thereby diminishing the reduction in inductor volume with increasing frequency. Shielded inductors with closed flux paths are preferred to "open" bobbin-type cores. These closed-core structures contain or hold most of the flux lines within the magnetic material, which prevents it from coupling into nearby components and etch. The flux field is highest near the gap of the inductor, so care must be taken during layout to keep sensitive and high-impedance circuits away from it. Shielded inductors have current ratings that are approximately 25% less than the non-shielded variety, due to the additional core volume and the smaller-gauge wire that must be used.

The minimum input and output capacitance requirements are also inversely proportional to frequency. As the frequency increases, the required filtering is reduced; so smaller capacitance values are required. At lower frequencies, ceramic capacitors do not have the bulk capacitance necessary for the required filtering; therefore, aluminum electrolytic, organic electrolytic, or specialty polymer capacitors are used. Because these capacitors are ESR and ripple current limited, their volume varies little with switching frequency. Around 500 kHz and above, ceramic capacitors become a viable option. Ceramic capacitors have very low ESR; therefore, they are capacitance limited. As the switching frequency increases, the amount of charge per cycle delivered by the capacitors is reduced. The capacitance values are determined by the charge requirements; therefore, the capacitance requirements decrease

Figure 2. Simplified synchronous buck block diagram



as frequency increases. As with inductors, the packaging issues diminish the reduction in capacitor volume as switching frequency is increased. While power-supply filter component areas are reduced with increasing frequency, the control circuitry area stays constant. Figure 3 shows the overall power-supply area as well as the breakdown of area between the control circuit and the filter. Note that the total area is reduced by about 23% when going from 100 kHz to 250 kHz but is reduced by only 13% when going from 250 kHz to 500 kHz.

Switching frequency has a direct impact on power-supply efficiency. The main power-loss component in a power supply is typically in the power FETs. Power FET losses are comprised of several different terms, some being frequency-dependent and some not. Conduction losses in the FET are independent of frequency. This loss term is a function of power-supply current and FET resistance. FET losses that are directly proportional to frequency include gate drive, Coss, reverse recovery, body diode conduction, and switching losses. Each of these terms dissipates a fixed amount of energy each time the power supply completes a switching cycle. The more times per second the power supply switches, the more power is dissipated by these frequency-dependent loss components. At lower frequencies, FET conduction losses dominate. At higher frequencies, the conduction losses remain constant; while the frequency-dependent losses increase. At maximum output power, the fixed losses in the power supply are 892 mW at both 100 kHz and 1 MHz. The frequency-dependent losses are 165 mW at 100 kHz but increase to 1650 mW at 1 MHz. Figure 4 shows a graph of efficiency versus load and switching frequency.

Figure 3. Power-supply area vs. switching frequency

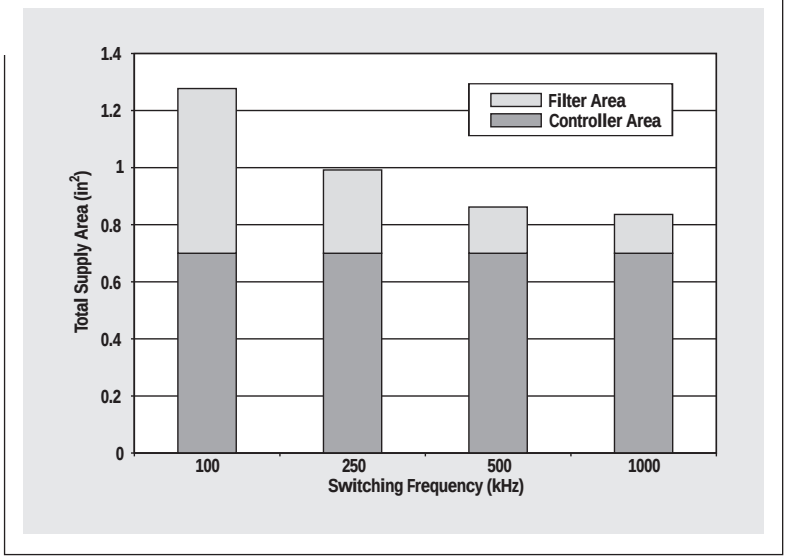
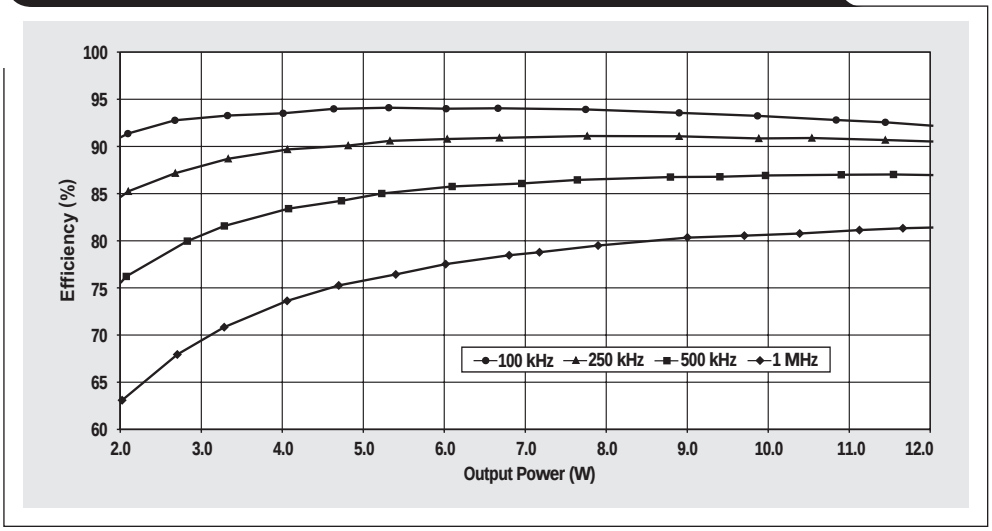


Figure 4. Higher switching frequencies result in lower efficiency



Power-supply reliability and cost are indirectly related to switching frequency. Reduced efficiency at higher switching frequencies translates into higher operating temperatures. Failure rate for semiconductors doubles for every 10°C rise in temperature. An estimate of temperature rise above ambient is shown in Figure 5. The data in Figure 5 assumes natural convection cooling with the board area shown in Figure 3. The designer has a few options to maintain a reasonable temperature rise for the higher switching frequencies. One is to increase the available area for cooling. This may include using either larger or multiple components in parallel in conjunction with a larger PWB to help spread the heat. For example, replacing one SO-8 package with two SO-8s or a D-Pak can significantly reduce junction temperatures. Another option is to provide additional cooling in the form of fans, heat sinks, or both. Both options increase the overall cost and size of the supply. The power supply shown in Figures 6 and 7 has over 2.5 in^2 of surface area; therefore, it runs with a temperature rise of only 45°C at 1 MHz and maximum load.

Figure 5. Power-supply temperature increases rapidly with frequency

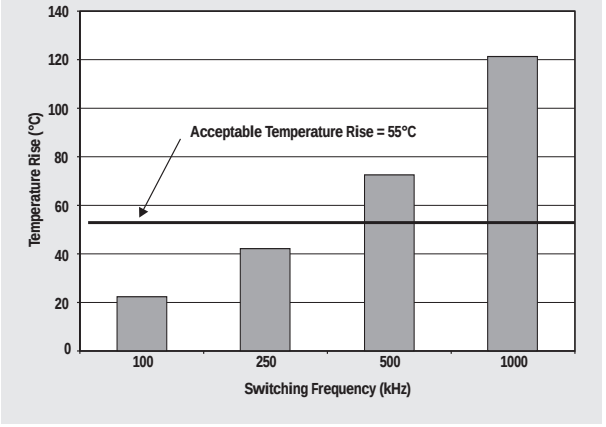
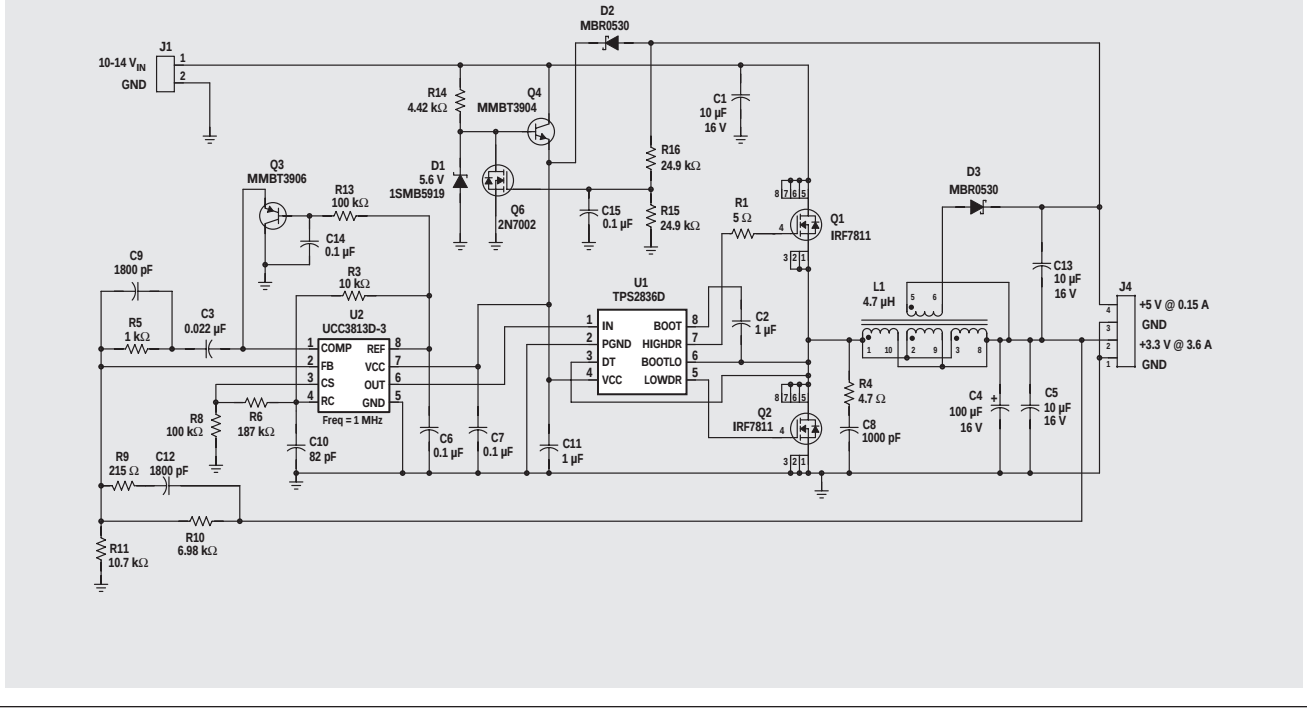


Figure 6. Complete ADSL power-supply schematic (with aux output)



Conclusion

Figure 8 summarizes the trade-offs between switching frequency versus ripple, size, and efficiency while maintaining a constant modem throughput. It may be tempting to try to optimize a particular power-supply parameter, but Figure 8 shows that changing one parameter may negatively impact the other parameters. The power-supply designer must act as a system engineer at the power-supply level, taking into account all design parameters to produce the optimal solution. If minimum area is a concern, the designer may choose a switching frequency around 500 kHz. At 500 kHz, the power-supply area is minimal due to the decreased sensitivity of the modem to switching noise; and the efficiency is still at an acceptable level. If minimum losses are the driving factor due to limited cooling or input-power constraints, the supply should be run somewhere between 200 kHz and 300 kHz. Within that range, frequency-dependent losses are minimized and the power-supply efficiency is near its maximum level; however, the volume is increased due to the additional filtering required to maintain an acceptable modem throughput.

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Dallas TX 75243

Related Web sites

www.ti.com/sc/device/TPS2836
www.ti.com/sc/device/UCC3813-1

Figure 7. Dual-output (3.3-V/5-V) circuit operates at 1 MHz

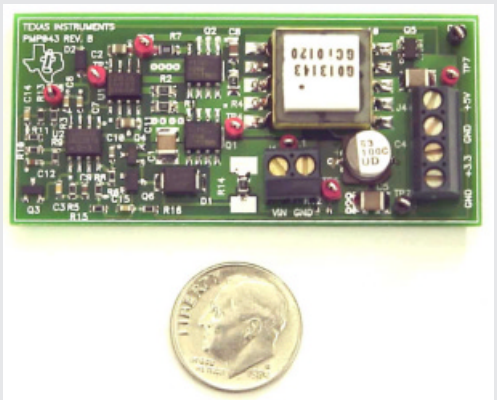
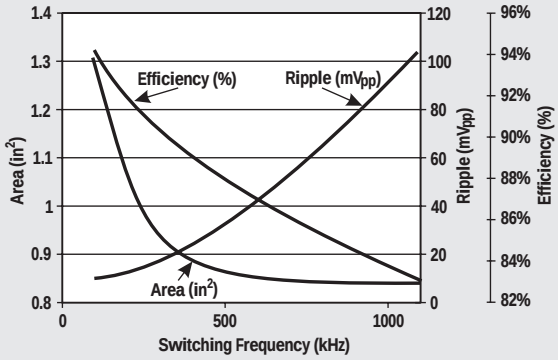


Figure 8. Trade-offs for a constant modem throughput



Powering electronics from the USB port

By Robert Kollman, *Senior Applications Manager, Power Management, DMTS,*
and John Betten, *Applications Engineer, Member Group Technical Staff*

Introduction

The USB interface can provide power to low-power peripherals but must adhere to the USB 2.0 specification (Reference 1). Table 1 provides an overview of the requirements placed on the peripheral equipment. The host equipment provides a 5-V supply capable of, in the worst case, only 2.25 W of power. In some cases, this is clearly not enough for the peripheral, and an alternate power source such as a wall adapter or off-line power supply is used. In other cases, 2.25 W is much more than is needed; and low-cost, linear regulators can be used to generate the supply voltages for the peripherals. However, in many cases this power limit necessitates the use of higher-efficiency power-supply designs and complicates the system trade-offs of cost, efficiency, and size. This article discusses these issues.

Table 1. USB power requirements at a glance

PARAMETER		REQUIREMENT
Voltage	Low-power device	4.4 to 5.25 V
	High-power device	4.75 to 5.25 V at upstream connector
Maximum quiescent current	Low-power device	500 µA
Maximum low-power current		100 mA
Maximum high-power current		500 mA
Maximum power draw		2.25 W
Maximum input capacitor		10 µF
Maximum inrush		50 µC

Another unique requirement of the USB power interface is the different current draws allowed. When a device is first connected to the USB, its bypass capacitor could be charged abruptly and create a glitch on the host equipment supply. The USB specification resolves this problem by limiting the initial power surge in two ways. The peripheral device is allowed only a small (<10-µF) bypass capacitor, and the charge drawn from the bus is limited to 50 µC over a specified time. Larger capacitors can be used if inrush limiting is provided. Once the USB is connected, there are further limits on current draw. The host first recognizes the peripheral as low-power, allowing it to draw less than 100 mA of current. The peripheral can ask the host to recognize it as a high-power device in a process called "enumeration." Once enumeration is completed and permission is granted, the allowed peripheral current is increased to 500 mA. The USB spec also includes a suspend mode that supports remote wake-up. This mode limits quiescent current to a total of 500 µA for a low-power device and 2.5 mA for a high-power device. It often requires the use of switches to power down portions of the peripheral's electronics.

The USB 1.0 specification has been active since its release in November 1995. Products that were delivered to the 1.0 specification had no official logo associated with them. Many times the products did not fully meet the current-limit requirements, which usually was not a problem with the product connected to a PC. However, problems did arise when there were multiple products connected in a hub arrangement. With the release of the 2.0 specification, certified products will be marked with a logo. The certification promises to be more rigorous, and designers should expect to meet the requirements of the new specification.

Inrush limit and power segmentation

There are two possible configurations for USB products—a single peripheral connected directly to a host, or a set of peripherals connected through hubs to the host. For a single peripheral, the current-limiting requirements usually are not an issue unless a large input capacitor is placed across the power-supply voltage for hold-up. If hubs are used, current limiting will definitely be required due to the unknown nature of the peripherals that will be plugged into the hub.

The current limits can be implemented in two manners, one using discrete power devices with external control circuits, and the other with the switches integrated into the controllers. In higher-power applications, the discrete approach usually yields a lower-cost solution. However, in lower-power applications, an integrated approach is very attractive. With the low voltages and currents involved in the USB, a number of manufacturers are developing ICs specifically targeted for these markets. Figure 1 on the next page presents a typical circuit. The first output is an adjustable linear regulator that can be configured for 0.9- to 3.3-V output, which powers the hub controller and other electronics. The second is a switched output that powers the peripherals connected to the hub. The integrated approach provides a number of desirable features. The device is much more rugged than a discrete approach because a thermal limit monitors the pass-element temperature and shuts down if an over-temperature is detected. Two-level current limiting is provided in the switch to prevent glitching of the host power bus. Initial power-up current is limited to 100 mA until the output reaches 93% of the input voltage; then, once the USB controller is enumerated, the current limit is raised to 500 mA, typical of the high-power peripherals.

Figure 1. Internal switch power segmentation and limiting

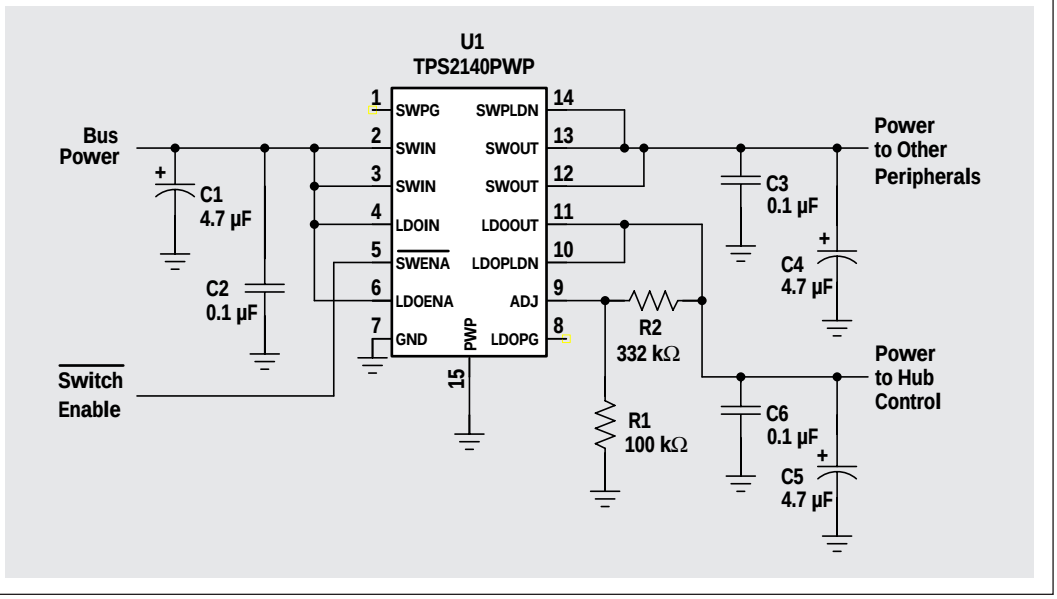


Table 2. Power-management options

POWER MANAGER IMPLEMENTATION	SWITCH RESISTANCE (mΩ)	CIRCUIT AREA (in^2)	OVER-TEMPERATURE PROTECTION	OVERALL RELATIVE COST (%)
Internal switch	100	0.30	Yes	80
External switch	50	0.5	No	100

Table 2 compares the two approaches, internal versus external switches or pass elements. The pass elements have higher resistance in the internal switch approach, which occupies less than 60% of the external switch approach. However, the silicon die area is more costly in the internal switch because more mask levels are involved in the IC's device structure than in a simple MOSFET. Typically, the IC will use over 20 mask levels compared with 8–10 levels of the MOSFET. The higher level of integration eliminates at least two semiconductor packages and the resulting poor interconnect efficiency. In addition, the higher level of integration provides a higher reliability as bond wires and solder joints are eliminated. Reliability is further enhanced with the over-temperature protection of the internal switch. With the external switch, there is no cost-effective method to measure MOSFET temperature to protect it from shorted loads. Current foldback and power cycling techniques can help but do not provide the robustness of the thermal shutdown. The last column of the table presents a cost comparison between the two approaches. The costs are almost the same and would bear a closer examination on a particular requirement. Generally, the reason the costs are so close is that the external switch approach uses multiple semiconductor packages compared with the single package of the integrated switch. Each of the packages has its own overhead of assembly and test, making the overall system-level costs about equivalent.

Powering low-voltage digital electronics

Generating low voltages, such as 3.3 V, from the USB can be done in several ways. Regardless of the configuration used, the output current for a 3.3-V output is limited to 0.65 A (assuming 95% efficiency) due to the 2.25-W input power limitation. The options to provide these lower voltages include linear regulators, switching power supplies, and charge pumps. Within switching power supplies, there are two further subgroups, synchronous and conventional. The synchronous is more efficient and costly and will be used to get as much power from the USB as possible.

The linear regulator is the lowest-cost and highest-density option for generating lower voltages from the 5-V USB. When there is no power issue, it will be the circuit of choice. However, when power becomes an issue, switching regulators can more efficiently power the

peripheral. Figure 2 shows one of the lowest-cost buck switching regulator options available. In this circuit, the switching of the FET, Q2, is controlled to "buck" the average voltage presented to the output filter, which then smooths the switching waveform. The drawback of this circuit is that the lack of controller integration requires an external FET and drive circuit, which makes the circuit relatively large. An external FET provides flexibility in the design, allowing lower on resistance devices to be used compared with integrated FET controllers, and possibly achieving greater efficiency.

In Figure 2, a large percentage of the overall power loss is dissipated in the freewheeling diode D2. In Figure 3 this diode is replaced with an N-channel FET, making this circuit a synchronous buck converter, which significantly improves the converter efficiency. Efficiency improvements

Figure 2. Low-cost, non-synchronous buck regulator

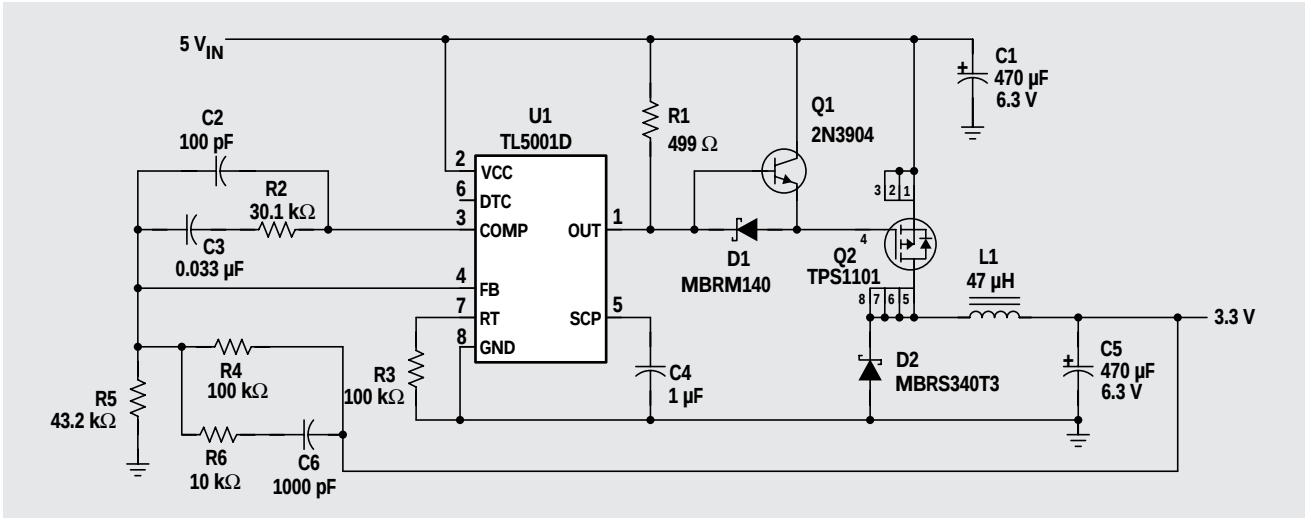


Figure 3. External-switch synchronous buck regulator

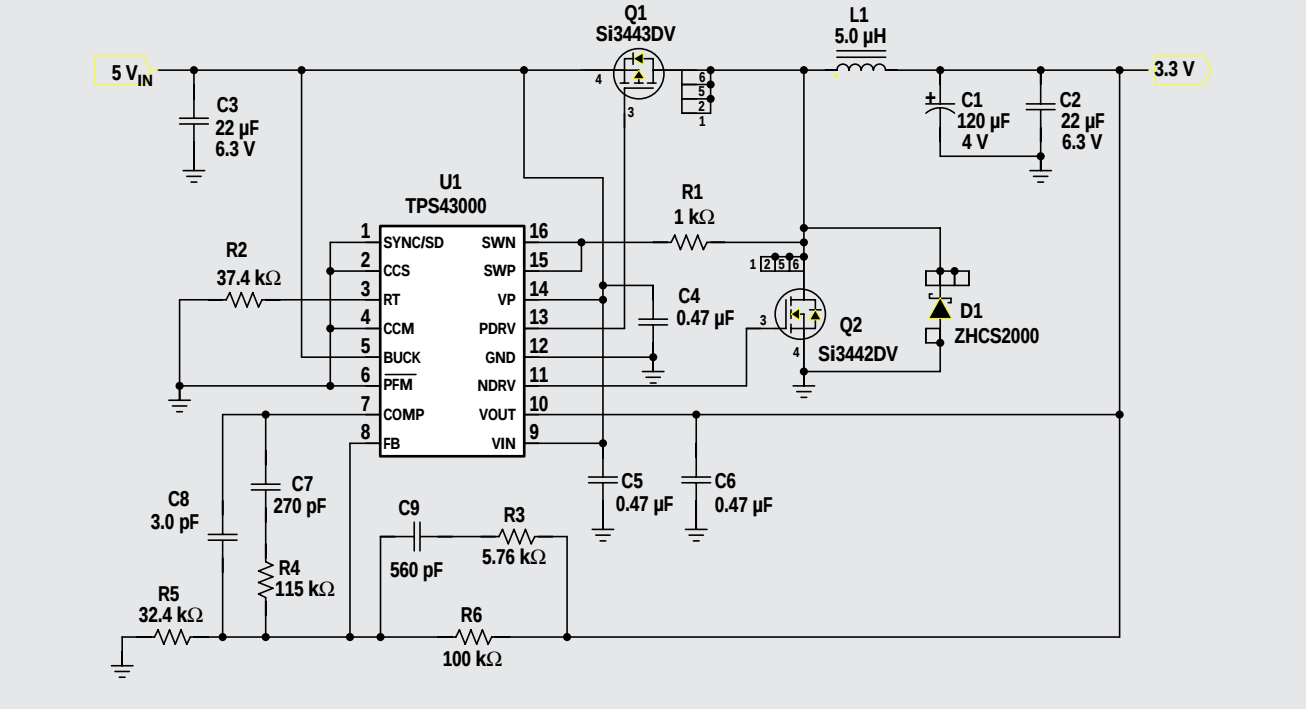


Figure 4. Step-down charge pump

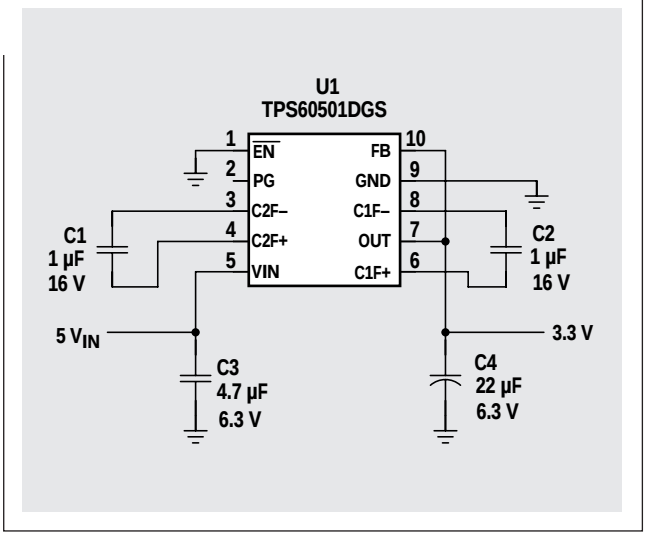
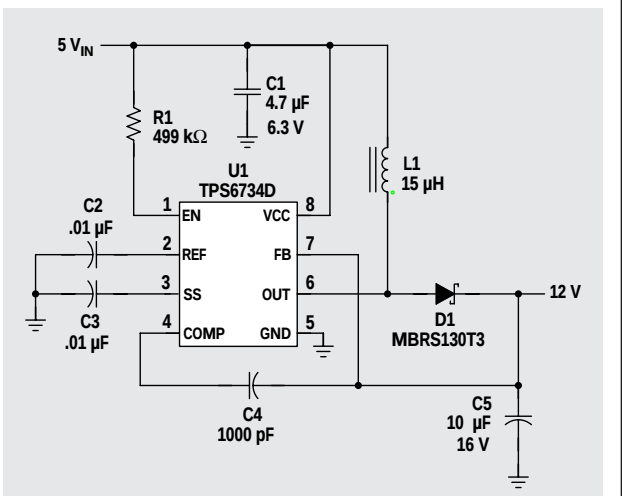


Figure 5. Boost regulator



can be realized over a wide load range with this circuit. At very light loads, pulse skipping can decrease gate-drive losses. When the output voltage drops 2% below the nominal voltage set point, the converter senses it and switches until the output reaches an upper threshold; it then puts itself in sleep mode until the load discharges the output capacitor to the lower threshold again. This circuit provides excellent efficiency but is more costly than the one in Figure 2. Its circuit area is also slightly smaller, mainly because the controller can operate at frequencies of up to 1 MHz, which allows the inductor and input/output capacitors to be noticeably smaller.

Integrating the top FET, bottom FET, drive circuit, and feedback compensation into the controller provides for a small, integrated, and efficient converter solution. This is becoming a very popular solution because it is generally simple to design and has a very short design cycle time. Software is available that aids in the design, making it possible for novices to design power supplies. Controllers such as the TPS5431x and TPS5461x SWIFT™ series provide such integration, but their cost is higher due to the added performance and features.

Circuit area is often a critical design parameter. The step-down charge pump in Figure 4 represents an extremely small solution. Four ceramic capacitors and the charge pump controller are the only components required for this solution. The controller utilizes internal FETs that connect two flying capacitors in various series or parallel configurations, dumping their energy to the output. The input voltage and the load are used to set the internal FET configuration automatically. At loads heavier than 150 mA, the controller acts as an LDO and stops using the switched capacitors altogether. Output current is limited to a maximum of 0.25 A, which limits this circuit to low-power applications. Efficiency is between 80 and 90% for light loads between 1 mA and 50 mA, but drops off to approximately 65% above that when operating in LDO mode. The cost of Figure 4 is one of the lowest, due to the low cost of the ceramic capacitors.

Table 3 provides a summary of the low-voltage step-down options discussed. Efficiency, cost, and circuit area are also listed for reference. So what's the right choice? Linear regulators, when you can afford the losses. Then take a look at charge pumps and determine their losses based on conversion ratios. Finally, evaluate non-synchronous and then synchronous regulators. In each case, the system cost and size increase, but more power is available for the load. A second trade-off in the switching power supplies involves deciding between internal and external FETs. The cost is usually lowest with external FETs; while the design time, component count, and size will be smaller with internal FETs.

Table 3. Low-voltage (5-V to 3.3-V) regulator options

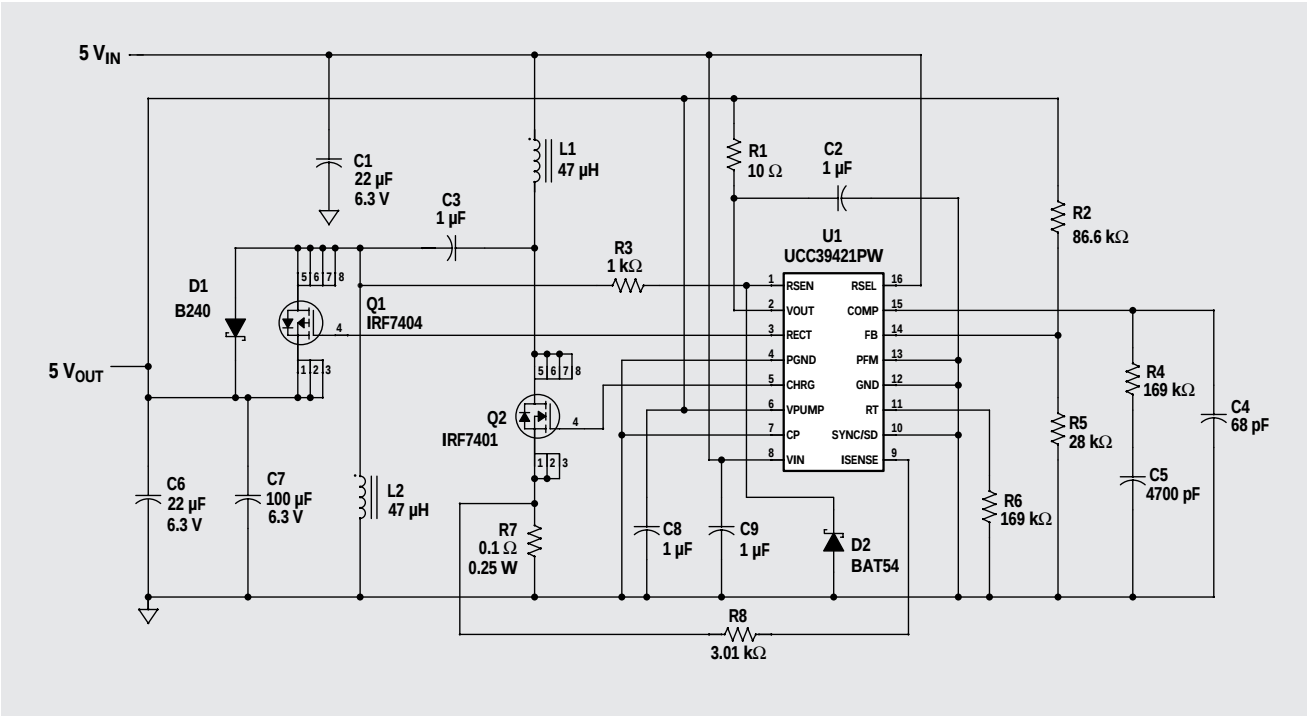
TOPOLOGY	INTERNAL SWITCH	TYPICAL EFFICIENCY (%)	OVERALL RELATIVE COST (%)	AREA (in^2)
Linear	Y	66	40	0.1
Non-synchronous buck	N	87	100	1.2
Non-synchronous buck	Y	85	150	1.1
Synchronous buck	N	96	200	1.0
Synchronous buck	Y	95	250	0.7
Charge pump*	Y	60 to 90	70	0.15

*Current is limited to 0.25 A, and efficiency is largely dependent on input voltage.

Powering higher-voltage analog

Higher-legacy voltages, such as 5 V and 12 V, are often required to power analog circuits. The loading on these outputs is typically not as heavy as on their digital voltage counterparts—usually less than 100 mA. The circuit in Figure 5 is a boost regulator that provides 12 V and will provide up to 120 mA while operating over the 5-V USB output voltage range. In this

Figure 6. Synchronous SEPIC converter



design, the FET is integrated into the controller along with the feedback resistor network, reducing total parts count to a minimum. A drawback to this approach is that the circuit block provides no current limit. If the 12-V output is shorted to ground, there is nothing in the V_{IN}, L1, D1 path to limit current.

An alternative topology, the SEPIC, can overcome this shortcoming. Also, the SEPIC conversion ratio extends above and below the input voltage as compared with the boost, whose ratio just includes voltage greater than V_{IN}. Since the USB voltage can range from 4.5 V to 5.5 V, the SEPIC converter in Figure 6 makes an excellent choice for a 5-V output. This SEPIC uses a synchronous rectifier Q1 to reduce the losses in the output diode and improve efficiency by several percent. Diode D1 conducts only during the on/off transitions of Q1 to prevent the intrinsic diode of Q1 from conducting. Additional benefits include low-input ripple currents and inherent current limiting. On the negative side, the addition of the dc blocking capacitor C3 is required. Since the blocking capacitor and output capacitors must handle large pulsing currents, they require a high RMS ripple-current rating and a low ESR to minimize the output ripple voltage. Ceramic capacitors are usually chosen due to their high ripple-current rating and low cost.

Figure 7. Synchronous buck converter with auxiliary output winding

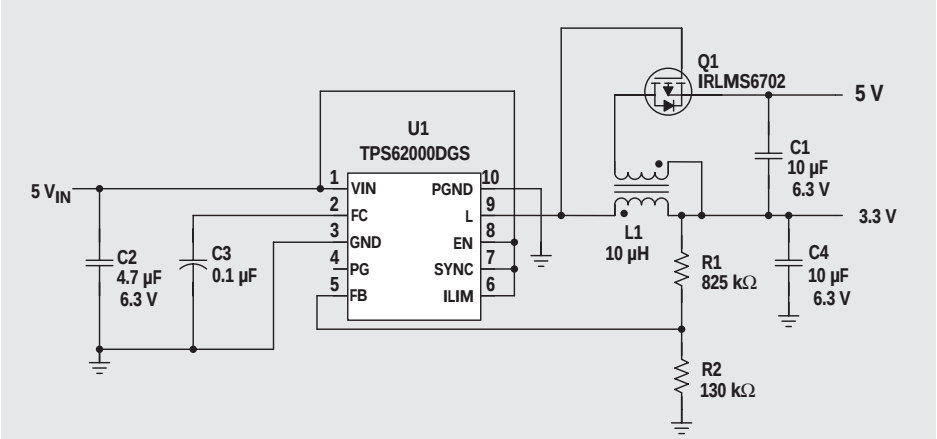


Figure 7 shows an option for providing dual-output voltages from a single synchronous buck converter. When the bottom-side FET (internal to TPS62000) conducts, FET Q1 turns on, and output cap C1 charges with an additional voltage developed across the secondary of L1. The level of the auxiliary voltage is determined by the turns ratio

Table 4. Higher-voltage regulator options

TOPOLOGY	INTERNAL SWITCH	CURRENT LIMIT	TYPICAL EFFICIENCY (%)	OVERALL RELATIVE COST (%)	AREA (in^2)
5-V to 12-V boost	N	N	86	280	0.7
5-V to 12-V boost	Y	N	85	320	0.6
5-V to 5-V SEPIC*	N	Y	89	560	1.0
5-V to 5-V SEPIC	Y	Y	85	550	0.9
3.3-V to 5-V charge pump**	Y	Y	65 to 75	200	0.2
Sync buck w/aux winding†	Y-Sync buck N-Aux	Y	95	100	0.3

* Synchronous operation
** TPS60133 charge pump controller, 0.3-A maximum output current
† Cost and area of auxiliary output only

between the two windings of L1. The voltage across C1 is stacked on the 3.3-V regulated output; so, for a 5-V auxiliary output, an additional 1.7 V needs to be developed across L1's secondary. A turns ratio of 2:1 will work well in this application. For low current levels, the voltage drops developed across the internal bottom FET and Q1 (which turn on in phase with each other) are small and often cancel each other out. These FET drops may not significantly add to the output-voltage tolerance error, and good regulation can be achieved.

Table 4 presents a comparison of some of the options for generating higher voltages for analog loads. Here again, the decision involves a trade-off between cost, performance, and loss. If power is not a problem, the first choice to consider is a charge pump. When loss becomes an issue, a switching regulator may become warranted. The first circuit to consider, particularly if a buck regulator is being used, is the auxiliary winding scheme of Figure 7. It adds minimal cost and degrades efficiency the least. Next come the SEPIC and boost regulator. The need for short-circuit protection will determine which approach will be favored. Usually a boost will be chosen for its higher efficiency if current limiting is not needed or can be accommodated elsewhere in the system. There are also trade-offs in synchronous and non-synchronous operation, as well as in an internal versus external switch, as in the buck regulator.

USB-powered DSL modem power supply example

The circuit in Figure 8 (next page) is an example of a complete USB power supply with 3.3-V, 5-V, and 12-V outputs. With the 3.3-V powered at 0.32 A, the 5-V at 0.05 A, and the 12-V at 0.05 A, the overall efficiency is 89.5%, which allows the input power to remain below the 2.25-W maximum limit. In operation, only the 3.3-V output is allowed to power up at turn-on, with the 5-V and 12-V enable pins being held low by the bus controller. No more than 100 mA is drawn off the 3.3-V output during power-up in low-power mode. Enumeration then comes from the bus controller to allow the 5-V and 12-V to power up. A boost topology was used for both the 5-V and 12-V outputs, with the 5-V power stage input powered from the 3.3-V output. The controller chosen for both boost regulators was the low-cost TL1451A dual controller. The approach taken for this design example is geared toward low cost and high efficiency rather than small area. Figure 9 shows a photograph of the completed hardware, which measures 1.5" × 2".

Figure 9. DSL modem power supply

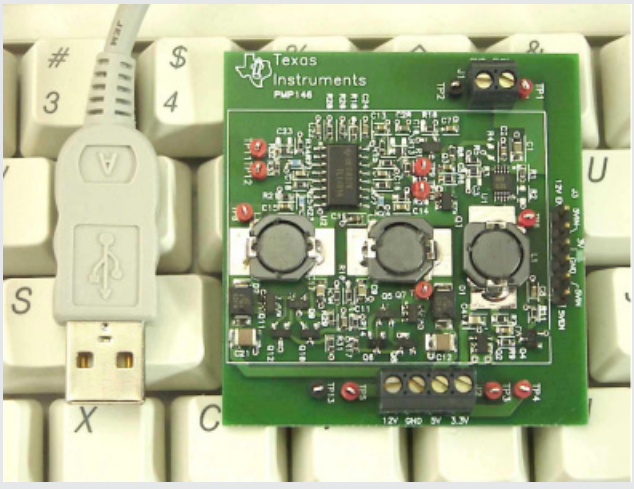
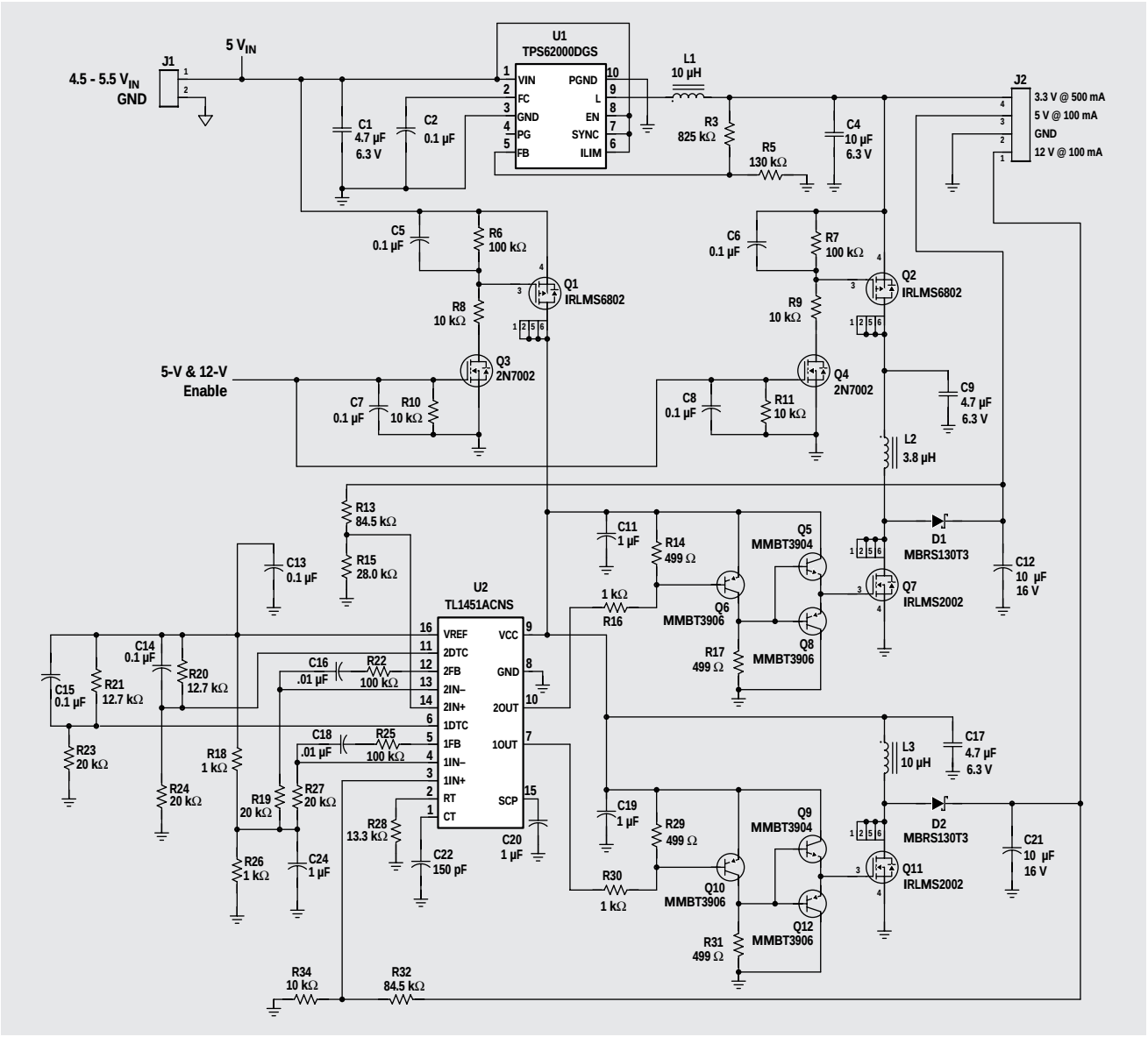


Figure 8. USB-powered DSL modem power supply



Conclusion

The design of a power supply powered from the USB port is heavily driven by the 2.25 W of available input power and the peripheral load requirements. The design process should involve a very careful analysis of load currents followed by a program to minimize them. Once the loads have been determined, the power-supply engineer should develop multiple block diagrams with the topologies described in this article to develop the lowest-cost, most power- and area-compliant approach. The array of integrated circuits to support these designs is very diverse; the designer has the options of striving for maximum integration, minimum cost, and ease of use.

Reference

1. USB Implementers Forum Inc., “Universal Serial Bus Specification Revision 2.0,” www.usb.org

Related Web sites

www.ti.com/sc/device/*partnumber*
Replace *partnumber* with TL1451A, TL5001, TPS2140, TPS6734, TPS43000, TPS54310, TPS54610, TPS54611, TPS60130, TPS60500, TPS62000 or UCC39421
www.usb.org

Fully differential amplifier design in high-speed data acquisition systems

By James Karki
Member, Group Technical Staff, High-Performance Linear

Introduction

Signal integrity is paramount in high-speed data acquisition systems in applications such as communications, imaging, instrumentation, video, and multimedia; and many engineers are finding the solution to be fully differential signal processing. The advantages are inherent in the architecture:

- External common-mode noise sources (from the power supply and other circuitry) are rejected by the differential nature of the architecture.
- Even-order harmonics tend to cancel.
- The required voltage swing for each differential output is only half that of its single-ended counterpart, thus reducing distortion and easing power-supply requirements.

All high-performance, high-speed data converters are now using differential inputs to enhance performance. Most often, amplification, impedance matching, filtering, and level shifting are required in front of the ADC. Not only are fully differential op amps ideal for these functions, but they also greatly simplify the design task.

Fully differential signal processing represents a paradigm shift in the design process that has some nuances that are not obvious. The purpose of this article is to highlight these design issues and show how to deal with them.

TI's THS45xx family of fully differential op amps is designed with a combination of high bandwidth, low distortion, and low noise that makes them suitable for interfacing to 12-bit and 14-bit high-speed data converters.

The data acquisition problem can be broken into four parts as depicted in Figure 1—the overall system requirements, the source interface, the amplifier's role or function, and the ADC interface. The design strategy is to design the interfaces between the signal source and the ADC with the proper amplifier function to realize the system requirements.

Source to amplifier interface

There are two general categories of sources that need to be considered: single-ended and differential. Single-ended sources are most often referenced to ground, whereas differential sources are not. The following discussion considers the design issues when a fully differential op amp is used in both situations.

In amplifier design, the input impedance of the amplifier is typically of prime concern; and this holds true for fully differential op amps.

Interfacing to a single-ended, ground-referenced source

If the source is single-ended and referenced to ground, a fully differential op amp can be used to convert the signal to differential (and level shift) as shown in Figure 2. V_S is the input source, with associated output impedance R_S.

Balance and gain

It is important to maintain balance in the amplifier by setting $R_{F1} = R_{F2}$ and $R_{G1} + R_S = R_{G2}$. The effect of mismatching the resistors is discussed later.

The differential output voltage is given by

$$V_{OD} = \frac{2(V_S)(1-\beta_1)+2V_{OCM}(\beta_1-\beta_2)}{(\beta_1+\beta_2)}, \text{ where}$$

$$\beta_1 = \frac{R_{G1}+R_S}{R_{G1}+R_S+R_{F1}} \text{ and } \beta_2 = \frac{R_{G2}}{R_{G2}+R_{F2}}.$$

If the resistor ratios are matched, the ratio of single-ended input to differential output gain is given by

$$\frac{R_{F2}}{R_{G2}} = \frac{R_{F1}}{R_{G1}+R_S}.$$

Note that the source resistance affects the gain of the amplifier.

Figure 1. The data acquisition problem

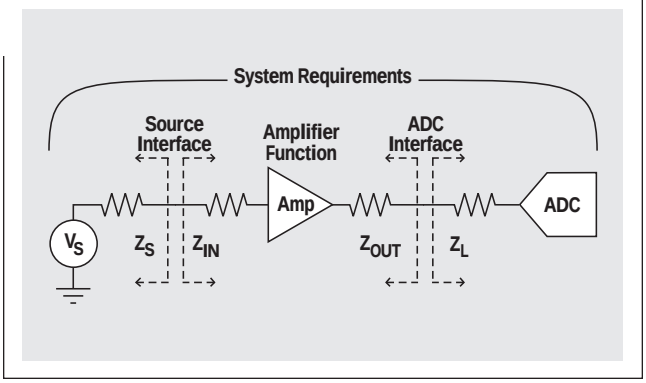
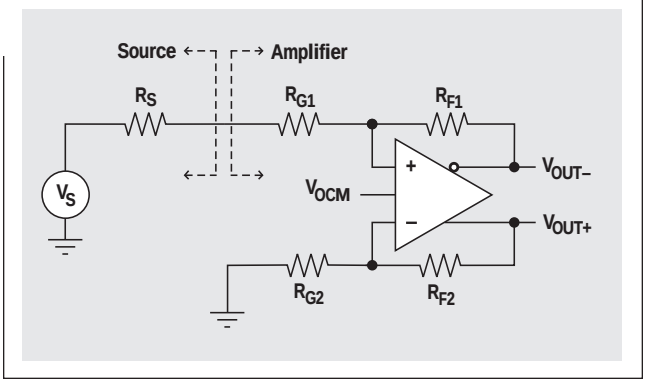


Figure 2. Single-ended source



The input impedance equals

$$\frac{R_{G1}}{1-\frac{K}{2\times(1+K)}},$$

where K is the gain of the amplifier. At high gain this converges to $2 \times R_{G1}$.

Input common-mode voltage

It is important not to violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming that the op amp is in linear operation, the voltage across the input pins is only a few millivolts at most; so finding the voltage at one input pin will determine the input common-mode voltage range to the op amp. In Figure 2 it is easiest to find the voltage at the negative input pin of the op amp, given by

$$V_{OUT+}\times\frac{R_{G2}}{R_{G2}+R_{F2}}.$$

To determine the required V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}.

The input common-mode voltage range is more likely to present a problem when the amplifier is operated with single-supply voltages and higher gains. For instance, take two amplifiers, each configured as shown in Figure 2, operating from +5 V with V_{OCM} = +2.5 V and the differential output voltage V_{OD} = 2 V_{p-p}. (Details on V_{OCM} are covered later under "Interfacing to the ADC.") One amplifier has a gain of 1 and the other has a gain of 10.

- With gain = 1, the required voltage range is 1 to 1.5 V—fairly relaxed limits.
- With gain = 10, the required voltage range is 0.18 to 0.27 V. The amplifier's V_{ICR} must go very near the negative supply voltage rail.

For this type of application, the IC designer must pay special attention to ensure that the op amp's V_{ICR} includes the negative rail. Take, for example, the THS4501; special level-shifting circuitry is used so that V_{ICR} can actually go below the negative rail.

Interfacing to a differential source

A differential input source is depicted in Figure 3. V_S is the differential input source, with associated output impedances R_{S1} and R_{S2}.

Balance and gain

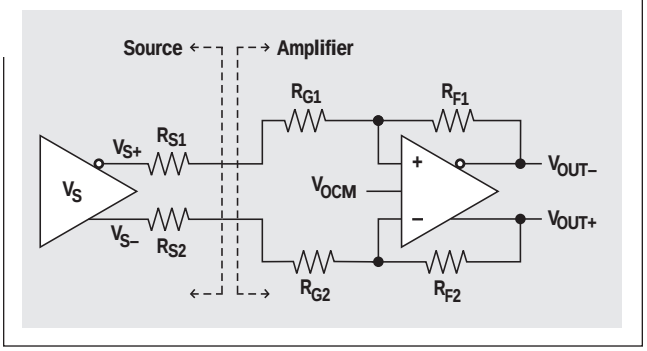
Again, it is important to maintain balance in the amplifier by setting $R_{F1} = R_{F2}$ and $R_{G1} = R_{G2}$. The input source must also be balanced with $R_{S1} = R_{S2}$. The effect of mismatching the resistors is discussed later.

The differential output voltage is given by

$$V_{OD}=\frac{2\left[(V_{S+})(1-\beta_1)-(V_{S-})(1-\beta_2)\right]+2V_{OCM}(\beta_1-\beta_2)}{(\beta_1+\beta_2)},$$

$$\text{where } \beta_1=\frac{R_{G1}+R_{S1}}{R_{G1}+R_{S1}+R_{F1}} \text{ and } \beta_2=\frac{R_{G2}+R_{S2}}{R_{G2}+R_{S2}+R_{F2}}.$$

Figure 3. Differential source



If the resistor ratios are matched, the ratio of differential input to differential output gain is given by

$$\frac{R_{F1}}{R_{G1}+R_{S1}}=\frac{R_{F2}}{R_{G2}+R_{S2}}.$$

Note that the source resistance is included in the gain equation again. The input impedance is equal to $R_{G1} + R_{G2}$.

Input common-mode voltage

Again, it is important not to violate the input common-mode voltage range (V_{ICR}) of the op amp. The analysis is not quite as easy as with a single-ended input, but still we can analyze one input pin and assume that the other has the same voltage due to amplifier action.

If we treat the positive input as a summing node, the voltage is given by

$$\left(V_{OUT-}\times\frac{R_{G1}+R_{S1}}{R_{G1}+R_{S1}+R_{F1}}\right)+\left(V_{S+}\times\frac{R_{F1}}{R_{G1}+R_{S1}+R_{F1}}\right).$$

To determine the required V_{ICR} of the op amp, the voltage at the positive input is evaluated at the extremes of V_{OUT-} and V_{S+}.

The input common-mode voltage range is more likely to present a problem when the source has a high or low common-mode voltage and the amplifier has high gain.

Let's look at an example of interfacing a CCD sensor to an ADC. The CCD sensor has 500 mV differential output centered around +9 V. The amplifier has a gain of 2 powered by +9 V referenced to ground, and V_{OCM} = +2.5 V; so the amplifier's output is 1 V_{p-p} centered around +2.5 V. The voltage range at the positive input to the op amp is +7.17 to +7.33 V. This is close to the positive rail, but not so close as to present a problem. If the sensor's output were lower and a high gain were required, the voltage range would approach the positive rail and the op amp might not work properly.

If the common-mode voltage of the source can be adjusted, centering it within the amplifier's V_{ICR} provides for optimal performance.

The impact of mismatched resistors

As stated earlier, the resistors need to be matched to maintain balance in the amplifier. What happens if the resistors are not matched?

In the following discussion:

- R_F is the feedback resistor from the output to the input on either side of the op amp; i.e., R_{F1} or R_{F2}.
- R_G is the resistance from the source to the input on either side of the op amp and includes the source resistance; i.e., $R_{G1} + R_S$, $R_{G1} + R_{S1}$, or $R_{G2} + R_{S2}$.

If the resistor ratios (R_F/R_G) are mismatched between the two sides of the op amp, the gain will vary proportionately to the mismatch, being a little higher than the average of the two sides. The internal common-mode feedback circuit will still maintain the output common-mode voltage equal to V_{OCM}. The output signals therefore remain balanced, swinging plus and minus with reference to V_{OCM}.

Ratio matching errors in the external resistors will degrade the circuit's ability to reject input common-mode noise. A 1% mismatch will result in about a 46-dB input CMRR.

Similarly, if the dc common-mode voltages at the input and output are different, matching errors will result in an offset in the differential output voltage. For the example given ($G \approx 1$, 1% mismatch, ground-referenced input signal, and V_{OCM} = 2.5 V), the output offset equals 12 mV.

To further illustrate the impact of mismatched resistors, the node voltages of the circuits shown in Figures 2 and 3 are analyzed with a 10% mismatch:

- Table 1 shows the effect of mismatched resistors in the single-ended source amplifier circuit shown in Figure 2: $R_{F1} = R_{F2} = R_{G2}$, but $R_{G1} + R_S = 0.9(R_{G2})$, and V_{OCM} = +2.5 V. Since the source's common-mode voltage is different from the output common-mode voltage of the op amp, the mismatch causes an offset in the differential output (V_{OD} = –0.135) with zero input. The gain is 0.946 + 0.135 = 1.081.
- Table 2 shows the effect of mismatched resistors in the differential source amplifier circuit shown in Figure 3: $R_{F1} = R_{F2} = R_{G2} + R_{S2}$, but $R_{G1} + R_{S1} = 0.9(R_{G2} + R_{S2})$; common-mode voltage of the source = +2.5 V; and V_{OCM} = +2.5 V. With the common-mode voltage of the source equal to the output common-mode voltage of the amplifier, the mismatch does not cause an offset in the differential output (V_{OD} = 0.000) with zero input. The gain of the amplifier is 1.054.

V_{OCM} is used to set the op amp's output to the common-mode voltage of the ADC's input.

At dc and lower frequencies, if the ratio R_F/R_G is equal between the two sides, the amplifier will be balanced. However if $R_{F1} \neq R_{F2}$ (or $R_{G1} \neq R_{G2}$), parasitic capacitance will unbalance the op amp at higher frequencies. For best operation, the feedback (and input) resistors should be equal.

Table 1. Effect of 10% resistor mismatch with a single-ended, ground-referenced source

V_S	V_{OCM}	V_{OUT+}	$V_{OUT–}$	V_{OD}	GAIN
0	2.5	2.432	2.568	–0.135	—
1	2.5	2.973	2.027	0.946	1.081

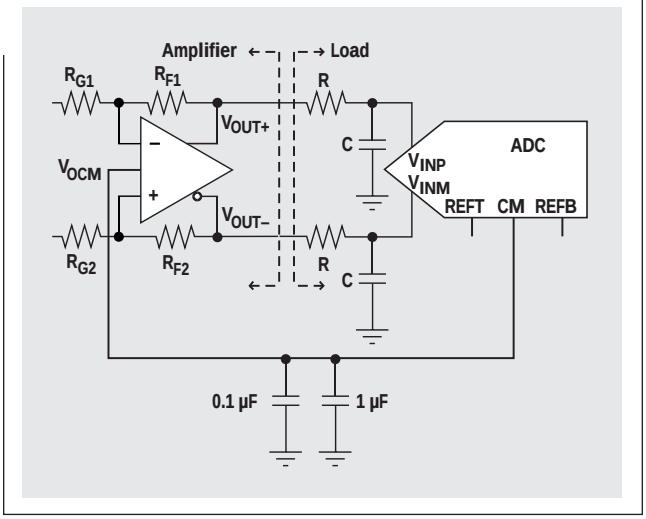
Table 2. Effect of 10% resistor mismatch with a differential source

V_{S+}	$V_{S–}$	V_{OCM}	V_{OUT+}	$V_{OUT–}$	V_{OD}	GAIN
2.5	2.5	2.5	2.500	2.500	0.000	—
3	2	2.5	3.027	1.973	1.054	1.054

Interfacing to the ADC

A primary function of the amplifier is to process the incoming signal so that it is at the correct bias point and amplitude to get optimal performance from the ADC. Obviously, it must have the bandwidth and ac performance to do this without compromising the signal. A simple, fully differential op amp-to-ADC interface is shown in Figure 4. The primary design issues in the interface are the load the amplifier drives and setting the proper output common-mode voltage.

Figure 4. Fully differential op amp-to-ADC interface

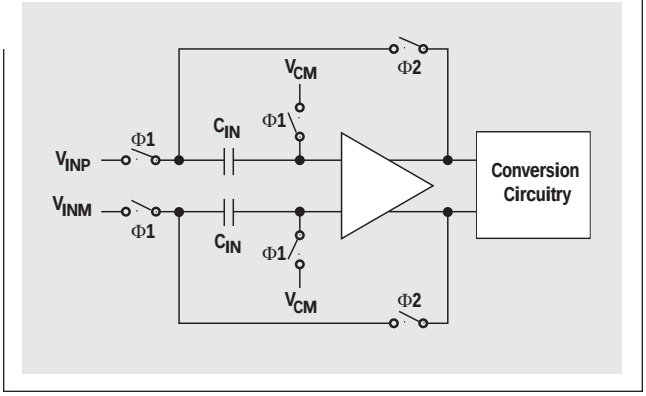


ADC input

Figure 5 shows a functional diagram of a high-performance ADC input. During Φ1, the input capacitors are charged to the difference between the input and V_{CM} (this is the sampling period—typically half the clock period). During Φ2, the charge is transferred to the conversion circuitry, where it is converted into the digital output.

It is almost universally recommended that a resistor and capacitor be used between the op amp's output and the ADC's input, as shown in Figure 4.

Figure 5. High-performance ADC input



This resistor-capacitor (RC) combination has multiple functions:

- The capacitor is a local charge reservoir for the ADC.
- The resistor isolates the amplifier from the ADC.
- In conjunction, they form a low-pass noise filter.

Charge reservoir

During the sampling phase, current is required to charge the ADC's input sampling capacitors. If external capacitors are placed directly at the input pins, most of the current is drawn from them. They are seen as a very low-impedance source. They can be thought of as serving much the same purpose as a power-supply bypass capacitor—to supply transient current, with the amplifier then providing the bulk charge.

Typically, a low-value capacitor in the range of 10 to 100 pF should provide the required transient charge reservoir.

Isolation

All this capacitance and the switched-capacitor input nature of the ADC is one of the worst loading scenarios that a high-speed amplifier will encounter. The resistor provides a simple means of isolating the associated phase shift from the feedback network and maintaining the phase margin of the amplifier.

Typically, a low-value resistor in the range of 10 to 100 Ω should provide the required isolation.

Noise filter

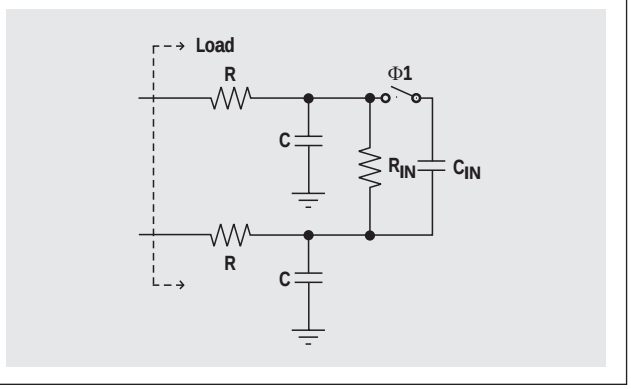
Together, R and C form a real pole in the s-plane located at the frequency

$$f_P = \frac{1}{2\pi RC}.$$

Placing this pole at about 10× the highest frequency of interest ensures that it has no impact on the signal.

Since the resistor is typically a small value, it is very bad practice to place the pole at (or very near) frequencies of interest. At the pole frequency, the amplifiers drive a load whose magnitude is $\sqrt{2} \times R$. If R is only 10 Ω or so, the amplifier is very heavily loaded above the pole frequency and will generate excessive distortion.

Figure 6. ADC input load model



Amplifier loading

With the RC combination at the input of the ADC, the amplifier drives a load that can be modeled as shown in Figure 6. Sometimes the input impedance of the ADC is such that $R_{IN} >> R$ and $C_{IN} << C$. In such cases the internal values can be ignored, and the input model is simply the external RC combination. For proper performance analysis, the amplifier should be tested with this load.

The output impedance of the op amp is important in considering the effect of output loading. Due to negative feedback, the output impedance of the op amp is very low over most of its bandwidth.

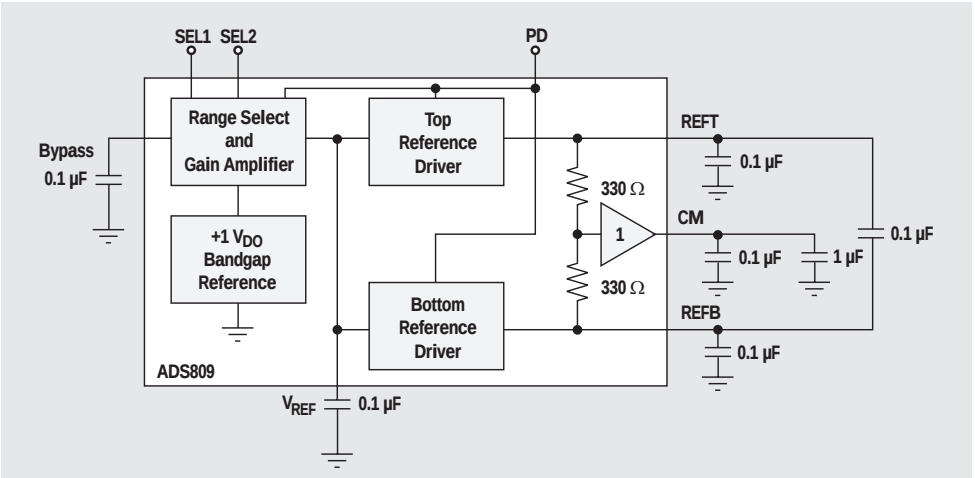
$$Z_O = \frac{z_O}{1 + A_F\beta},$$

where Z_O is the closed-loop output impedance; z_O is the open-loop output impedance; A_F is the frequency-dependent, open-loop gain of the amplifier; and β is the feedback factor

$$\beta = \left(1 + \frac{R_F}{R_G}\right).$$

At low frequencies the product $A_F\beta$ is very large and the output impedance → 0. The open-loop gain falls in proportion to the frequency. It is important, therefore, to use an amplifier at frequencies where $A_F\beta$ is very large to minimize the effect of the voltage divider between the output impedance and the load.

Figure 7. ADS809 internal reference circuit and recommended bypass scheme



ADC reference and input common-mode voltages

Figure 7 shows the internal reference circuit that is published in Reference 1. The reference voltages, REFT and REFB, determine the input voltage range of the converter. The voltage CM is

at the midpoint between REFT and REFB. The input signal to the ADC must swing symmetrically about CM to utilize the full dynamic range of the converter. This means that the output common-mode voltage of the amplifier must match this voltage.

The V_{OCM} input on the THS45xx is provided specifically for this purpose. Internal circuitry forces the output common-mode voltage to equal the voltage applied to V_{OCM}. Thus, V_{OUT+} and V_{OUT-} swing symmetrically about V_{OCM}. In many cases, all that is required is to tie CM to V_{OCM} with bypass capacitor(s) to ground (typically 0.1 µF to 10 µF).

Figure 8 shows a simplified schematic of the V_{OCM} input on the THS45xx. With V_{OCM} unconnected, the resistor divider sets the voltage halfway between the power-supply voltages. The equation

$$I_{Ext} = \frac{2V_{OCM} - (V_{CC+} + V_{CC-})}{50\ k\Omega}$$

shows how to calculate the current required from an external source to overdrive this voltage. Internal circuitry is used to cancel the bias current (I_{EA}) drawn by the V_{OCM} error amplifier. It is easy to see that, if the desired V_{OCM} is halfway between the power-supply voltages (as in a single +5-V-supply application), no external current is required. On the other hand, if the amplifier is being powered from ±5 V and the desired V_{OCM} is +2.5 V, the external source will need to supply 100 µA. Depending on the CM output drive from the ADC, a buffer may be required to supply this current.

Most high-performance ADCs using differential inputs have an output for setting the common-mode voltage of the drive circuit. Different manufacturers use different names for it—CM, REF, V_{REF}, V_{CM}, or V_{OCM}. Whatever it is called, there are two important things to remember: (1) Make sure it has enough output drive current if V_{OCM} is not at midrail; and (2) use bypass capacitors to reduce common-mode noise.

Figure 8. V_{OCM}

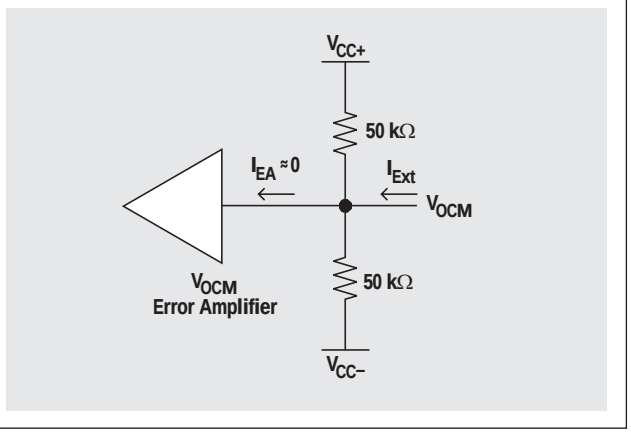


Figure 9. Single real-pole low-pass filter

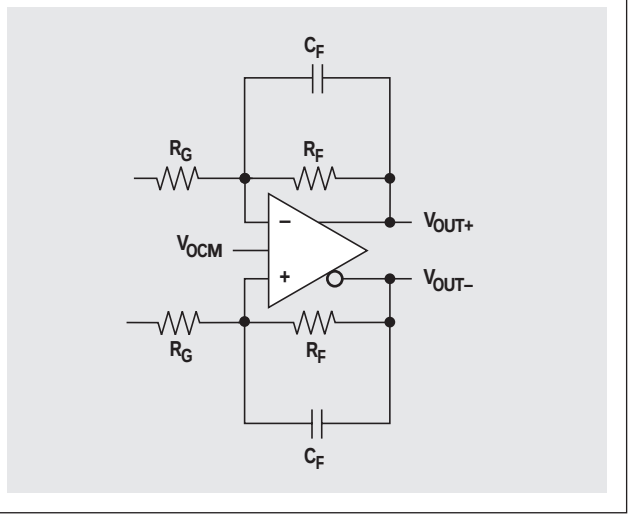
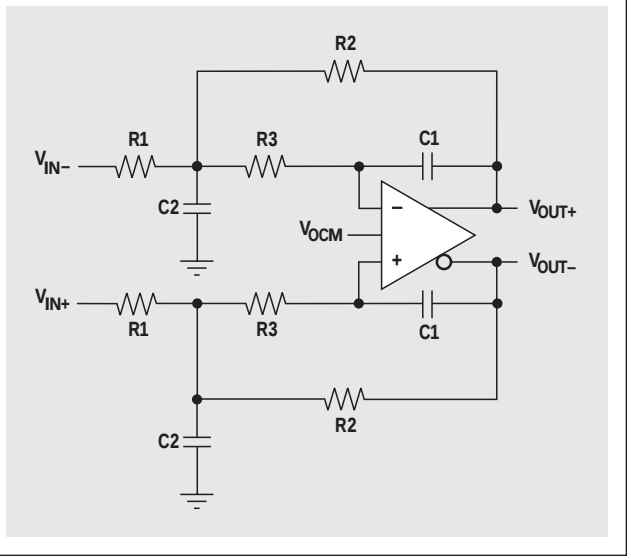


Figure 10. Second-order low-pass filter



Amplifier function

We have already discussed important amplifier design issues like setting the gain when interfacing to the source, and level shifting when interfacing to the ADC. Another common function the amplifier performs is filtering out-of-band signals. The following considers active low-pass filter design with fully differential op amps.

Single real pole

An active low-pass filter is made by adding capacitors of equal value across each feedback resistor, as shown in Figure 9. In this configuration, the op amp will attenuate frequencies above

$$f_P = \frac{1}{2\pi R_F C_F}.$$

The pole is a real pole in the s-plane.

Complex pole pairs

The classic filter types like Butterworth, Bessel, Chebyshev, etc. (second-order and greater), cannot be realized by real poles; they require complex poles. The multiple feedback (MFB) topology is used to create a complex pole pair and is easily adapted to fully differential op amps, as shown in Figure 10.

This is an active second-order low-pass filter, and the transfer function is

$$\frac{V_{OUT}}{V_{IN}} = \left[\frac{K}{-\left(\frac{f}{FSF \times f_C}\right)^2 + \frac{1}{Q}\left(\frac{jf}{FSF \times f_C}\right) + 1} \right],$$

where $V_{OUT} = (V_{OUT+}) - (V_{OUT-})$ and $V_{IN} = (V_{IN+}) - (V_{IN-})$,

$$K = \frac{R2}{R1}, \; FSF \times f_C = \frac{1}{2\pi\sqrt{R2R3C1C2}}, \text{ and}$$

$$Q = \frac{\sqrt{R2R3C1C2}}{R3C1 + R2C1 + KR3C1}.$$

K sets the pass band gain, f_C is the cut-off frequency of the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2}, \text{ and } Q = \frac{\sqrt{Re^2 + |Im|^2}}{2 \times Re},$$

where Re is the real part and Im is the imaginary part of the complex pole pair.

For design purposes, setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in

$$FSF \times f_C = \frac{1}{2\pi RC\sqrt{n \times m}} \text{ and } Q = \frac{\sqrt{mn}}{1 + m(1 + K)}.$$

The corner frequency, gain, and filter type set FSF, f_C, K, and Q. With these goals in mind, the designer can design the filter most easily in the following sequence:

1. Choose a capacitor ratio, n, that corresponds to common capacitor values for C1 and C2.
2. Use the ratio n determined in Step 1 and the equation

$$Q = \frac{\sqrt{mn}}{1 + m(1 + K)}$$

to see if there is a value for m that results in the desired Q of the filter. If the desired Q is not attainable, go back to Step 1 and choose a different capacitor ratio.

3. When suitable ratios for m and n are found, calculate R2 with the equation

$$R2 = \frac{1}{FSF \times f \times 2\pi C\sqrt{n \times m}},$$

and find the nearest standard resistor value.

4. Pick the nearest standard resistor value for R3 = mR2.
5. R1 is determined from

$$R1 = \frac{R2}{K}.$$

Pick the nearest standard resistor value.

6. Double check that the standard resistor values result in the desired gain and filter response. If not, some "tweaking" of the values may have better results.

A spreadsheet is an invaluable tool for doing these calculations.

System requirements

In the past, traditional amplifier specifications like signal-to-noise ratio, harmonic distortion, spurious free dynamic range, etc., have been used to define the quality of a system. These specifications were derived from system requirements like resolution, sensitivity, bit error rate, and the like.

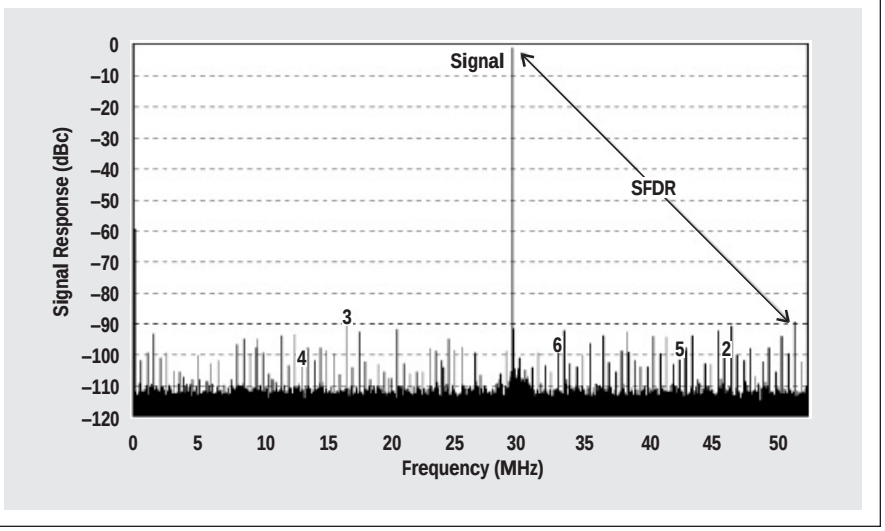
In the design of data acquisition systems today, the focus is on choosing the data converter. In high-speed, high-performance data acquisition systems, ac performance factors such as spurious free dynamic range (SFDR), effective number of bits (ENOB), and sampling rate drive the decision-making process, with dc errors being less important.

To determine the overall ac performance, the designer must analyze the system as a whole. The following discussion shows how to combine SFDR and ENOB to analyze the overall system performance.

SFDR

Spurious free dynamic range (SFDR) is the difference between the signal and the strongest spur, and is usually given in dBc. Figure 11 shows a fast Fourier transform (FFT) for a high-performance ADC. The spurious responses that are harmonics of the input signal are noted with their harmonic order (2–6). These harmonics are attributed to the nonlinearities in the input track-and-hold amplifier. In Figure 11 there is also a large number of spurs that are not harmonics of the input signal. These are attributed to the sampling process. Note that in Figure 11 the SFDR of the ADC is set by a spur that is not a harmonic of the signal.

Figure 11. FFT of a high-performance ADC



To determine the SFDR of the amplifier and ADC as a system, the output spectrum of the amplifier is overlaid on that of the ADC. The fully differential amplifier driving the ADC will have only spurs that are harmonics of the signal; so only harmonics of the signal will align and need to be added together.

How do we go about adding the harmonic spurs from two different sources? Since the electrical distances are not the same, resulting in random phase differences, the sources are added by their powers.

The FFT of the ADC's output is taken at a specified level, typically –1 dBFS. The amplifier's harmonics should also be measured at this level. Then the harmonic amplitudes of the amplifier and the ADC are converted from dBc to scalar quantities and added together. The result is converted back to dBc. The equation form is

$$HDx_{Combined}(dBc) = 10 \times \log_{10}\left[10^{\left(\frac{HDx\_Amp}{10}\right)} + 10^{\left(\frac{HDx\_ADC}{10}\right)}\right],$$

where HDx_Amp and HDx_ADC are the harmonic spurs in dBc from the amplifier and ADC.

Remembering some simple relationships helps to analyze the system quickly without doing any math. If the harmonics are equal, add 3.01 dB. If there is more than a 10-dB difference between the harmonic levels, ignoring the smaller one results in only a small error.

In a linear amplifier, the second and third harmonics normally are the most significant spurs and most likely will be the only points that need to be evaluated in this manner.

ENOB

Effective number of bits (ENOB) is not a traditional amplifier specification, but amplifiers can be attributed with an ENOB specification to compare them more directly with ADC specifications.

In an ADC, quantization noise sets a theoretical limit on the dynamic range that can be attained with a given number of bits. ENOB is a means of quantifying the effect of distortion and other noise sources within real ADCs that limit their dynamic range.

$$ENOB = \frac{SINAD(dBc) - 1.76}{6.02}.$$

The signal-to-noise ratio and total harmonic distortion added together (SINAD) is expressed as a positive number. To specify ENOB for an amplifier, measure the signal-to-noise ratio and harmonics at the ADC's specified input level, typically –1 dBFS. To get SINAD, add the signal-to-noise and harmonic levels by their powers in dBc. The procedure is the same as previously described for adding harmonics; convert from dBc to scalar quantities, add together, and convert the result back to dBc.

The ENOB of the combined system can be calculated by adding the SINAD of the amplifier and ADC together by their powers.

If the ENOB of the amplifier equals that of the ADC, the SINAD numbers are also equal. In this case, the combined SINAD is 3.01 dB lower, and the combined ENOB is 0.5 bit less.

Conclusion

We have considered the design of fully differential op amps in high-speed data acquisition systems, including the source/amplifier interface, amplifier/ADC interface, amplifier function, and overall system requirements.

Following are the key points to remember.

Source interface

- Input impedance:
  - With a single-ended source, $Z_{IN} = \frac{R_{G1}}{1 - \frac{K}{2 \times (1+K)}}$.
  - With a differential source, $Z_{IN} = R_{G1} + R_{G2}$.
- Include source impedance in the gain calculation.
- Ensure that the amplifier has the required input common-mode voltage range.

ADC interface

- Output impedance of the amplifier at low frequency is very low, $\rightarrow 0$, but can become a concern at higher frequencies.
- The RC combination between amplifier and ADC
  - provides isolation,
  - serves as a local charge reservoir, and
  - acts as a low-pass noise filter.
- The V_{OCM} pin allows an easy means of setting the output common-mode voltage. Ensure that the source has the required drive if V_{OCM} is not set to midrail.

Amplifier function

- Include source impedance in the gain calculation.
- Level shifting is accomplished via the V_{OCM} pin.
- The design can easily accommodate active first- or second-order low-pass filter function.

System requirements

- Add common spurs by their powers.
- If the largest spurs are equal and they align, then SFDR is degraded by 3.01 dB.
- If the ENOBs are equal, then ENOB is degraded by 0.5 bit.

Reference

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "12-Bit, 80-MHz Sampling Analog-to-Digital Converter," ADS809 Data Sheet	sbas170

Related Web sites

www.ti.com/sc/device/ADS809
www.ti.com/sc/device/THS4501

Worst-case design of op amp circuits

By Ron Mancini
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Introduction

Building reliable hardware requires all component tolerances to be accounted for during the design stage. Worst-case design techniques do not change the basic transfer equations for an op amp circuit; rather, the components assume a wide range of values that lead to a corresponding range of output voltages. This becomes complicated because active and passive components have different error sources and tolerances.

The sample design used as a teaching aid is a single-stage op amp configured as an amplifier: the circuit is designed, the effects of passive components are calculated, the effects of steady state versus drift errors are discussed, and methods of eliminating errors are discussed. Op amps have internal error sources, but they are left as the subject of another article because component drift tolerances almost always overshadow op amp internal error sources. Circuit equations not developed here are taken from Reference 1.

Passive component and reference tolerances

Resistors are the fundamental component in all circuits, so we consider their tolerances in detail. Resistors are specified with a purchase tolerance (P) expressed as a percentage; for example, 0.5%, 1%, 2%, 5%, and 10% are popular purchase tolerances. The purchase tolerance guarantees that the resistor is within its nominal value when you receive it. As soon as the resistor is used in an assembly, it starts to change value; and, because the resistor value usually is close to the limit of the purchase tolerance, its value changes beyond the purchase tolerance. External stresses like temperature, aging, pressure, humidity, mounting, sunlight, dust, and soldering force component values to change over time.

Resistor tolerances are estimated in Table 1. Notice that the purchase tolerance is kept separate from the drift tolerance; this is because the purchase tolerance can be adjusted, but the drift tolerance occurs during normal operation and causes errors unless calibration before measurement (CBM) is done.

The resistor manufacturing process determines the drift tolerance. The tighter-tolerance resistors are manufactured with more stable, controlled methods and with materials that resist drift. Excessive drift results in manufacturing rejects, and the tight process/material control techniques that minimize drift in the factory also minimize drift in the field.

It is common to represent a resistor as R_1 or R_2; and, keeping this nomenclature, we calculate the purchase and/or drift tolerance as $(1 \pm 0.01P \pm 0.01D)R_1$ to obtain the worst-case resistor value. The purchase and drift tolerances are given as percentages, and the ±0.01 factor converts them to actual values. Purchase and drift tolerances are positive or negative depending on external conditions, manufacturing methods, materials, and internal stresses. Individual resistor tolerances must be represented as positive or negative (whichever yields the worst-case calculation), unless the data sheet specifically states that all resistors drift in a prescribed direction. When calculating the absolute worst-case maximum value for a 5% $R_1 = 10\ k\Omega$, use $(1 + 0.01P + 0.01D)R_1 = (1 + 0.05 + 0.05)R_1 = 1.1R_1 = 11\ k\Omega$. The absolute worst-case minimum value for this resistor is $(1 – 0.01P – 0.01D)R_1 = (1 – 0.05 – 0.05)R_1 = 0.9R_1 = 9\ k\Omega$.

Capacitor tolerances, while not discussed in detail here, are handled in the same manner. Capacitor tolerances vary much more than resistor tolerances because of the radically different methods used to manufacture capacitors. Electrolytic capacitors often have purchase tolerances of +80, –20%; but some glass and NPO ceramic capacitors have purchase tolerances of 1%. In general, it is best to triple all capacitor tolerances unless you check the manufacturer's data sheets and determine otherwise. This errs on the conservative side but is good judgment when you haven't done your homework.

Reference voltages can be derived from reference ICs, zener diodes, signal diodes, or power supplies. The reference voltage has four errors: initial tolerance, temperature drift, load sensitivity, and noise. Initial tolerance is comparable to purchase tolerance in a resistor and is treated in

Table 1. Resistor tolerances

PURCHASE TOLERANCE (P) (%)	DRIFT TOLERANCE (D) (%)	TOTAL TOLERANCE (T) (%)
0.5	0.25	0.75
1	2	3
2	2	4
5	5	10
10	15	25

the same manner. Temperature drift, load sensitivity, and noise must be calculated for the environmental conditions to which the finished product will be exposed; furthermore, you must assume that these worst-case conditions exist simultaneously. Obviously, these three error sources are cumulative drift errors. Remember, the reference voltage acts like the command input to a servo and, if the circuit functions correctly, follows command input to the best of its ability.

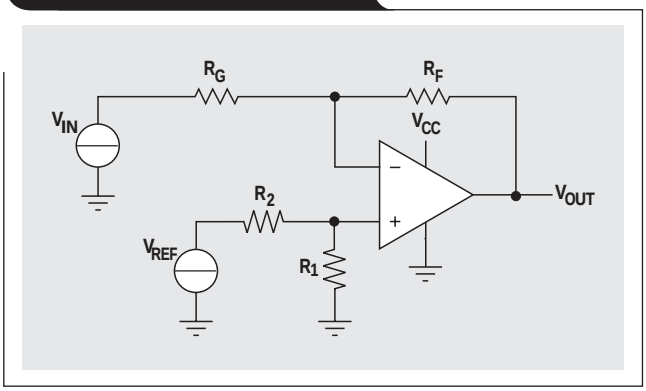
Design of the nominal circuit and resistor selection

The equation for the amplifier required by this design is

$$V_{OUT} = -16\,V_{IN} + 10.4. \quad \textbf{(1)}$$

The circuit that conforms to this equation is shown in Figure 1.

Figure 1. Amplifier circuit



Equation 1 is the general form of a transfer function; it is repeated with the op amp resistors as parameters in Equation 2.

$$V_{OUT} = -\left(\frac{R_F}{R_G}\right)V_{IN} + V_{REF}\left(\frac{R_1}{R_1+R_2}\right)\left(\frac{R_F+R_G}{R_G}\right) \quad \textbf{(2)}$$

Comparing terms in Equations 1 and 2 yields Equations 3 and 4.

$$|16| = \frac{R_F}{R_G} \quad \textbf{(3)}$$

$$b = V_{REF}\left(\frac{R_1}{R_1+R_2}\right)\left(\frac{R_F+R_G}{R_G}\right) \quad \textbf{(4)}$$

All resistors used in this sample design are 1%, and the reference voltage is 2.5 V with P = 1% and D = 2%. Equation 3 establishes the ratio of R_F to R_G as 16:1; and this ratio is satisfied by a large number of discrete resistor values like 16 Ω and 1 Ω, 160 Ω and 10 Ω, 1600 Ω and 100 Ω, or 160 kΩ and 10 kΩ. The designer establishes the impedance of the design by picking a resistor value that scales the remaining values. Low-value resistors draw more current, have better frequency response, and load the op amp; while high-value resistors are noisy and susceptible to printed circuit board leakage. Let us pick 10 kΩ for R_G, and then R_F = 160 kΩ. These resistor values are a good compromise because they are in the middle of the impedance range; if another resistor selection must be made later they can be selected higher or lower to satisfy network interactions. Equation 4 is algebraically manipulated to yield Equation 5.

$$R_2 = \left[\frac{V_{REF}(R_F+R_G)}{bR_G} - 1\right]R_1 = 3.086R_1 \quad \textbf{(5)}$$

Let R_1 = 12.4 kΩ and R_2 = 38.3 kΩ. R_1 is selected such that the parallel value of $R_1||R_2$ equals the parallel value of $R_F||R_G$. Equal parallel resistor network values inserted in each amp lead create equal common-mode voltages from the bias currents, and the op amp rejects common-mode voltage very well. Also, the 1% purchase tolerance and the flexibility of two different scaling resistors (R_1 and R_G) enables the choice of exact resistor ratios, so recalculating the transfer equation using the selected resistor values yields $V_{OUT} = -16\ V_{IN} + 10.39$.

Worst-case analysis

Equation 2 is rewritten as Equation 6 (see below), which includes the total tolerance and has been written to obtain the maximum value of the transfer equation.

The purchase tolerance can be adjusted with a potentiometer or a DAC/variable gain amplifier combination. It is useful to know how much adjustment is required to account for the purchase tolerance, so the purchase tolerance is substituted for the total tolerance in Equation 7 (see below).

Calculation of the tolerances and potentiometer values

The maximum and minimum transfer functions (for P = 1%) are

$V_{OUT(MAXP)} = -16.32\ V_{IN} + 10.86$ and **(8)**

$V_{OUT(MINP)} = -15.68\ V_{IN} + 9.947$. **(9)**

$$V_{OUT(MAXT)} = -V_{IN}\left[\frac{(1+T)R_F}{(1-T)R_G}\right] + (1+T)V_{REF}\left[\frac{(1+T)R_1}{(1+T)R_1+(1-T)R_2}\right]\left[\frac{(1+T)R_F+(1-T)R_G}{(1-T)R_G}\right] \quad \textbf{(6)}$$

$$V_{OUT(MAXP)} = -V_{IN}\left[\frac{(1+P)R_F}{(1-P)R_G}\right] + (1+P)V_{REF}\left[\frac{(1+P)R_1}{(1+P)R_1+(1-P)R_2}\right]\left[\frac{(1+P)R_F+(1-P)R_G}{(1-P)R_G}\right] \quad \textbf{(7)}$$

Notice that the slope tolerance is 2%, double the resistor purchase tolerance. This doubling occurs because the tolerances occur in a pure resistor ratio (no addition or subtraction). The intercept has two resistor ratios multiplied by a reference tolerance. The intercept resistor error is 3.36% rather than 4% for two reasons: (1) The resistors are not in a pure ratio; and (2) there are two resistor ratios multiplied times the reference voltage. You can never assume that x% resistors yield a 2x% tolerance unless they are used in a pure ratio.

The purchase tolerance error can be plus or minus, so the prudent designer doubles the error tolerance when calculating the value of a potentiometer to account for a double tolerance; and, because potentiometers have large errors, he usually triples the error tolerance. The slope error is now 6%. The potentiometer is in the R_G circuit, so its value is calculated as 0.06(10 kΩ) = 600 Ω. Since this potentiometer value is hard to find, a 1-kΩ potentiometer is used in the design. The value of R_G is reduced by half the potentiometer value to 9.53 kΩ. When the potentiometer is at zero value, the slope is –16.79 V; and when the potentiometer is at full value, the slope is –15.19 V. The full range of required values is therefore available with this adjustment.

The combined intercept tolerance (reference and resistors) is 4.4%, and tripling that tolerance yields 13.2%. The potentiometer is in the R_1 circuit, so its value is calculated as 0.132(12.4 kΩ) = 1.64 kΩ. Since this potentiometer value is hard to find, a 2-kΩ potentiometer is used in the design. The value of R1 is reduced by half the potentiometer value to 11.3 kΩ. When the potentiometer is at zero value, the intercept is 9.68 V; and when the potentiometer is at full value, the intercept is 10.95 V. The full range of required values is therefore available in the adjustment. The final circuit is shown in Figure 2.

The potentiometer selection procedure described here is adequate for the vast majority of design work. Tripling the purchase tolerance insures that the adjustment has adequate range to satisfy worst-case conditions with a good margin. This shortcut sacrifices resolution because an adjustment cannot have simultaneous wide range and wide resolution. Usually, resolution is not a problem; but when increased resolution is required, it can be obtained by using a multiturn potentiometer. When this trick fails to provide adequate resolution, the designer must go back to Equations 8 and 9, solve them for the limit resistor values, and insure that the potentiometer is just large enough to yield the limits.

Drift tolerances and their elimination

The resistor and reference drift tolerance is 2%. A large portion of the resistor drift tolerance results from temperature variations caused by ambient temperature fluctuations and self-heating; thus, when the resistor current is small and the ambient temperature is controlled, smaller drift tolerances are appropriate. Use the reference specifications to calculate the reference drift tolerance for each application, and don't neglect manufacturing and end-of-life stresses. Normally, purchase tolerances can be adjusted, but drift tolerances usually limit the circuit's accuracy. The worst-case analysis equations are used to calculate the effects of the drift tolerances.

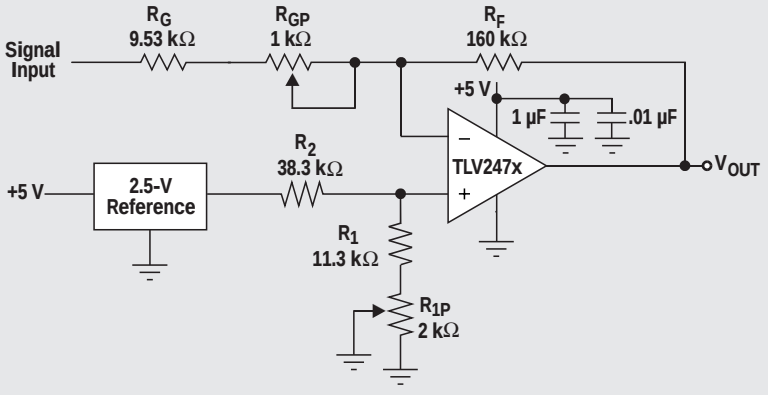
The maximum and minimum transfer functions (for D = 2%) are

$$V_{OUT(MAXD)} = -16.64\ V_{IN} + 11.34 \text{ and} \quad \textbf{(10)}$$

$$V_{OUT(MIND)} = -15.37\ V_{IN} + 9.514. \quad \textbf{(11)}$$

The transfer function varies approximately 15% because of the drift tolerances, and the best accuracy that the circuit can guarantee is 3 bits. Choosing more accurate resistors lowers the drift tolerance, and choosing resistors with a guaranteed temperature coefficient dramatically lowers the drift tolerance because all resistors must drift in the same direction. Careful evaluation of the ambient and life conditions might lower the drift tolerance, and you may choose to assume the risk that the components never drift to worst-case values. When the manufacturing volume of these circuits is large, statistics guarantee that some circuits will drift to the extreme; and it may be

Figure 2. Final circuit schematic



cost-efficient to accept those failures. Drift problems are the hardest for field people to identify and solve, so you might want to err on the cautious side.

The drift can be virtually eliminated by using CBM techniques. A DAC can be used to set the reference voltage, and a variable gain amplifier can be used as the gain stage (refer to Figure 3). The reference DAC is set to the nominal reference voltage. A known input voltage is applied, and the gain DAC increases the gain till the proper output voltage is achieved. A second known voltage is applied to the input, and the reference DAC is adjusted till the output voltage is correct. Rocking these two adjustments quickly yields better than 0.1% precision. If the measurement is taken shortly after the CBM process, it is very accurate.

Summary

Passive components have purchase and drift tolerances, and the drift tolerance may be larger than the purchase tolerance. The purchase tolerance can be adjusted at the end of the manufacturing process, but the drift tolerance can be adjusted only just prior to making a measurement. A circuit's output voltage can drift 15% if 1% resistors are used. Drift tolerances can be drastically reduced with CBM techniques.

Reference

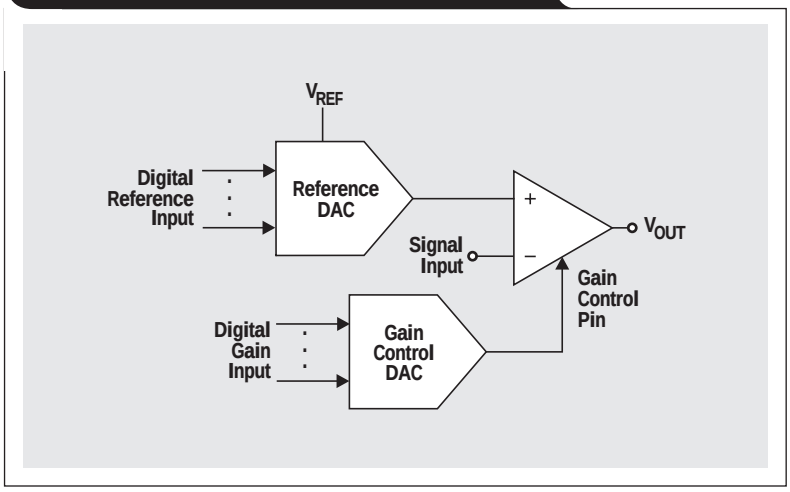
For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "Op Amps for Everyone," Design Reference . . .	slod006

Related Web sites

www.ti.com/sc/device/TLV247x

Figure 3. Block diagram of a CBM circuit



Using high-speed op amps for high-performance RF design, Part 1

By Bruce Carter

Advanced Linear Products, Op Amp Applications

Why use op amps for RF design? Traditional RF design techniques using discrete transistors have been practiced successfully for decades. RF designers who are comfortable with things "as-is" will scrutinize introduction of a new design technique using op amps. The cost of high-speed op amps, in particular, will raise eyebrows. Why replace a transistor that costs a few cents with a component that may cost several dollars?

This is a valid question to ask for high-volume consumer goods; and, in almost every case, the answer will be to stay with traditional techniques. For high-performance RF equipment, however, high-speed op amps have some distinct advantages. Many other applications have migrated to op amps to take advantage of the superior performance they provide. It is reasonable to assume that high-speed applications such as RF will also make the move.

This article will be presented in two parts. Part 1 focuses on the actual topology of RF stages formed with op amps and the scattering parameters. Part 2 will focus on some fine points of RF design and more specifications unique to RF.

Advantages

The major advantage of using high-speed op amps is a high degree of flexibility over discrete transistor implementations. When discrete transistors are used, the bias and operating point of the transistor interact with the gain and tuning of the stage. In contrast, when op amps are used, the bias of the stage is accomplished simply by applying the appropriate power supplies to the op amp power pins. Gain of the stage is completely independent of the bias. Gain does not affect the tuning of the stage, which is accomplished through passive components.

Op amps also reduce transistor parameter drift over the system operating temperature range.

Disadvantages

As attractive as op amps are for RF design, there are some barriers hindering their use. The first is, of course, cost.

The RF designer must learn how to set the op amp's operating point, but the process is considerably easier than biasing a transistor stage.

The RF designer is used to describing RF performance in certain ways. Op amp ac performance is described in terms of ac performance. The RF designer must learn how to translate op amp ac performance parameters into an RF context. That is one of the main purposes of this article.

Voltage feedback or current feedback?

The RF designer considering op amps is presented with a dilemma. Are voltage-feedback amplifiers or current-feedback amplifiers better for the design?

The bandwidth specification given in op amp data sheets refers only to the point where the unity gain bandwidth of the device has been reduced by 3 dB by internal compensation and/or parasitics—not very useful for determining the actual operating frequency range of the device.

Internally compensated, voltage-feedback amplifier bandwidth is dominated by an internal "dominant pole" compensation capacitor, resulting in a constant gain/bandwidth limitation. Current-feedback amplifiers, in contrast, have no dominant pole capacitor and therefore can operate much more closely to their maximum frequency at higher gain. Stated another way, the gain/bandwidth dependence has been broken.

Comparing a voltage-feedback and current-feedback op amp illustrates this:

- THS4001, a voltage-feedback amplifier with a 270-MHz (–3-dB) open-loop bandwidth, is usable to only about 10 MHz at a gain of 100 (20 dB).
- THS3001, a current-feedback amplifier with a 420-MHz (–3-dB) open-loop bandwidth, is usable to about 150 MHz at a gain of 100 (20 dB).

The choice is still up to the designer. At unity and low gains there may not be much advantage to using a current-feedback amplifier, but at higher gains the choice is clearly a current-feedback amplifier. Many RF designers would be extremely happy if they could obtain a gain of 10 (20 dB) in a single stage with a transistor—difficult to do. With an op amp, it is almost trivial.

The RF designer must be aware of some issues with current-feedback amplifiers:

- Conventional circuit topologies are unchanged for current-feedback amplifiers.
- Current-feedback amplifier data sheets recommend values for R_F, the feedback resistor. These recommendations should be taken seriously. Gain adjustment should be made with R_G.
- Keep capacitors out of the feedback loop.

Other than these restrictions, no additional care is needed with the current-feedback amplifier except the normal care in layout and meeting bypass requirements of high-speed RF circuitry.

For both voltage- and current-feedback amplifiers, capacitance on the inverting op amp input should be limited, as this is a major cause of instability. It is very easy to accumulate stray capacitance on a sloppy PCB layout. To reduce this stray capacitance, Texas Instruments recommends a hole in the ground and power planes under the inverting input of an op amp on a multilayer board.

A review of traditional RF amplifiers

A traditional RF amplifier (Figure 1) uses a transistor (or, in the early days, a tube) as the gain element. The dc bias ($+V_{BB}$) is injected into the gain element at the load through a bias resistor, R_B. RF is blocked from being shorted to the supply by an inductor, L_C, and dc is blocked from the load by a coupling capacitor.

Both the input impedance and the load are 50 Ω, which ensures matching between stages.

When an op amp is substituted as the active circuit element, several changes are made to accommodate it.

By themselves, op amps are differential-input, open-loop devices. They are intended for a closed-loop operation (different from a receiver's AGC loop). The feedback loop for each op amp must be closed locally, within the individual RF stage.

There are two ways of accomplishing this—"inverting" and "non-inverting." These terms refer to whether or not the output of the op amp circuit is inverted from the input. From the standpoint of RF design, this is seldom of any concern. For all practical purposes, either configuration will work and give equivalent results. The non-inverting configuration is probably the easiest to use.

Figure 2 shows a non-inverting RF amplifier. The input impedance of the non-inverting input is high, so the input is terminated with a 50-Ω resistor. Gain is set by the ratio of R_F and R_G. For log gain,

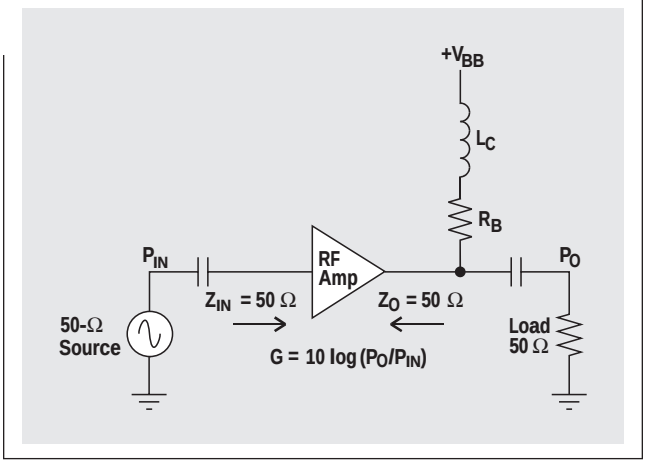
$$G = 20\log\frac{1}{2}\left(1+\frac{R_F}{R_G}\right)\text{ dB.}$$

For a desired gain,

$$1+\frac{R_F}{R_G} = 2(10^{G/20}).$$

The output of the stage is converted to 50 Ω by placing a 50-Ω resistor in series with the output. This, combined with a 50-Ω load, means that the gain is divided by 2 (–6 dB) in a voltage divider; so a unity-gain (0-dB) gain stage would become a gain of 0.5, or –6 dB.

Figure 1. Traditional RF stage



The RF designer may notice that the power-supply requirements have been complicated by the addition of a second negative supply. The stage can be modified easily for single-supply operation.

Amplifier gain, revisited

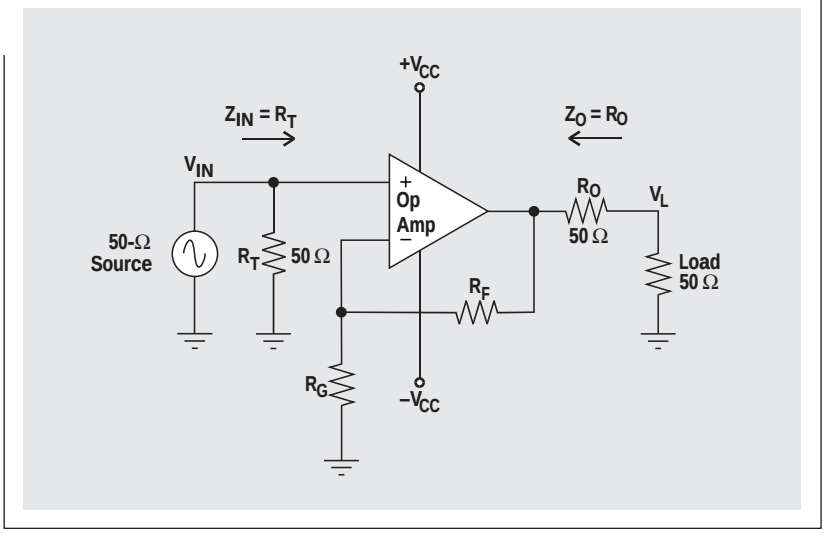
Op amp designers think of the gain of an op amp stage in terms of voltage gain. RF designers, however, are used to thinking of RF stage gain in terms of power:

$$\text{Absolute power (W)} = \frac{V_{rms}^{\ 2}}{50\,\Omega}.$$

$$P_O(\text{dBm}) = 10\log\left(\frac{\text{Absolute power}}{0.001\,\text{W}}\right).$$

$$\text{dBm} = \text{dBV} + 13 \text{ in a 50-}\Omega\text{ system.}$$

Figure 2. Non-inverting RF op amp gain stage



Scattering parameters

RF stage performance is often characterized by four "scattering" parameters, which are defined in Table 1. (VSWR, or voltage standing-wave ratio, is just another term for input or output reflection.)

The term "scattering" has a certain implication of loss, and that is indeed true in three cases. Reflections, as in the VSWR scattering parameters S_{11} and S_{22}, can cancel useful signals. Reverse transmission, S_{12}, steals output power from the load. The only desirable scattering parameter is S_{21}, the forward transmission. Design of an RF stage involves maximizing S_{21} and minimizing S_{11}, S_{22}, and S_{12}.

Small-signal ac parameters specified for RF amplifiers are derived from S-parameters. These specifications are frequency-dependent. They are measured with a network analyzer and an S-parameter test set. The test circuit is shown in Figure 3.

Table 1. Scattering parameters

	SCATTERING PARAMETER	RF AMPLIFIER SPECIFICATION
S_{11}	Input reflection	Input VSWR
S_{22}	Output reflection	Output VSWR
S_{21}	Forward transmission	Amplifier gain and bandwidth
S_{12}	Reverse transmission	Reverse isolation

Input and output VSWR S_{11} and S_{22}

VSWR is a ratio and therefore a unitless quantity. It is a measure of how well the input and output impedances are matched to the source and load impedances. They should be as closely matched as possible to avoid reflections.

VSWR is defined as:

$$\text{VSWR} = \frac{Z_{I/O}}{Z_S} \text{ or } \frac{Z_S}{Z_{I/O}}, \text{ whichever} > 1,$$

where $Z_{I/O}$ is the amplifier input or output impedance; and Z_S is the test system source impedance. The ideal VSWR is equal to 1:1, but typical VSWRs will be no better than 1.5:1 for RF amps over their operating frequency range.

Measuring the input VSWR is a matter of measuring the ratio of the reflected power versus incident power on Port 1 (S_{11}) in Figure 3. A perfect match will reflect no power. Output VSWR is measured the same way at Port 2 (S_{22}).

An op amp's input and output impedances are determined by external components selected by the designer. For this reason, VSWR cannot be specified on an op amp's data sheet.

Return loss

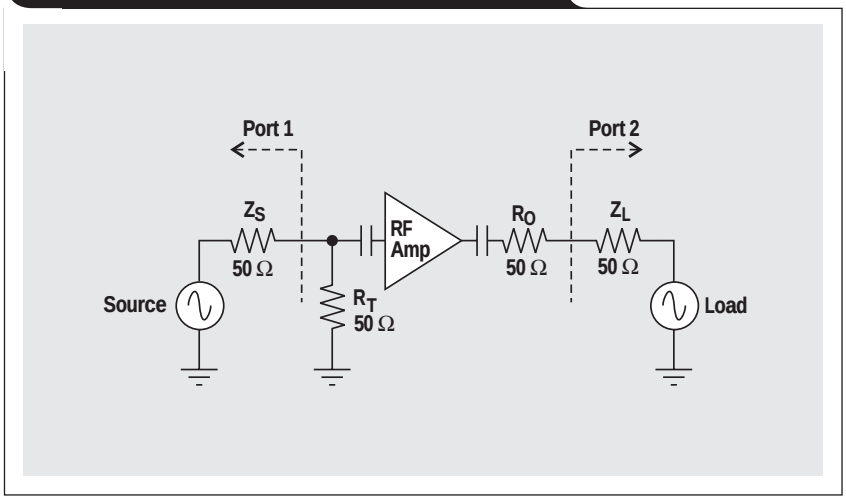
Return loss is related to VSWR in the following way:

$$\text{Return loss} = 20\log\left(\frac{\text{VSWR}+1}{\text{VSWR}-1}\right) = 10\log(S_{11})^2 \text{ input}$$

$$\text{or} = 10\log(S_{22})^2 \text{ output}.$$

R_O is not a perfect match for Z_L at high frequencies. The output impedance of the amplifier will increase as the loop

Figure 3. Scattering-parameter test circuit



gain falls off. This will change the output VSWR. A peaking capacitor, C_O, added in parallel with R_O, can compensate for this effect (Figure 4). Because op amp output impedance will be well defined, a fixed value usually can be substituted after experimentation determines the correct value.

Reducing the input impedance of the amplifier will extend the maximum usable frequency by swamping the effects of high-frequency parasitic components.

Forward transmission S_{21}

The forward transmission S_{21} is specified over the operating frequency range of interest. S_{21} is never specified on an op amp data sheet because it is a function of the gain, which is set by the input and feedback resistors R_F and R_G, respectively. The forward transmission of a non-inverting op amp stage is:

$$S_{21} = A_L = \frac{V_L}{V_{IN}} = \frac{1}{2}\left(1 + \frac{R_F}{R_G}\right).$$

The forward transmission of an inverting op amp stage is:

$$S_{21} = A_L = -\frac{V_L}{V_{IN}} = -\frac{1}{2}\left(\frac{R_F}{R_G}\right).$$

Op amp data sheets show open-loop gain and phase. It is the responsibility of the designer to know the closed-loop gain and phase. Fortunately, this is not difficult. The data sheets often include excellent graphs of open-loop bandwidth and sometimes include phase. Closing the loop produces a straight line across the graph at the desired gain, curving to meet the limit. The open-loop bandwidth plot should be used as an absolute maximum. The designer who approaches the limit does so at the expense of extensive compensation and complex PCB layout techniques.

Reverse transmission S_{12}

Op amp topologies, in particular current-feedback amplifiers, assume that both inputs are connected to low impedances. Therefore, the reverse isolation of op amp RF circuits is excellent.

Reverse isolation is somewhat better in non-inverting current-feedback amplifier configurations, because the output signal must also leak through the circuitry connecting the non-inverting and inverting inputs to get to the source.

Phase linearity

Often, a designer is concerned with the phase response of an RF circuit. This is particularly the case with video design, which is a specialized type of RF design. Current-feedback amplifiers tend to have better phase linearity than voltage-feedback amplifiers.

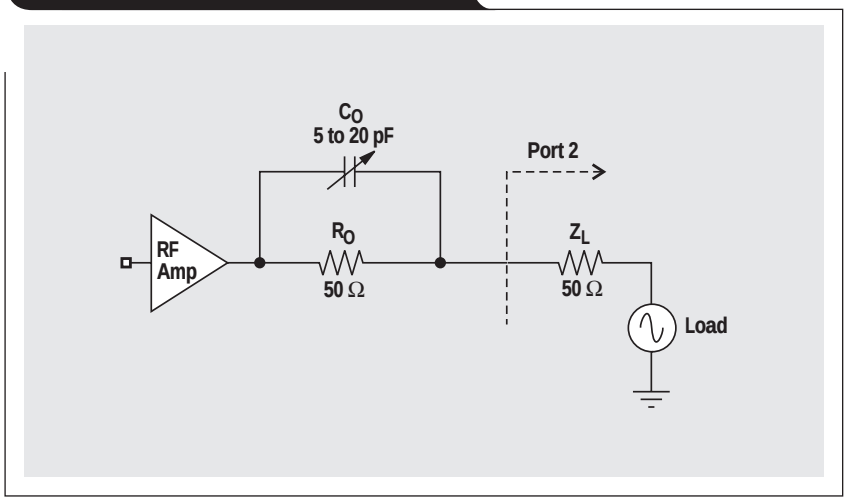
- Voltage-feedback THS4001: Differential phase = 0.15°.
- Current-feedback THS3001: Differential phase = 0.02°.

Look for Part 2 of this article and conclusions to be published in a future issue of *Analog Applications Journal*.

Related Web sites

www.ti.com/sc/device/THS3001
www.ti.com/sc/device/THS4001

Figure 4. Output peaking capacitor



Analog design tools

By John Bishop
Applications Specialist, High-Performance Linear Products

Introduction

Most analog designers are using design tools developed for use on the computer. Many such tools are available via TI's Analog and Mixed-Signal home page (www.ti.com/sc/analogmsp) by selecting the Engineer Design Utilities link located in the product group windows for AMPLIFIERS AND COMPARATORS and POWER MANAGEMENT. These tools operate as stand-alone Windows® operating system applications, Web-based applications, or Microsoft® Excel spreadsheets. This article lists available analog tools and provides some information about each.

Applications for the designer

Tables 1 and 2 on pages 53–54 list applications along with their supported products, environments, and descriptions.

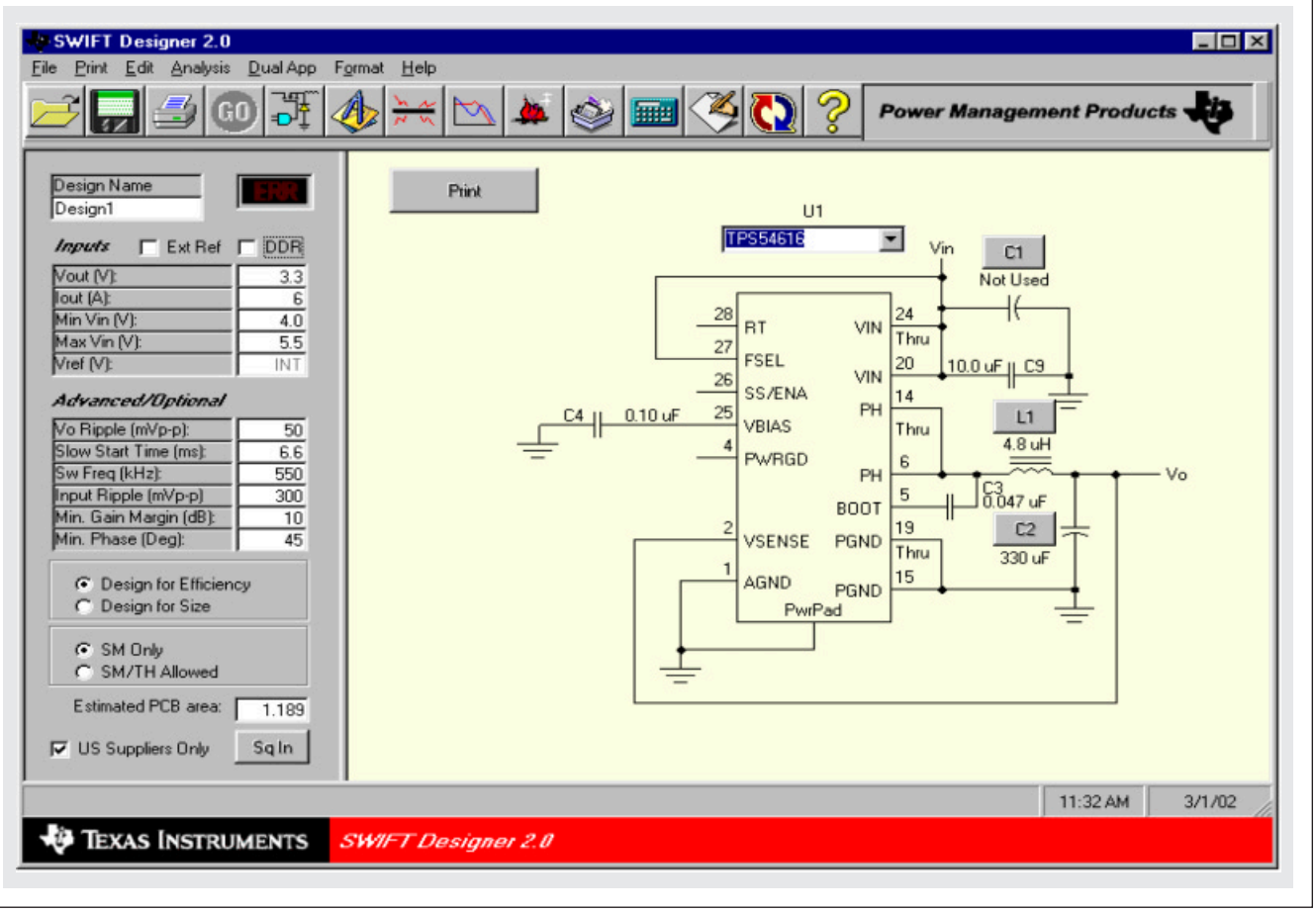
Windows application tools

These tools were developed as Windows applications because they are the most comprehensive and computer-intensive. They can be downloaded and installed on the user's computer.

SWIFT™ Designer

Figure 1 is a screen shot from SWIFT (Switcher with Integrated FET Technology) Designer. The software generates a complete design solution using TPS54610, TPS54616, or TPS54672 buck PWM regulator devices. SWIFT provides the designer with a schematic, bill of materials, efficiency graph, and response graph for the completed design.

Figure 1. SWIFT Designer screen display showing TPS54616 PWM regulator



FilterPro™ for Windows

FilterPro is a Windows application that can be downloaded from the Web and installed in the user's computer. It is supported with an Application Report (Reference 2).

FilterPro allows a designer to develop a low-pass filter with up to 10 poles by using a Sallen-Key or multiple-feedback (MFB) circuit type. In addition, the filter type can be either Bessel, Butterworth, or Chebyshev.

Figure 2 is a screen shot from FilterPro.

Web-based tools

An advantage of Web-based tools is that they usually download quickly because they comprise HTML pages whose file sizes are small. No installation program must be run, and the tools don't need to be installed permanently on the designer's hard drive.

Some tools, such as the Resistor Value Selection utility, contain JavaScript programs that perform calculations usually done by programs written for Excel or Windows.

Fully differential component calculator

When a fully differential amplifier is employed, it is important to balance the two feedback paths with the same resistor ratio to prevent an offset from being present between the two outputs. When a single-ended input is to be terminated and connected to one of the inputs, this termination must be accounted for in the feedback ratio for that input. Doing this results in a gain change. In addition, the termination resistor value used should take into account the input impedance of the amplifier circuit. For these reasons, it is difficult to calculate optimal component values for a fully differential amplifier design whose input is single-ended and terminated.

The program shown in Figure 3 (on page 52) is a JavaScript application that accepts your entry of source resistance (R_s), feedback resistor (R4) or gain resistor (R3), and desired differential gain (A). It then calculates the other resistors.

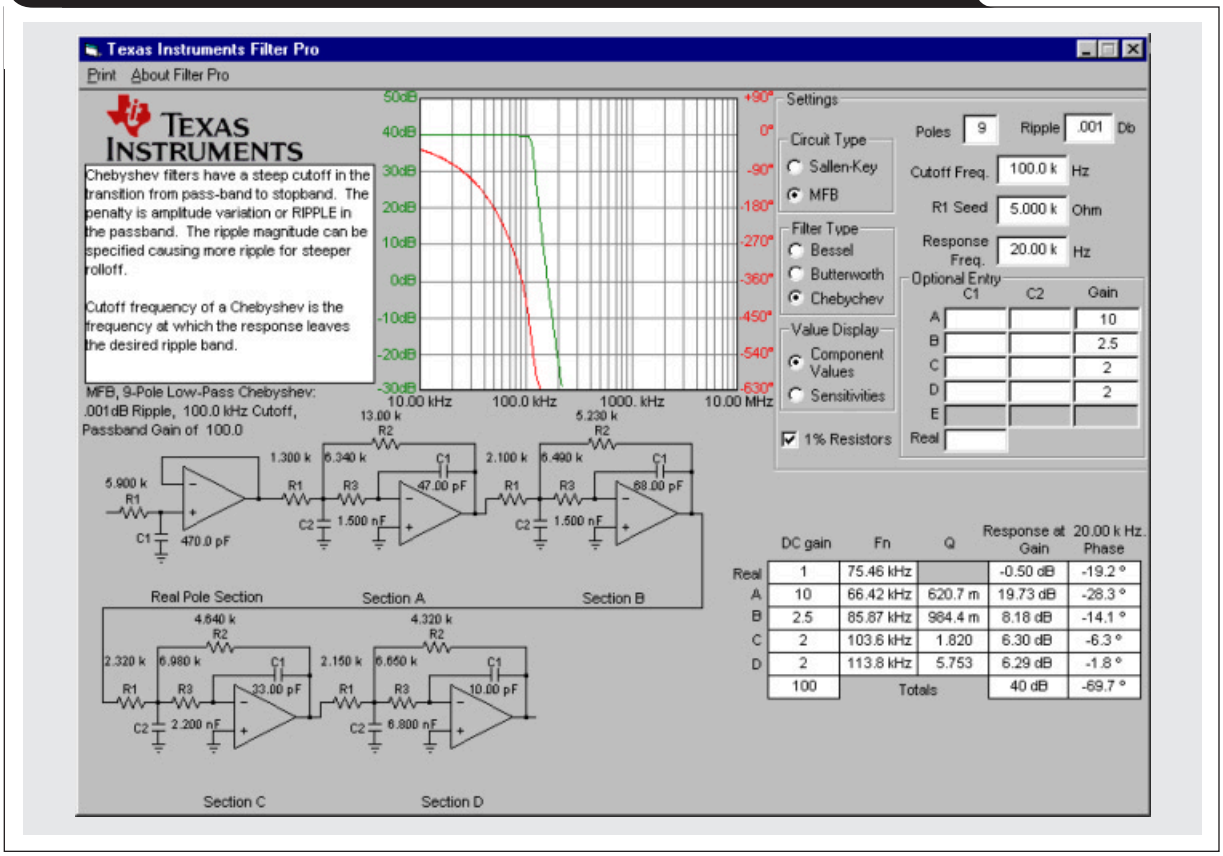
Selecting the "E96" or "E192" radio buttons will cause the calculated resistor values to be selected from the E96 group (96 values per decade) or E192 group (192 values per decade), respectively. E96 values are commonly known as 1% resistors, while E192 values are known as 0.5% resistors. Tighter tolerances are available for these groups. When the "Exact" radio button is selected, the values are not selected from the E96 or E192 groups.

$R_{R3,\ R4}$ is the input impedance represented by R3 and a portion of R4 as determined by the action of the amplifier and its gain.

Limits

1. The gain entry is the differential gain of the total circuit. The voltage divider consisting of R_s, R_t, and the amplifier input resistance causes a gain of 0.5 at the input of R3. A gain of 2 from this point to the outputs will cause a total differential gain of 1. A gain entry of less than 0.5 is not allowed. A total gain of less than 0.5 would cause the amplifier to be less than unity gain; therefore it may not be stable. The maximum gain entry is 1000.

Figure 2. FilterPro screen display showing 9-pole MFB filter with 40-dB gain



2. The input impedance of the stage reflects the active response of the amplifier combined with the values of R3 and R4. The design is not valid if the stage input impedance is less than the source resistance.
3. Values entered for R3 and R4 must be positive numbers.
4. Resistor values, whether entered or calculated, must be equal to or between 1 Ω and 1 MΩ.

Excel tools

These tools are Excel spreadsheet files that operate under Microsoft® Excel when downloaded. The Excel method is good for many engineers and designers who need to do a simple task with little effort. It is also very helpful to those who are developing Excel applications, because they can either edit the downloaded tool as needed or insert parts of it into their own Excel tools.

Like the Web-based tools, Excel tools download quickly and don't require a large amount of hard drive space.

Conclusion

Using design tools developed by Texas Instruments, a designer can develop analog applications with fewer complex calculations. In addition, the interactive nature of many of these tools enables iterative design techniques that are not feasible without them.

The functionality and number of these applications have increased dramatically over the past year, and many future additions are expected.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "Op Amps for Everyone," Design Reference	. . .slod006
2. "FilterPro™ MFB and Sallen-Key Low-Pass Filter Design Program," Application Report	. . .sbfa001

Related Web sites

www.ti.com/sc/analogmsp
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with THS4131, TL431, TLC555, TPS6734, TPS7101, TPS7201, TPS7301, TPS54610, TPS54611, TPS54672 or UAF42

Figure 3. Fully differential amplifier component calculator

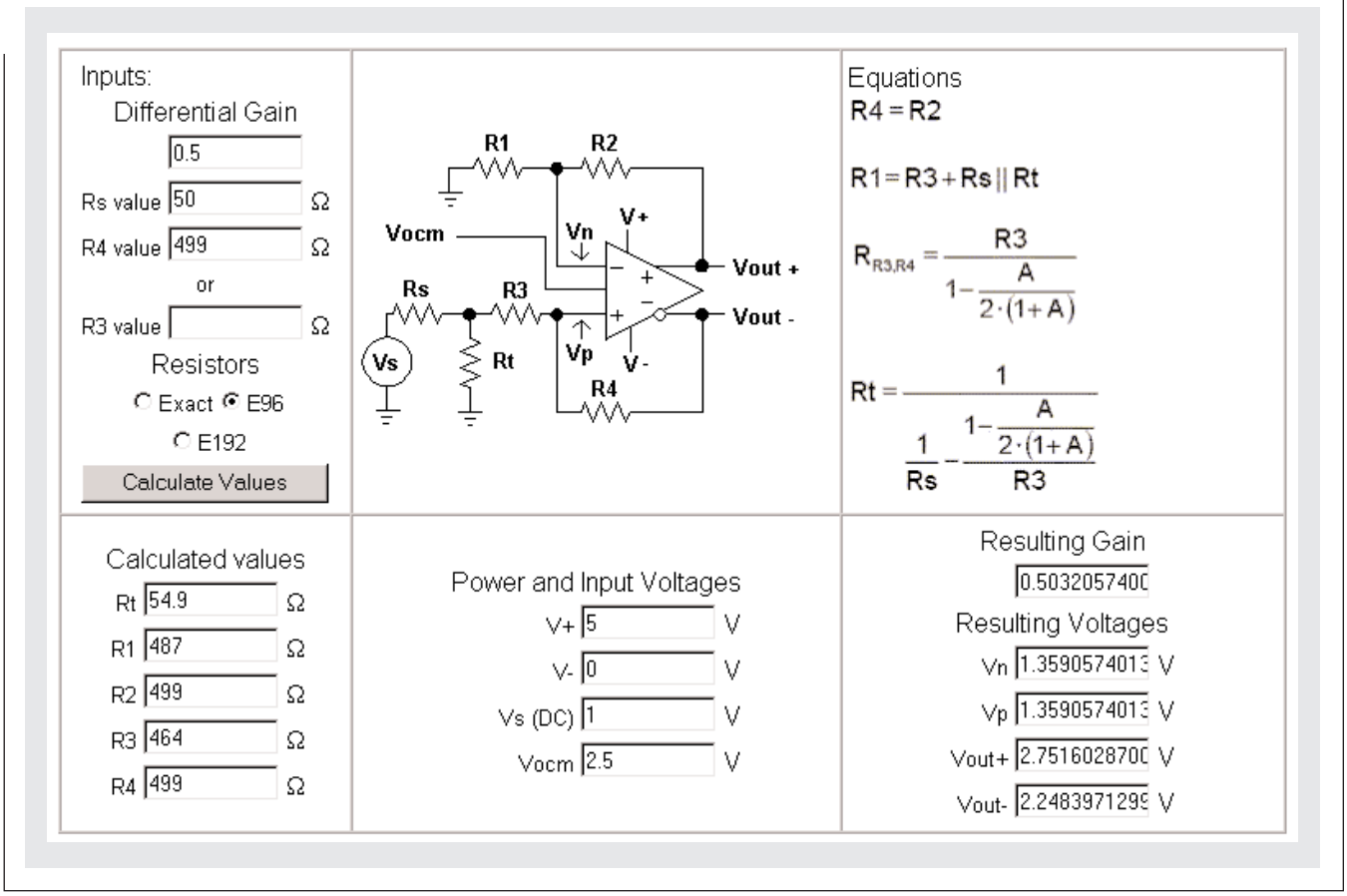


Table 1. Analog design tools available on the Web for Amplifiers and Comparators
To find the tools below, go to www.ti.com/sc/analogmsp and, under AMPLIFIERS AND COMPARATORS, click on Engineer Design Utilities.

APPLICATION NAME	SUPPORTED PRODUCTS	ENVIRONMENT	DESCRIPTION
Fully Differential Amplifier Component Calculator	Fully differential amplifiers	Web-based	This utility calculates the resistor values for a single-ended input to a differential output amplifier with a terminated input.
Buffer Op Amp to Analog-to-Digital Converter Design	Standard and fully differential amplifiers	Web-based	This tool shows typical input buffer solutions for analog-to-digital converters based on parameters the user supplies.
Op Amp Gain and Offset Stage Component Calculator	Standard op amps	Excel	This spreadsheet shows the schematic and calculates the resistors required for systems with both dc gain and offset. Four cases are shown that correspond to the cases in Chapter 4 of Reference 1.
Effective Number of Bits Calculator	THS4131 and THS4141 fully differential amplifiers	Excel	Allows the calculation of the effective number of bits of resolution for the THS4131 and THS4141, given the noise figure, frequency of operation, peak-to-peak voltage, and THD for the frequency of choice.
Fully Differential Op Amp Gain Calculator	Standard fully differential amplifiers	Excel	This calculator predicts the expected values for V_{OUT+} and V_{OUT-} for any ratio of (R1/R2) and (R3/R4), given R1, R2, R3, R4, V_{IN+}, V_{IN-}, and V_{OCM}.
Resistor Value Selection	General electronics	Web-based	This utility selects a standard resistor value when a calculated value is entered.
Reading the E96 5-Band Resistor Color Code	General electronics	Web-based	This utility allows a designer or technician to enter the color bands of a 5-band resistor and then see its value.
Reading the E24 4-Band Resistor Color Code	General electronics	Web-based	This utility allows a designer or technician to enter the color bands of a 4-band resistor and then see its value.
Inverting Op Amp Gain Stage Utility	Standard op amps	Excel	Specify the desired voltage gain of the system, open-loop gain of the selected op amp, and range of the base resistor; and this Excel utility calculates the best set of resistors to use in an inverting op amp configuration. In this utility the user can choose 0.5%, 1%, or 5% resistors.
Non-Inverting Op Amp Gain Stage Utility	Standard op amps	Excel	Specify the desired voltage gain of the system, open-loop gain of the selected op amp, and range of the base resistor; and this Excel utility calculates the best set of resistors to use in an inverting op amp configuration.
Voltage Divider Utility	General electronics	Excel	Specify the input voltage, desired output voltage, and range of the base resistor; and this Excel utility calculates the best set of resistors for a voltage divider to achieve the desired output voltage. In this utility the user can choose 0.5%, 1%, or 5% resistors.
FilterPro™ for Windows	Standard op amps	Windows	The FilterPro program is designed to aid in the design of low-pass filters implemented with the multiple-feedback and Sallen-Key topologies.
FilterPro for UAF	UAF42 universal active filter	DOS	The SWIFT™ Designer power-supply design program enables both novice and experienced designers to produce single-output, step-down converter designs with ease.
Single Pole Low Pass Filter Response Calculator	Standard op amps	Excel	This Excel spreadsheet uses macros to calculate the frequency-response characteristics of a single-pole, active low-pass filter network.
Optimum R and C Values for Filters Calculator	Standard op amps	Excel	This Excel spreadsheet uses the time-constant formula to calculate the optimum R and C values for filters at a given frequency.
Analog Filter Op Amp Design	General electronics	Web-based	This utility offers three different levels of analog filter design using operational amplifiers: • "What type of filter do I need?", a guide for beginners. • The Filter Wizard, for less experienced designers. • The Filter Expert, for more experienced designers.

Table 2. Analog design tools available on the Web for Power Management
To find the tools below, go to www.ti.com/sc/analogmsp and, under POWER MANAGEMENT, click on Engineer Design Utilities.

APPLICATION NAME	SUPPORTED PRODUCTS	ENVIRONMENT	DESCRIPTION
SWIFT Designer	TPS546xx, buck converters	Windows	The SWIFT family of low-input-voltage, high-output-current, synchronous-buck PWM converters (TPS546xx) integrates all required active components including high- and low-side N-channel power MOSFET switches.
Buck Power Converter Design	General buck switch-mode converter	Excel	This spreadsheet will calculate the values of the power-stage components for a buck switch-mode power converter. The user needs to fill in only the input voltage, output voltage, load current, switching frequency, forward voltage drop of the rectifier, and the on resistance of the switch.
Error Amp Impedance	Standard op amps	Excel	A typical operational amplifier load is equivalent to a resistor and two capacitors. This spreadsheet calculates this load impedance at any given frequency.
Hysteretic Frequency	Any TI hysteretic controller	Excel	This spreadsheet calculates the operating frequency of TI's hysteretic power supply controllers. It includes both the simplified and accurate models.
Low Dropout (LDO) Regulators	TPS7x01 family of adjustable low-dropout regulators	Excel	This file calculates the operating parameters for the Texas Instruments TPS7x01 family of adjustable low-dropout regulators. The closest 1% resistor values are calculated as well as the maximum power dissipation, worst-case output voltages, Power Good trip voltages, and maximum operating temperature for free-air and case temperature for the given operating conditions.
TPS6734 Divider	TPS6734 fixed 12-V boost converter	Excel	This spreadsheet shows the effects of an external resistor divider network on the TPS6734 fixed 12-V boost converter.
Via Calculator	General electronics	Excel	This spreadsheet calculates the capacitance; inductance; and dc and ac impedance of a via on FR-4-type PC boards.
Wire Impedance Calculator	General electronics	Web-based	This tool calculates the ac and dc resistance of a wire of a given diameter at a particular frequency.
Temperature Rise Calculator	General electronics	Web-based	This tool calculates the internal temperature rise of a cylindrical electrolytic capacitor, given the RMS ripple current, the ESR of the capacitor, and the length and diameter of the capacitor.
Hold Up Capacitance Calculator	General electronics	Web-based	This calculator determines the capacitance required to hold up a power supply (or support some average load), given an initial voltage, final voltage, load (in watts), and required hold-up time.
Trace Calculator	General electronics	Web-based	This spreadsheet calculates the dc resistance, voltage drop, and power loss in PC-board trace. It also calculates the dc and ac impedance, voltage drop, and power loss in circular wire of any length.
RC Divider	General electronics	Excel	This spreadsheet calculates and plots the frequency response of an RC divider.
Calculator for TL431	TL431 family of devices	Excel	This spreadsheet calculates all component parameters for any desired output voltage for the TL431 family of devices. It includes limits for each device. Resistor values are calculated to the nearest 1% value.
TLC555 Design Calculator	TLC555 timer	Excel	This spreadsheet calculates the complete design of a TLC555 timer-based astable circuit, given the timing capacitance, on time, and desired duty cycle. Resistor values are calculated to the nearest 1% value.

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