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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as “how-to” instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following product categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Because this book is limited in size, readers should refer to more detailed technical information, which can be found on TI’s product-specific websites listed at the end of each article.

The design and performance of a precision voltage reference circuit for 14-bit and 16-bit A-to-D and D-to-A converters

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and Doug Moore, *Managing Director, Thaler Corp., Tucson, Arizona*

Introduction

The first paper on this topic appeared in the November 1999 issue of *Analog Applications Journal* (www.ti.com/sc/analogapps). It introduced the VRE3050 precision voltage reference and described the criteria for selecting a reference for data converters that operate over the industrial temperature range and the importance of the external voltage reference for high-resolution data converters in general.

This article describes the performance and design of a complete precision voltage reference circuit consisting of the VRE3050 precision reference, the MAX1682 charge pump voltage doubler, and the THS1240 ADC evaluation board.* The MAX1682 provides a stable +10 V for the VRE3050 reference. The output from the VRE3050 is divided down to provide a 2-V differential signal to the THS1240 converter.

The circuit is designed to provide an adjustable external precision voltage reference to minimize voltage drift and to operate over the commercial (0°C to +70°C) temperature range. Such a circuit has been used to provide an adjustable external voltage reference for 12-bit, 14-bit, and 16-bit communication data converters.

High-resolution A-to-D and D-to-A converters rely on an external precision voltage reference to establish absolute measurement accuracy. Any reference error undermines the overall system accuracy; thus, the external voltage reference must provide accurately set constant voltage, independent of load changes, temperature, input supply voltage, and time.

The circuitry

The complete external voltage reference circuit is shown in Figure 1. Designed for simplicity, the circuit is comprised of a 2x charge pump (MAX1682), a precision voltage reference (VRE3050), and an adjustable resistor divider. The circuit was evaluated on the THS1240 evaluation board.

The MAX1682 is suitable for use in low-voltage, low-current applications where power management is a concern. The MAX1682 can deliver 30 mA of output current with a voltage drop of only 600 mV. The device output appears at pin 2 of U1 (see Figure 1). For an input of +5 VDC the

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*The THS1240EVM will be available 3Q00. The THS1050EVM or THS1060EVM may be used as an equivalent evaluation board.

Figure 1. A practical adjustable voltage reference circuit for 12-bit, 14-bit, and 16-bit data converters

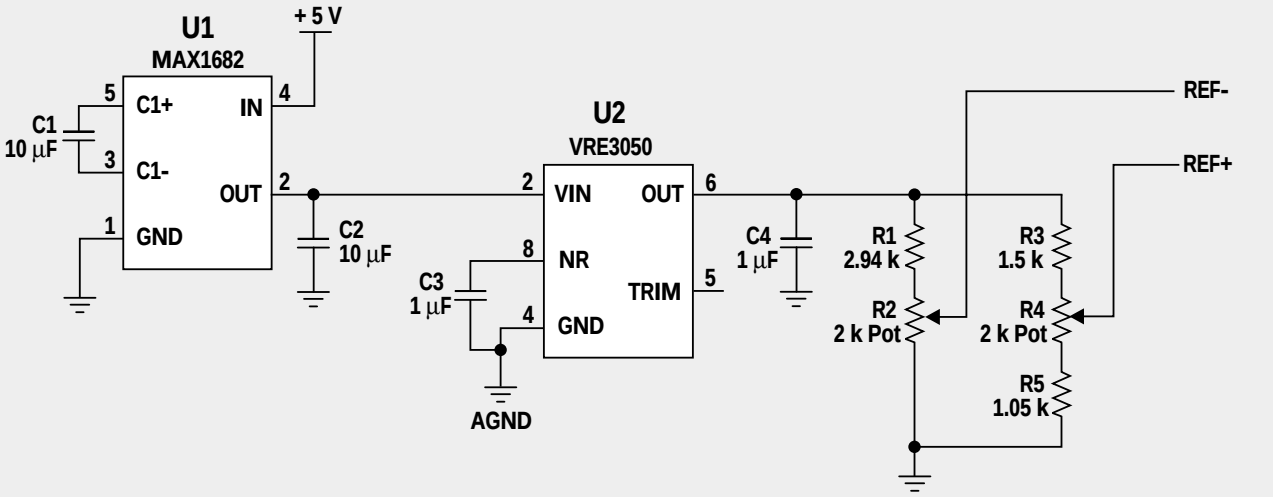
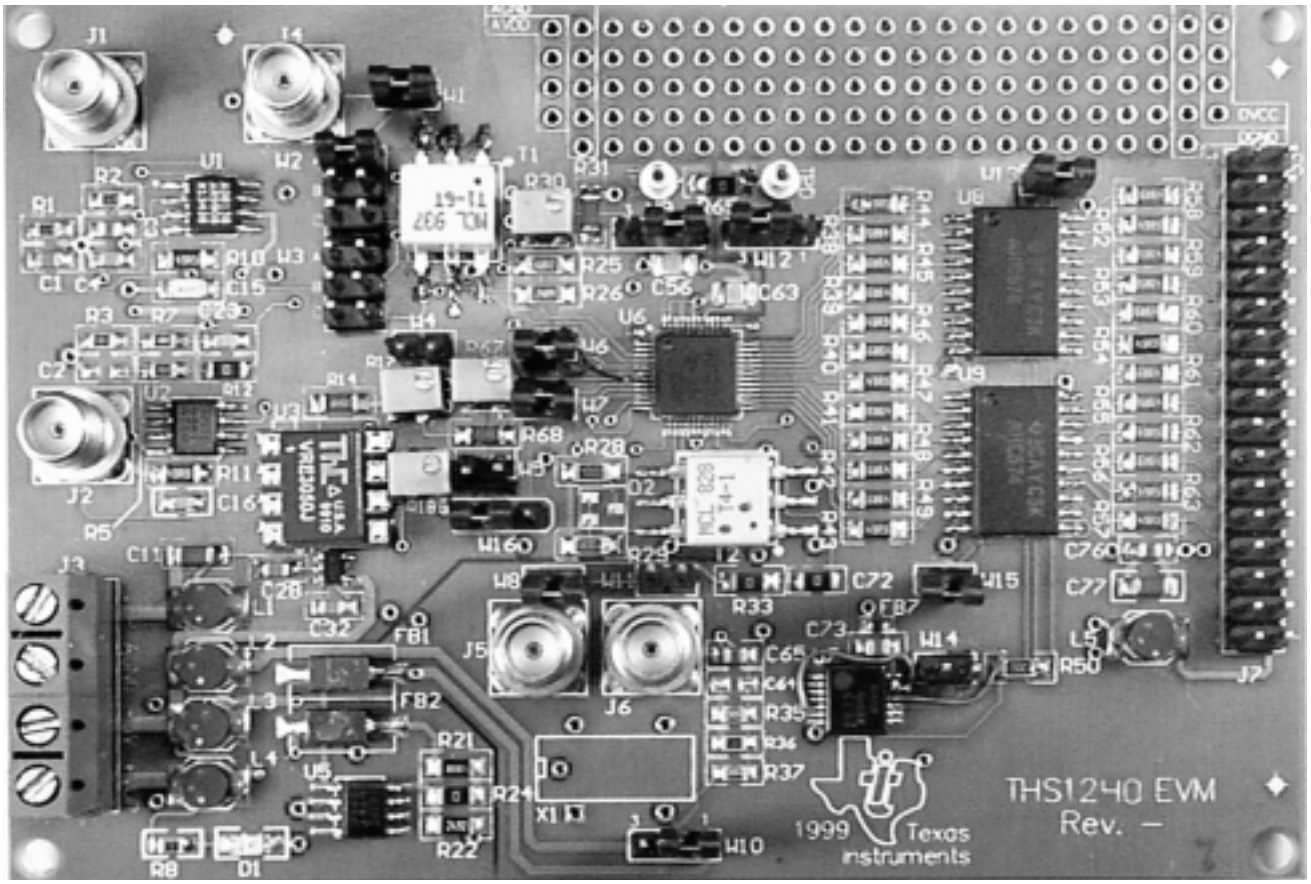


Figure 2. THS1240 evaluation module



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chip's output is +10 VDC. Capacitors C1 and C2 need some consideration inasmuch as the values need to be large enough to reduce noise at both the input and output of the device. A 10-µF capacitor was used in the circuit. Capacitor C2 must be rated for >10 V. The MAX1682 output is used to supply the DC input voltage required by the VRE3050. Component C3, connected to U2 pin 8, is recommended for high-frequency (10-Hz to 10-kHz) noise reduction. The VRE3050 has a low 3-μV_{p-p} noise from 0.1 to 10 Hz. Capacitor C4 was added to the VRE3050 output pin to reduce the high-frequency system noise at the input to the THS1240.

The new generation of A-to-D and D-to-A converters requires an external ΔV_{ref} that ranges from 1.2 V to 3.5 V. The common voltage references available on the market are 1.2 V, 2.5 V, 4.096 V, and 5 V. Intermediate voltages are often generated from a standard reference voltage using resistor networks. The resistors used are the surface-mount chip type (CR1206-8W) that have a 1% tolerance and a TC of 100 ppm/°C. This design uses potentiometers to make the V_{ref} adjustable. Potentiometers R2 and R4 are used to set REF– and REF+ voltages, respectively. The potentiometer's temperature coefficient (TC) will affect the value of both REF+ and REF– ; therefore, the potentiometers must be chosen from the same series and manufacturer. The TC for the Bourns 3214 series potentiometers used in this circuit is specified at 100 ppm/°C max.

Test set-up

The printed circuit board (PCB) used to evaluate the reference circuit is shown in Figure 2. It is the THS1240 evaluation module (EVM) PCB populated with the reference circuit components and a 2-pin power supply connector used for connecting +5 VDC directly to the MAX1682. The PCB is constructed from FR4 material with separate layers for power and ground planes. The power plane layer is split into an analog and a digital power section and the ground plane layer is also split into an analog and a digital ground section. Both analog and digital grounds are tied together at one single point on the ground plane layer. This helps to minimize switching noise interactions between the digital and analog circuits on the THS1240 EVM.

The measurement circuit for the voltages, set-up, and adaptation of the THS1240 evaluation module PCB is shown in Figure 3.

The THS1240 evaluation board was connected to a DC power supply, then placed in a temperature-controlled oven (±0.5°C). A Thaler ACE100/ADC150 24-bit A/D evaluation board was used to monitor the voltage on pin 6 of the VRE3050 reference and pins REF– and REF+ on the THS1240 board. The grounds were tied to a common point to minimize ground loops. The oven was programmed for the commercial temperature range with data collection points at 70°C, 25°C, and 0°C and the industrial temperature range with data collection points at 85°C, 25°C, and –40°C. The data was collected and stored to a file for analysis.

PCB layout

Poor printed circuit board layout (i.e., ground loops) can adversely affect the performance of the reference as well as the output voltage, noise, and thermal performance of the device. Inherent stress in the PCB can also be transferred to the components and can affect the performance of the reference and the overall accuracy of the system.

Results

The output voltages, associated temperatures, and temperature coefficients are summarized in Tables 1 and 2. The temperature coefficient is calculated using the box method.

$$TC = \left[\frac{V_{max} - V_{min}}{V_{nominal} \times (T_{max} - T_{min})} \right] \times 10^6$$

Nominal values of 5 V for the Thaler reference and 2 V for the THS1240 EVM outputs were used. The VRE3050 reference has a TC of 0.5 ppm/°C, which is within the datasheet specification for a J grade device. The output voltage at REF– and REF+ includes the TC error from the trim pot and the resistors, which are each rated at 100 ppm/°C max. The actual drift was ~20 ppm/°C for each of the THS1240 EVM outputs with respect to 2 V. The 2-V differential voltage has a TC of only 5 to 6 ppm/°C. For a 12-bit converter over the commercial temperature

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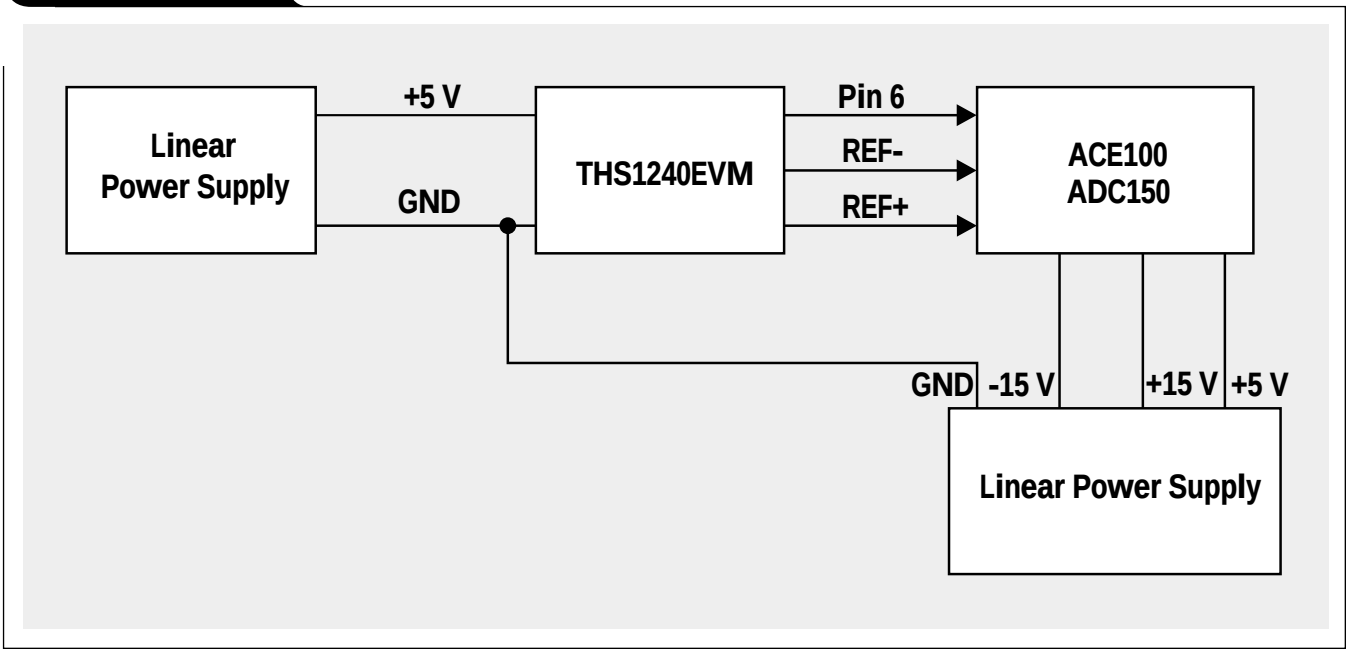
Table 1. Test results for commercial output voltages

OUTPUT VOLTAGE	0°C	25°C	70°C	TC 0 to 70°C
Thaler reference—VRE3050	4.999763 V	4.999587 V	4.999769 V	0.5 ppm/°C
REF+ from THS1240 EVM	2.996484 V	2.995324 V	2.994505 V	14 ppm/°C
REF– from THS1240 EVM	0.992623 V	0.991307 V	0.989975 V	19 ppm/°C
ΔV_{ref} (REF+ to REF–)	2.003861 V	2.004017 V	2.004530 V	5 ppm/°C

Table 2. Test results for industrial output voltages

OUTPUT VOLTAGE	–40°C	25°C	85°C	TC –40 to 85°C
Thaler reference—VRE3050	4.999922 V	4.999610 V	4.999808 V	0.5 ppm/°C
REF+ from THS1240 EVM	2.998485 V	2.995123 V	2.993548 V	20 ppm/°C
REF– from THS1240 EVM	0.998929 V	0.996100 V	0.992546 V	26 ppm/°C
ΔV_{ref} (REF+ to REF–)	1.999556 V	1.999023 V	2.001002 V	6 ppm/°C

Figure 3. Test set-up



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range, that equates to ~1 LSB and ~4 LSB over the industrial temperature range.

The thermal hysteresis of the reference circuit design was also evaluated, and the results are summarized in Table 3. Thermal hysteresis was calculated on the room readings after a temperature excursion to 85°C. The VRE3050J had 2.4 ppm of hysteresis over the 60°C temperature excursion, and the ΔV between V+ and V– had 14 ppm of hysteresis.

Summary

An external precision voltage reference is the best way to obtain a very stable and adjustable precise V_{ref} for high-resolution A-to-D or D-to-A converters. The proposed circuit with a variable voltage reference is adequate for circuits that require a variable reference over the commercial operating temperature range. When higher than 12-bit accuracy is required in a system over the industrial temperature range, the trim potentiometers and resistor dividers should be removed from the system. Thaler Corporation offers custom output voltages on their high-precision references.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. Maxim Corp., MAX1682/1683 Switched-Capacitor Voltage Doubler Datasheet.	—
2. THS1240, 12-bit, 40-MSPS, IF Sampling Communications A/D Converter Datasheet	slas279
3. Thaler Corp., Evaluation Board ACE100 Datasheet.	—
4. Thaler Corp., Precision Reference VRE3050 Datasheet.	—

Related Web site

www.ti.com/sc/docs/products/analog/ths1240.html
www.ti.com/sc/docs/products/analog/ths1060.html
www.ti.com/sc/docs/products/analog/ths1050.html
www.ti.com/sc/docs/apps/analog/data_converters.html
www.ti.com/sc/docs/products/msp/dataconv/index.htm
www.ti.com/sc/docs/tools/analog/dataconverterdevelopmentboards.html

Table 3. Thermal hysteresis

OUTPUT VOLTAGE	25°C	85°C	25°C	HYSTERESIS
Thaler reference—VRE3050	4.999610 V	4.999808 V	4.999622 V	2.4 ppm
ΔV_{ref} (REF+ to REF–)	1.999023 V	2.001002 V	1.999051 V	14 ppm

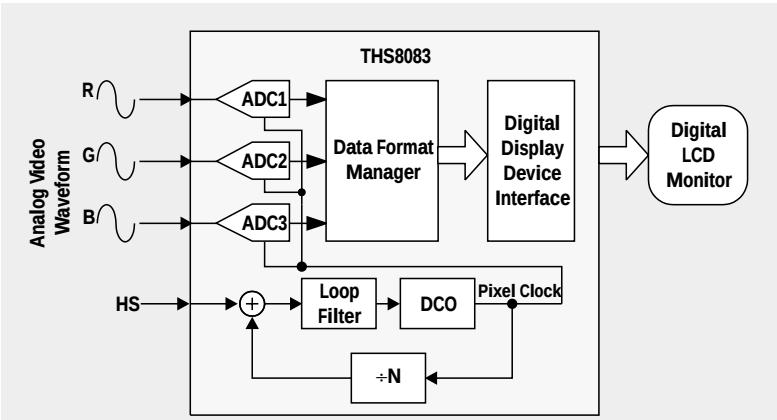
Introduction to phase-locked loop system modeling

By Wen Li, *Senior System Engineer, Advanced Analog Product Group*
and Jason Meiners, *Design Manager, Mixed-Signal Product Group*

Introduction

Phase-locked loops (PLLs) are one of the basic building blocks in modern electronic systems. They have been widely used in communications, multimedia and many other applications. The theory and mathematical models used to describe PLLs are of two types: linear and nonlinear. Nonlinear theory is often complicated and difficult to deal with in real-world designs. Analog PLLs have been well modeled by linear control theory. Starting from a well-defined model in the continuous-time domain, this article introduces a modeling and design method for a digital PLL based on linear control theory. It has been proved that a linear model is accurate enough for most electronic applications as long as certain conditions are met. Figure 1 shows a block diagram of the Texas Instruments THS8083 device that targets LCD monitor and digital TV applications. The task of the PLLs in these devices is to recover the pixel clock based on input reference HS (horizontal sync). This PLL has been accurately modeled by the method introduced in this article.

Figure 1. A typical PLL application



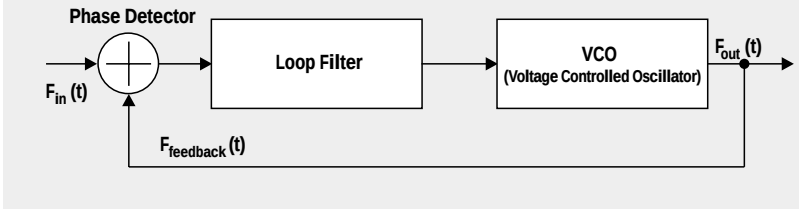
From a PLL system point of view, the DCO has the same function as the VCO, but it is implemented in the digital domain, so the output frequency of the DCO is a function of the input digital value.

A linear PLL model in the continuous-time domain (S-domain)

From Figure 2, the PLL can be easily recognized as a feedback control system. This system consists of the following components.

- Phase detector—detects the phase difference between the input signal $F_{in}(t)$ and the feedback signal $F_{feedback}(t)$
- Loop filter—typically, a filter with low-pass characterization
- VCO—voltage-controlled oscillator whose output frequency is a function of its input voltage

Figure 2. Functional block diagram of a typical PLL

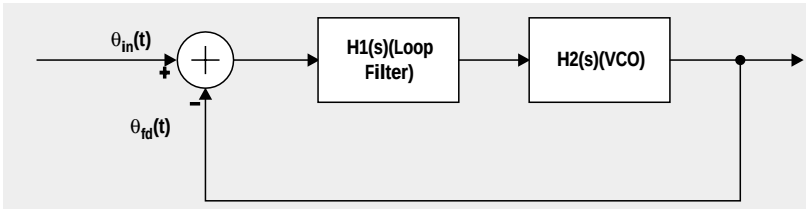


A linear model of the PLL in S-domain

Based on the condition that phase error is small, which can be expressed mathematically as $\sin(\theta) \approx \theta$, a PLL can be accurately described by a linear model. Figure 2 is a block diagram of a linear PLL model.

In Figure 3, $\theta_{in}(t)$ is the phase of the input signal, and $\theta_{fd}(t)$ is the phase of the feedback signal. Since the system is described in the continuous-time

Figure 3. A linear model of the PLL in S-domain



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domain, the transfer functions of each component are given out in Laplace-transform format.

- Transfer function of loop filter:

$$H1(s) = \frac{G_{lp}}{G_{lp} + S} \quad (1)$$

- Transfer function of VCO:

$$H2(s) = \frac{G_{vco}}{S} \quad (2)$$

- Closed-loop transfer function of a PLL:

$$H_{cl}(s) = \frac{G_{lp}G_{vco}}{S^2 + G_{lp}S + G_{lp}G_{vco}} \quad (3)$$

Based on the closed-loop transfer function (Equation 3), one can see that this is a second-order system. In automatic control system theory, the transfer function of the second-order system often can be written as

$$H_s(S) = \frac{{\omega_n}^2}{S^2 + 2\zeta\omega_n S + {\omega_n}^2}, \quad (4)$$

where ω_n is defined as natural undamped frequency, and ζ is defined as damping ratio. This system is called a standard prototype second-order system.

Based on the transfer function of a second-order prototype system, a characteristic equation of the system is defined as

$$\Delta(s) = S^2 + 2\zeta\omega_n S + {\omega_n}^2 \quad (5)$$

By solving the roots of the characteristic equation, two poles of the system, S_0 and S_1, can be derived.

$$S_0 = -\zeta\omega_n + j\omega_n\sqrt{1-\zeta^2} = -\alpha + j\omega, \quad \text{and} \quad (6)$$

$$S_1 = -\zeta\omega_n - j\omega_n\sqrt{1-\zeta^2} = -\alpha - j\omega, \quad (7)$$

where α is defined as damping factor and ω is defined as damped frequency.

Based on Equations 6 and 7, as soon as ζ and ω_n of the system are given, the poles of a second-order prototype system can be determined. Those two parameters are usually used to specify performance requirements of a system. As a matter of fact, most transient-response performances of a system can be determined based on these two parameters. The following is a list of performance parameters defined based on ζ and ω_n. Derivations of these equations can be found in most control theory textbooks.[1]

Damping factor α:

$$\alpha = \zeta\omega_n \quad (8)$$

Damped frequency ω:

$$\omega = \omega_n\sqrt{1-\zeta^2} \quad (9)$$

Settling time:

$$t_s = \frac{4}{\zeta\omega_n} \quad (10)$$

Maximum overshoot time:

$$t_{max} = \frac{\pi}{\omega_n\sqrt{1-\zeta^2}} \quad (11)$$

Maximum overshoot:

$$M = 1 + e^{-\pi\zeta/\sqrt{1-\zeta^2}} \quad (12)$$

Maximum overshoot in percentage:

$$M_{pct} = 100e^{-\pi\zeta/\sqrt{1-\zeta^2}} \quad (13)$$

Until this point, a second-order system has been defined in S-domain, and this system will meet performance requirements specified by ζ and ω_n.

Modeling of digital PLL (DPLL) in the discrete-time domain (Z-domain)

So far, all the modeling shown is in the continuous-time domain. This model can be applied directly to an analog PLL. But the design requirement is for a digital PLL. Normally, the output responses of a discrete-time control system are also functions of continuous-time variable t. Therefore, the goal is to map the system that meets the time-response performance requirements specified by ζ and ω_n to a corresponding second-order model in Z-domain.

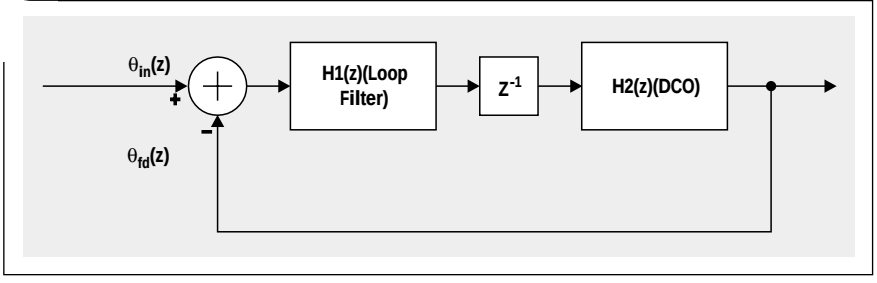
A linear model of PLL in discrete-time domain

A block diagram of the model of a DPLL is shown in Figure 4. Transfer functions of each component in the DPLL are in the Z-transfer format as follows.

- Transfer function of loop filter:

$$H1(Z) = \frac{aZ-1}{Z-1} \quad (14)$$

Figure 4. A DPLL model in the Z-domain



- Transfer function of a digital controlled oscillator (DCO):

$$H2(Z) = \frac{cZ}{Z-1} \quad \textbf{(15)}$$

- Z^{-1} is a delay unit, usually a register or register array.

With the block diagram and the transfer functions of components, a Linear Time Invariant (LTI) model can be developed to represent the PLL. The closed-loop transfer function of the DPLL model is then derived:

$$H(Z) = \frac{acZ - c}{Z^2 + (ac-2)Z + (1-c)} \quad \textbf{(16)}$$

Mapping the poles of a second-order system from S-domain to Z-domain

The transfer function of a second-order PLL in the Z-domain can be written in a general format as

$$H(z) = \frac{N(z)}{(Z-Z_1)(Z-Z_0)}, \quad \textbf{(17)}$$

where Z_0 and Z_1 are two poles of the system in Z-domain. Corresponding to the S-domain analysis, a characteristic equation of a discrete-time system is defined as

$$\Delta(z) = (Z-Z_1)(Z-Z_0) = Z^2 - (Z_1+Z_0)Z + Z_1Z_0 \quad \textbf{(18)}$$

C_1 and C_0 are defined as coefficients of the characteristic equation:

$$\begin{aligned} C_1 &= -(Z_1+Z_0) \\ C_0 &= Z_1Z_0 \end{aligned} \quad \textbf{(19)}$$

Then the characteristic equation can be written in the simplified format

$$\Delta(z) = Z^2 + C_1Z + C_0 \quad \textbf{(20)}$$

By definition of a discrete-time transformation,[2] two poles of this system in the Z-domain can be mapped from the poles in S-domain as

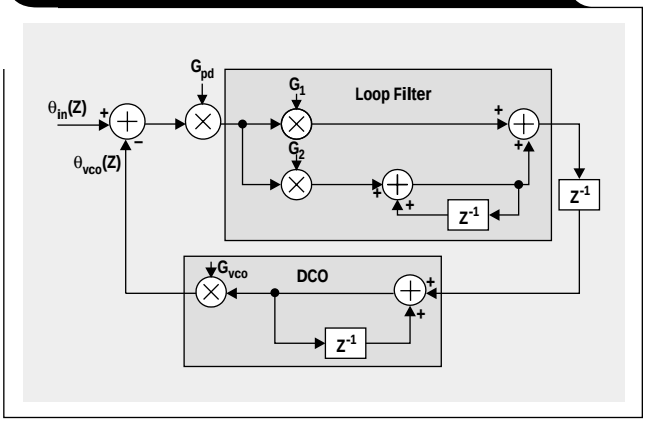
$$\begin{aligned} Z_0 &= e^{S_0T_s} = e^{\left(-\zeta\omega_nT_s + j\omega_nT_s\sqrt{1-\zeta^2}\right)} \text{ and} \\ Z_1 &= e^{S_1T_s} = e^{\left(-\zeta\omega_nT_s - j\omega_nT_s\sqrt{1-\zeta^2}\right)}, \end{aligned} \quad \textbf{(21)}$$

where T_s is the sampling period of the discrete system.

With the poles mapped in the Z-domain and Equation 19, coefficients C_0 and C_1 of the characteristic equation (Equation 20) can be derived in a format that is described by the parameters ζ and ω_n:

$$\begin{aligned} C_0 &= e^{-2\zeta\omega_nT_s} \\ C_1 &= -2e^{-\zeta\omega_nT_s}\cos\left(\omega_nT_s\sqrt{1-\zeta^2}\right) \end{aligned} \quad \textbf{(22)}$$

Figure 5. A completely implemented block diagram of a second-order DPLL system



Then a characteristic equation is derived by mapping the poles in a continuous-time domain system. Since the characteristic function will largely affect system transient responses, Equations 20 and 17 can determine the transfer function of a DPLL. The numerator of Equation 17 can be a constant scaling factor, or zeros can be introduced to tune the performance of the system. For example, if the DPLL adopts the architecture-based Equation 16, its transfer function will be determined as soon as the poles are mapped. The following section presents a completely implemented DPLL.

Implementation of a second-order DPLL

This section presents detailed information for implementing a completed DPLL system based on the previous analysis and model mapping results. An architecture diagram of a second-order DPLL system is presented in Figure 5. Based on this architecture, each basic building block is described.

- Loop filter—an IIR filter has been designed as the loop filter. H1(z) is its transfer function:

$$H1(z) = \frac{G_1 + G_2 - G_1Z^{-1}}{1-Z^{-1}}, \quad \textbf{(23)}$$

where G_1 and G_2 are the gains of the IIR filter.

- A digital-controlled VCO or a discrete-time oscillator (DTO) will have H2(z) as its transfer function:

$$H2(z) = \frac{G_{vco}}{1-Z^{-1}}, \quad \textbf{(24)}$$

where G_{vco} is the gain of the discrete VCO.

With these building blocks of the DPLL system, the closed-loop transfer function can be written as

$$H(z) = \frac{\theta_{vco}(z)}{\theta_{in}(z)} = \frac{H1(z)H2(z)Z^{-1}G_{pd}}{1+H1(z)H2(z)Z^{-1}G_{pd}}, \quad \textbf{(25)}$$

where G_{pd} is the gain of the phase detector.

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The expended format of this transfer function can be written as

$$H(z)=\frac{\theta_{vco}(z)}{\theta_{in}(z)}=\frac{(g1+g2)Z-g1}{Z^2+(g1+g2-2)Z+(1-g1)}, \quad \textbf{(26)}$$

where $g1 = G_{pd}G_{vco}G_1$ and $g2 = G_{pd}G_{vco}G_2$.

By comparing the characteristic equation $\Delta(z)$ of a DPLL (Equation 20), the following equation can be constructed:

$$C_0 = 1-g1$$
$$C_1 = g1+g2-2 \quad \textbf{(27)}$$

The g1 and g2 can be resolved based on Equations 27 and 22:

$$g1 = 1-e^{-2\zeta\omega_n T_s}$$
$$g2 = 1+e^{-2\zeta\omega_n T_s}-2e^{-\zeta\omega_n T_s}\cos\left(\omega_n T_s\sqrt{1-\zeta^2}\right) \quad \textbf{(28)}$$

With Equations 26 and 28, the model of a DPLL is completely derived.

Stability and steady-state error study of the DPLL system

Stability of the DPLL system

One mandatory requirement for designing DPLLs is that the DPLL system must be stable. Basically, the stable condition of a discrete-time system occurs when the roots of the characteristic equation are inside the unit circle $|Z| = 1$ in the Z-plane. Normally, after a system is implemented, numerical coefficients can be substituted into the characteristic equation. By solving the characteristic equation numerically, the positions of the poles can be found to determine if the system is stable; however, this method is technically difficult to use when implementing a DPLL, since numerical coefficients will not be available at the beginning of the process.

One of the most efficient methods for testing the stability of a discrete-time system is Jury's stability criterion.[1] This method can guide designs of a DPLL to converge to an optimized stable system quickly, without a large amount of numerical calculation and simulation. It can be applied directly to the second-order DPLL model to determine the stable condition. According to this criterion, the necessary and sufficient conditions are that the characteristic equation of a second-order system,

$$\Delta(Z) = a_2Z^2 + a_1Z + a_0 = 0, \quad \textbf{(29)}$$

should meet the following conditions in order to have no roots on or outside the unit circle:

$\Delta(1) > 0$,
$\Delta(-1) > 0$, and
$|a_0| < a_2$

Applying these conditions to the denominator of Equation 26, stable condition ranges of this DPLL architecture can be derived:

$$0 < g1 < 2 \quad \textbf{(30)}$$

$$0 < g2 < 4 \quad \textbf{(31)}$$

Steady-state error analysis of the DPLL

A steady-state error analysis of a DPLL is extremely important in PLL design. Now that a stable system has been described, the steady-state error of phase and frequency of the DPLL will be studied. It will be proven that both the phase and frequency error of this DPLL system will be zero when the system reaches its steady state.

Phase error analysis

Assume that the phase of the input signal has a step change. In the time domain, step changing of the phase of the input signal can be described by the step function

$$\Theta in(t) = \Delta\Theta \times u(t) \quad \textbf{(32)}$$

Here, $\Delta\Theta$ is the constant value by which the input signal phase jumped. Applying the Z-transform to Equation 32 yields

$$\Theta in(Z) = \frac{\Delta\Theta \times Z}{Z-1} \quad \textbf{(33)}$$

Based on the linear model, the output-response function of the DPLL for a phase-step input can be written as

$$\Theta fd(z) = H(Z) \times \Theta in(Z)$$
$$= \frac{\Delta\Theta \times Z(acZ-c)}{(Z-1)[Z^2+(ac-2)Z+(1-c)]} \quad \textbf{(34)}$$

Based on Equation 34, a numerical analysis can be carried out by using an existing software tool such as MATLAB. In this way, the steady-state error of an implemented DPLL system can be observed. The focus is on the general analytical results.

Assuming E(Z) is the phase-error function, by definition E(Z) can be written as

$$E(Z) = \Theta in(Z) - \Theta fd(Z) \quad \textbf{(35)}$$

Substituting Equation 34 into Equation 35 produces

$$E(Z) = [1-H(Z)]\Theta in(Z) \quad \textbf{(36)}$$

Substituting Equations 33 and 16 into Equation 36, the phase-error function is written as

$$E(Z) = \frac{\Delta\Theta Z(Z-1)}{Z^2+(ac-2)Z+(1-c)} \quad \textbf{(37)}$$

According to the Final-Value Theorem,

$$\lim_{k\to\infty} e(kT) = \lim_{z\to 1}(1-Z^{-1})E(Z) \quad \textbf{(38)}$$

Based on this theorem, the steady-state error, which is the final value of e(kT) in the time domain, can be derived. The condition for using the Final-Value Theorem is that the function $(1 - Z^{-1})E(Z)$ has no poles on or outside the unit circle $|Z| = 1$ in the Z-plane. The detailed method for meeting this condition has already been established.

Substituting Equation 37 into Equation 38 yields

$$\lim_{k\to\infty} e(kT) = \lim_{z\to 1} \frac{\Delta\Theta Z(Z-1)}{Z^2+(ac-2)Z+(1-c)} = 0 \qquad \textbf{(39)}$$

Conclusion: When the phase of the input signal s makes a step-jump, the phase error of this DPLL eventually will be eliminated by the closed-loop system.

Frequency error analysis

Given an input signal, assuming t = 0, its frequency jumps from $\omega 0$ to $\omega 1$, and let $\Delta\omega = \omega 1 - \omega 0$. The input phase can be written as

$$\Theta in(t) = \Delta\omega \times t \times U(t) \qquad \textbf{(40)}$$

Applying the Z-transform to Equation 40 to transfer it to Z-domain yields

$$\Theta in(Z) = \frac{\Delta\omega TZ}{(Z-1)^2} \qquad \textbf{(41)}$$

Substituting Equations 41 and 16 into Equation 36, the frequency-error function is derived as follows:

$$E(Z) = \frac{\Delta\omega TZ}{Z^2+(ac-2)Z+(1-c)} \qquad \textbf{(42)}$$

The Final-Value Theorem is applied to Equation 42 to get the steady-state error in time domain:

$$\lim_{k\to\infty} e(kT) = \lim_{z\to 1}(1-Z^{-1})E(Z)$$

$$= \lim_{z\to 1} \frac{\Delta\omega T(Z-1)}{Z^2+(ac-2)Z+(1-c)} = 0 \qquad \textbf{(43)}$$

Conclusion: When the frequency of an input signal has a step jump, the phase error of the DPLL eventually will be eliminated by the closed-loop system.

A design example

Following are a real design example and the simulation/ measuring results of the system.

Design requirements:

- Design a digital PLL that can recover the pixel clock of a PC graphics VGA output signal.
- The frequency of horizontal synchronization signal HS of VGA is f_s = 60023 Hz, T_s = 0.00001666s.
- The relationship between a period of the pixel clock T_p and a period of horizontal sync T_s is $T_s = 1312T_p$.
- PLL locking time is < 15 ms.
- One overshoot occurs during the locking process.

Based on these requirements, the following performance parameters can be determined:

$\zeta = 0.707$
$\omega_n = 2\pi 100$ rad/s
f_s = 60023 Hz, T_s = 0.00001666s

Based on these parameters, C_0, C_1, g1, and g2 can be calculated by using Equations 22 and 28:

$C_0 = 0.9853$
$C_1 = -1.9852$
g1 = 0.0147
g2 = 0.0001

The transfer function of the DPLL that meets the performance specification can be constructed:

$$H(z) = \frac{0.0148Z - 0.0147}{Z^2 - 1.9852Z + 0.9853} \qquad \textbf{(44)}$$

Based on this Z-domain model, the DPLL system performance can be simulated at system level. Figures 6 and 7 are simulation results based on this model.

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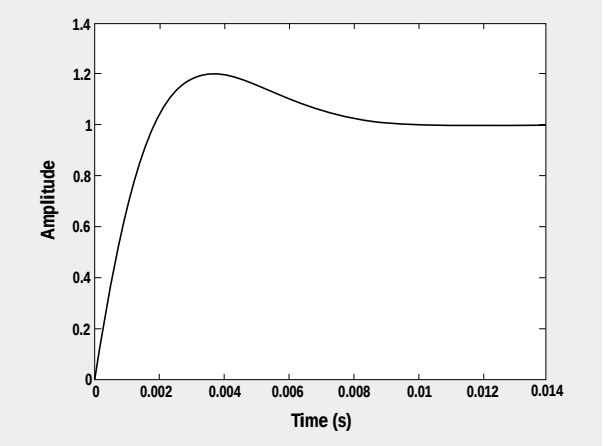
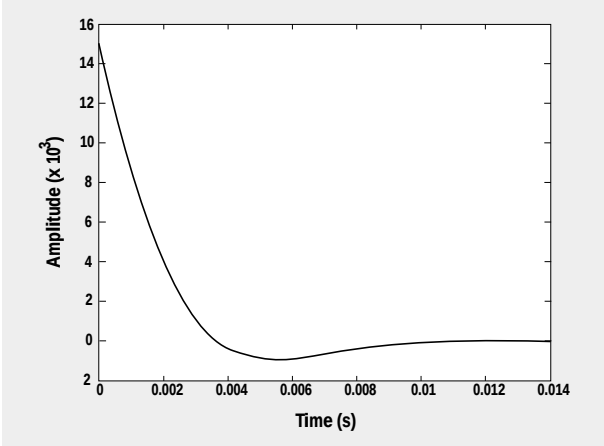
Figure 6. Step response of the DPLL system



1. Step function input response of the model describes the behavior of the system when the input signal phase is a step function. It also proves that the system is stable.

Figure 7. Impulse input response of the DPLL system



2. Impulse function input response of the model describes the behavior of the system when the input signal has a phase impulse error. It proves that the stable error of the system is zero.

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Physically, this DPLL is implemented in the following way:

- Phase detector—a high-speed counter to sample the input signal and calculate the phase error
- Loop filter—a digital IIR filter
- DCO—a DDS (direct-digital-synthesis) oscillator. From a PLL system point of view, the DCO has the same function as the VCO, but it is implemented in digital domain, so the output frequency of the DCO is a function of the input digital value.

References

1. Benjamin C. Kuo, *Automatic Control Systems*.
2. Alan V. Oppenheim and Ronald W. Schafer, *Discrete-Time Signal Processing*.
3. John L. Stensby, *Phase-Locked Loops, Theory and Applications*.

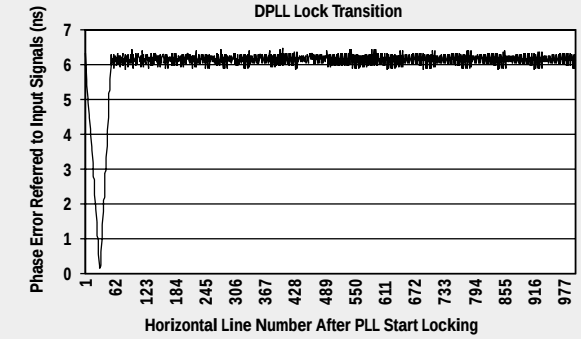
Related Web sites

www.ti.com/sc/docs/products/msp/dataconv/index.htm

Get product data sheets at:

www.ti.com/sc/docs/products/analog/ths8083.html

Figure 8. DPLL lock process based on a silicon-implemented DPLL



3. Silicon-implemented DPLL based on the Equation 32 model. It shows gate-level simulation/measuring results for a phase-locking process.

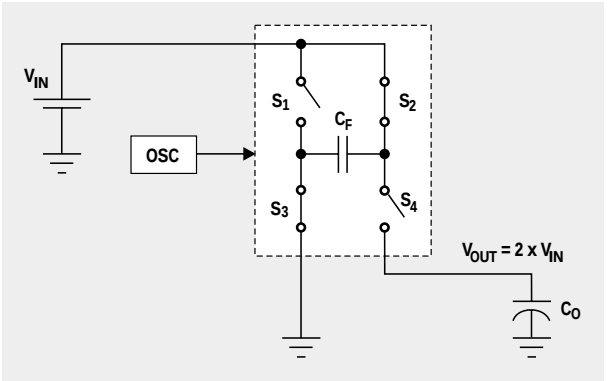
Simple design of an ultra-low-ripple DC/DC boost converter with TPS60100 charge pump

By Brigitte Kormann, *Field Application Engineer, Power Management*
and Jim Pelfrey, *Engineering Technician, Advanced Analog Products*

Introduction

Battery-powered equipment uses DC/DC step-up converters to generate supply voltages for internal circuits that require higher voltages than the available battery voltage. These can be inductive or capacitive converters. Inductive step-up converters, also called boost converters, have a high efficiency over the entire input voltage range. Capacitive converters—i.e., charge pumps—provide a high efficiency over selected input voltage ranges. However, since their design doesn't require any knowledge of magnetics, charge pumps are easier to implement, reducing the design time to a minimum. Higher output currents can easily be attained by operating two charge pumps in parallel. Figure 1 shows the block diagram of a basic single-ended charge pump configured as a voltage doubler.

Figure 1. Basic charge pump (charge phase shown)



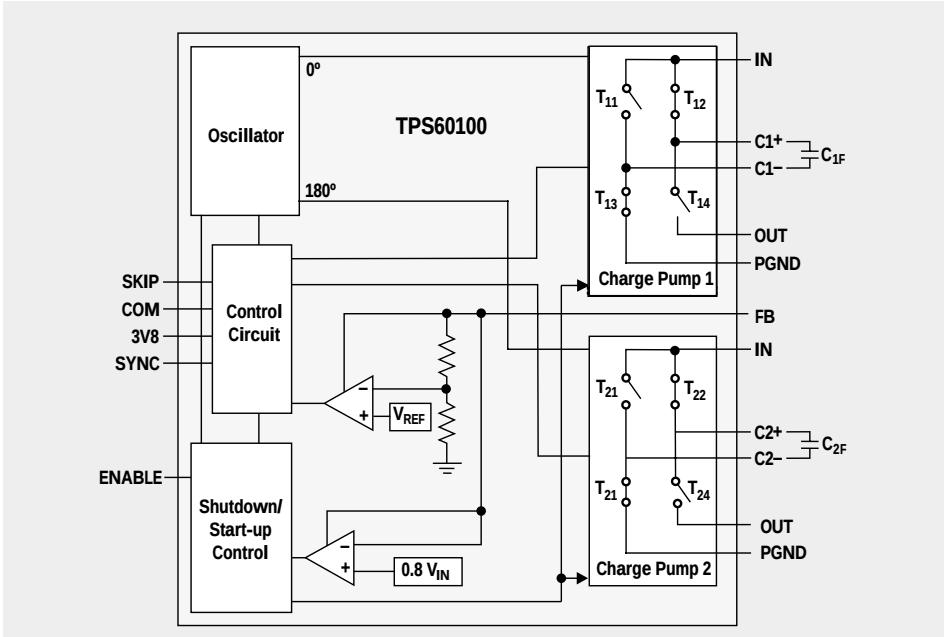
Charge pump operation in constant-frequency mode

The circuit operates in two phases, a charge phase and a transfer phase, which are controlled by an oscillator. During the charge phase the switches S_1 and S_4 are open, and switches S_2 and S_3 are closed. The battery charges the flying capacitor, C_F, to the input voltage level, V_{IN}. During the transfer phase, S_1 and S_4 are closed, and S_2 and S_3 are open. The voltage across C_F is in series with the input voltage. Both the battery and C_F are discharging into the output capacitor, C_O. The basic charge pump operates as a voltage doubler, generating an output voltage of

$$V_{OUT} = 2 \times V_{IN}$$

The new TPS60100 low-noise charge pump device from Texas Instruments contains two charge pumps that can operate in a complementary mode (push-pull mode) to minimize output ripple (Figure 2).

Figure 2. TPS60100 block diagram



While one charge pump operates in the charge phase to charge its transfer capacitor, C_{1F}, the other charge pump is in the transfer phase discharging C_{2F} into the output capacitor, C_O. The TPS60100 also provides a regulated 3.3-V output over a 1.8-V to 3.6-V input voltage range. The on-chip error amplifier senses output voltage variations via the feedback input, FB. The control circuit fed from the error amplifier controls the charge transferred to the output by driving the gates of MOSFET switches T_{11} and T_{21}, respectively (see Figure 2). When the output voltage drops, the gate drive

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increases, resulting in a larger charge being transferred to the output.

Although the TPS60100 provides a variety of programmable operating modes, the device needs to be set up for constant-frequency mode in push-pull operation to achieve the lowest output voltage ripple (see Figure 3).

Capacitor selection

For push-pull operation, a minimum of four capacitors is needed—one input capacitor (C_{IN}), two transfer capacitors (C_{1F}, C_{2F}), and one output capacitor (C_O). The following rules of thumb can be used to determine the values of the input and transfer capacitors with respect to the output capacitor:

$$C_O \geq 2 \times C_{IN} \quad \text{and} \quad C_O \geq 10 \times C_{xF}$$

In the constant-frequency mode, the value of C_O needs to be at least 22 µF or larger to ensure the stability of the regulation loop. With C_O = 22 µF, the recommended values for C_{IN} and C_{xF} are C_{IN} = 10 µF and C_{1F}, C_{2F} = 2.2 µF. To achieve a low output ripple, all capacitors should be ceramic capacitors because of their low equivalent series resistance (ESR). The low ESR of the transfer capacitors ensures minimum time constants when charging and discharging. The low ESR of C_{IN} and C_O is required to reduce the spikes that occur during the turnover from the transfer phase of one charge pump to that of the other. The lower the ESR of C_O, the lower is the output voltage ripple.

Figure 4 shows the AC output ripple of the circuit in Figure 3. The peak-to-peak ripple voltage is approximately 4 mV, while the spikes during the turnover of the transfer phases are reduced to 18 mV.

To further reduce the spikes, an L-C filter can be added to the output as shown in Figure 5. FB is connected to the filter output to avoid having the spikes enter the error amplifier. The series resistance of the inductor influences the regulation of the output voltage. A filter corner frequency of 2.3 MHz was chosen above the 300-kHz switching frequency to avoid loop stability issues.

Figure 3. Constant-frequency mode in push-pull operation for low output ripple

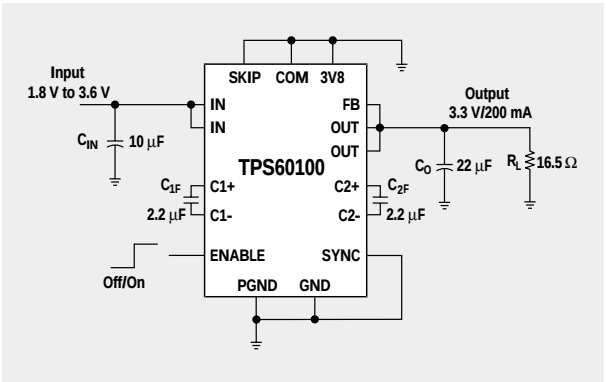


Figure 4. Output ripple without L-C filter

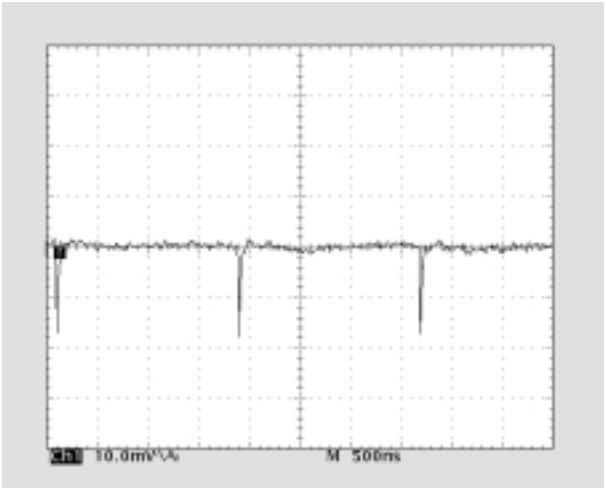


Figure 5. Output L-C filter reduces spikes and output ripples to an absolute minimum

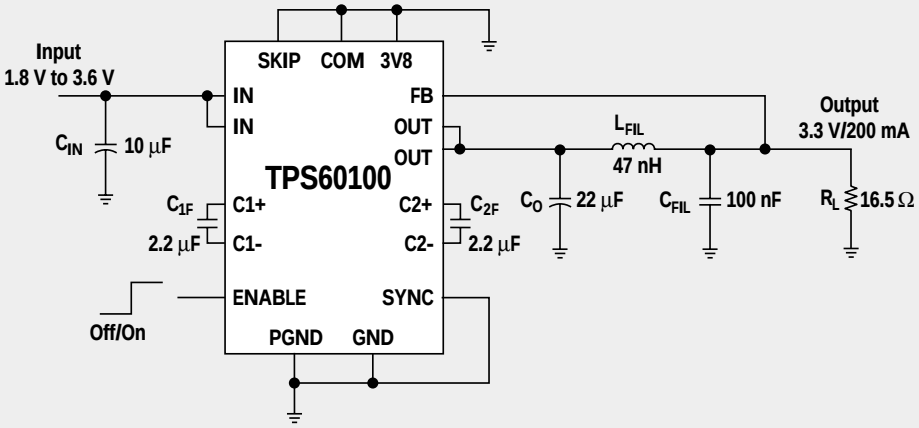


Figure 6 shows the same amount of AC output ripple; however, the spikes have been reduced to 6 mV by the L-C filter. All measurements were taken with a load resistance (R_L) of 16.5 Ω to draw the maximum output current of 200 mA.

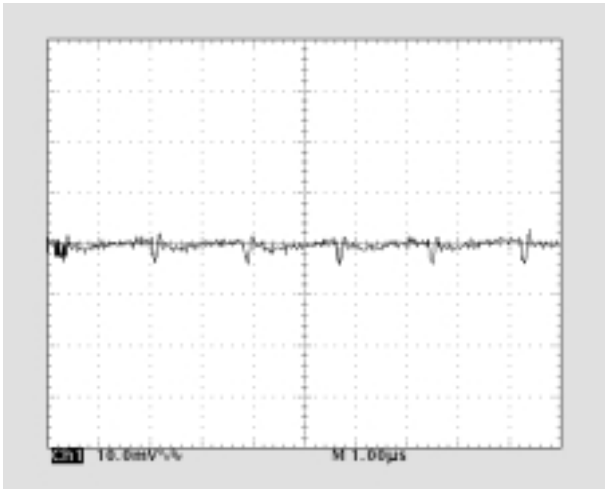
The reader should be aware that the energy dissipated in the series resistance of the inductor has to be delivered by the charge pump; therefore, with low input voltages and high output currents, the output voltage may go out of the voltage or temperature limits given in the data sheet.

The part numbers for the capacitors and the inductor are given in Table 1.

Table 1. Capacitor and inductor part numbers

PART	VALUE	PART NUMBER	MANUFACTURER
C_{IN}	10 µF/16 V	EMK325F106ZF (F/Y5V)	Taiyo Yuden
C_{1F}, C_{2F}	2.2 µF/16 V	LMK212BJ225MG-T	Taiyo Yuden
C_O	22 µF/10 V	LMK316F226ZL (F/Y5V)	Taiyo Yuden
L_{FIL}	47 nH/0.075 ΩΘ	1008G470GTE	Stetco
C_{FIL}	100 nF/16 V	EMK107BJ104AA (BJ/X7R)	Taiyo Yuden

Figure 6. Output ripple with L-C filter



For higher current requirements—i.e., 400 mA—two TPS60100s can operate in parallel as shown in Figure 7. Both devices, preferably operating in the same mode, share the output capacitor whose value doubles to 47 µF. Each device requires its own transfer capacitors and input capacitor.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

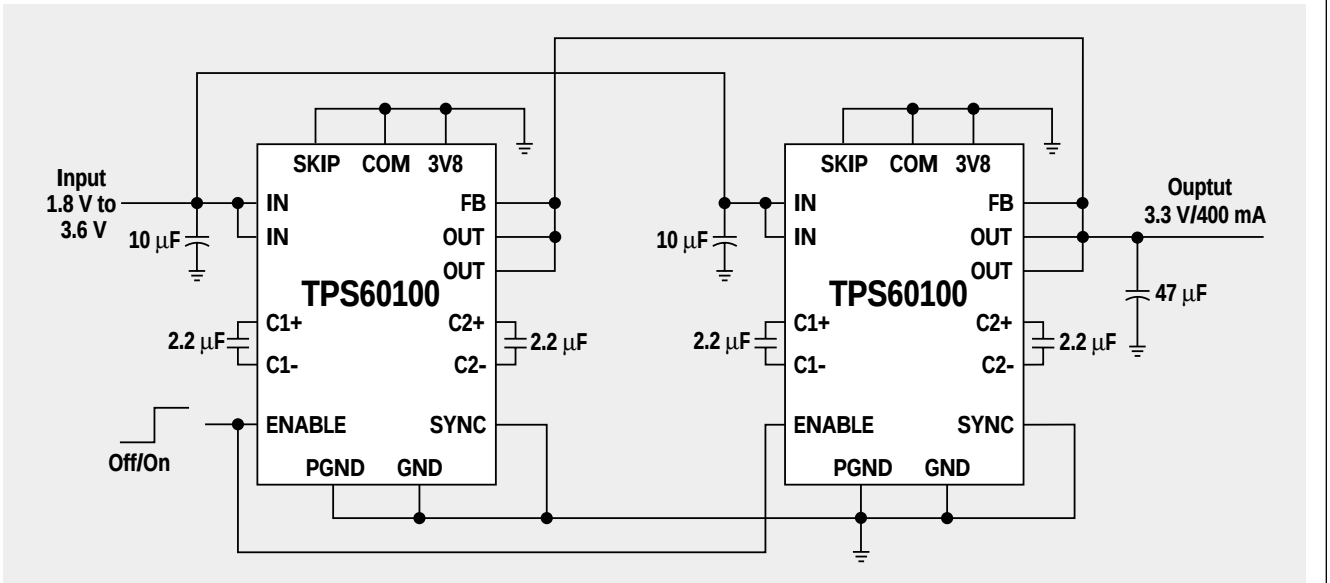
Document Title	TI Lit. #
1. TPS6010x/11x Application Report	slva070
2. TPS60100EVM-131 User's Guide	slvu016

Related Web sites

www.ti.com/sc/docs/products/msp/pwrmgmt/index.htm
www.ti.com/sc/docs/tools/analog/powermanagementdevelopmentboards.html

Get product data sheets at:
www.ti.com/sc/docs/products/analog/*device*.html
Replace *device* with tps60100, tps60101, tps60110, or tps60111

Figure 7. Two TPS60100 in parallel to provide 400-mA output current



Low-cost, minimum-size solution for powering future-generation Celeron™-type processors with peak currents up to 26 A

By Rais Miftakhutdinov, *System Engineering, Power Management Products*
and Philip Rogers, *System Engineering, Power Management Products*

Introduction

Next-generation microprocessors continue to challenge power system designers by increasing system power consumption. The latest design guidelines from Intel (Reference 4) require a maximum core current of up to 26 A for future processors in a PGA-370 package. The new TPS5211EVM-154 evaluation module with the TPS5211 hysteretic controller has been designed as a low-cost, minimum-size solution for this application. The TPS5211EVM-154 evaluation module includes a synchronous DC-DC buck converter, a socket for a PGA-370 microprocessor package with high-frequency decoupling capacitors, and a load-current transient tester. This module is a high-current modification of the TPS5210EVM-147 that is described in Reference 2. The DC-DC converter has a 5-V input and 1.65-V output and requires a 12-V, 40-mA supply voltage for the controller itself. The DC-DC converter occupies only 3.7 sq. in., while the temperature of the components does not exceed 80°C at room ambient temperature with a load current of 22 A. The transient characteristics of the module have been tested by Voltage Transient Test Tool v.2.0 from Intel and by an internal load-current transient tester at a peak load current of 26 A. A four-layer PCB, which is a very popular solution for a desktop main-board, was used in the module to get electrical and temperature conditions close to real conditions.

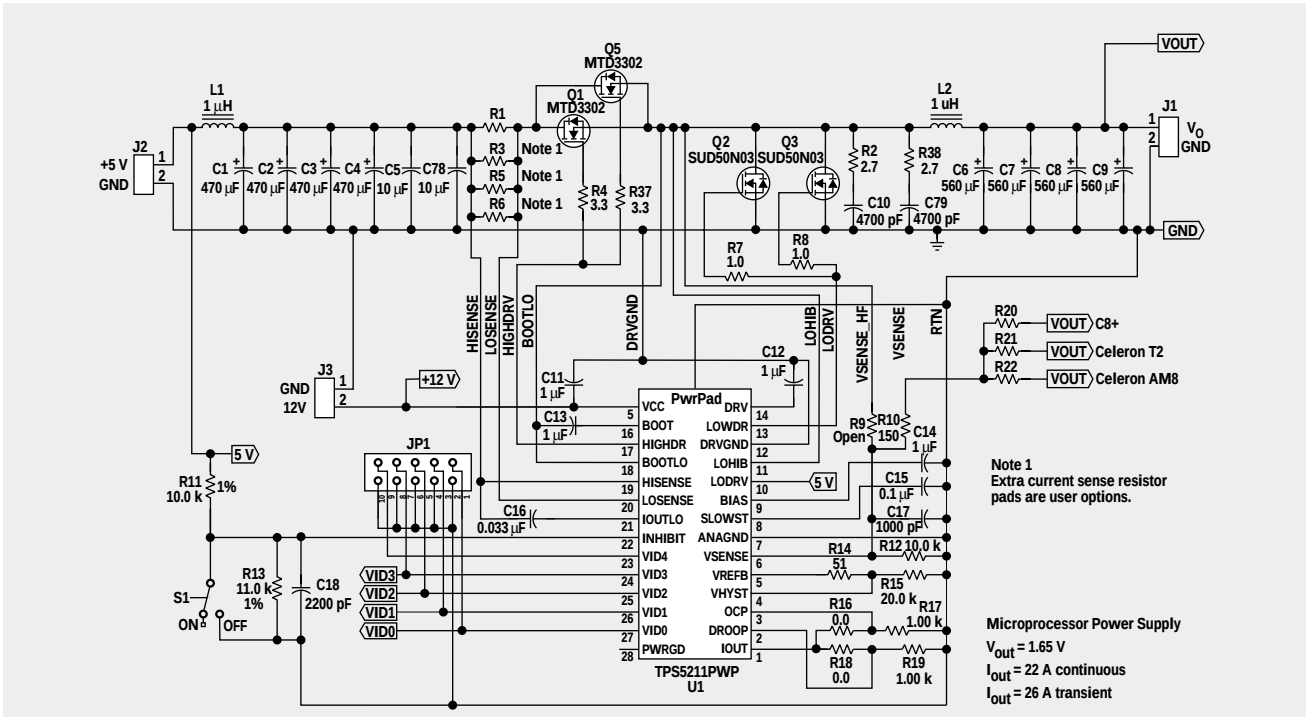
TPS5211EVM-154 evaluation module description

The TPS5211EVM-154 evaluation module (5.67″ x 3.19″ x 0.8″) includes three main parts:

- synchronous DC-DC buck converter,
- socket for a PGA-370 package, allowing use of the Transient Test Tool, and
- additional internal transient tester, which can be used if the Transient Test Tool is not available.

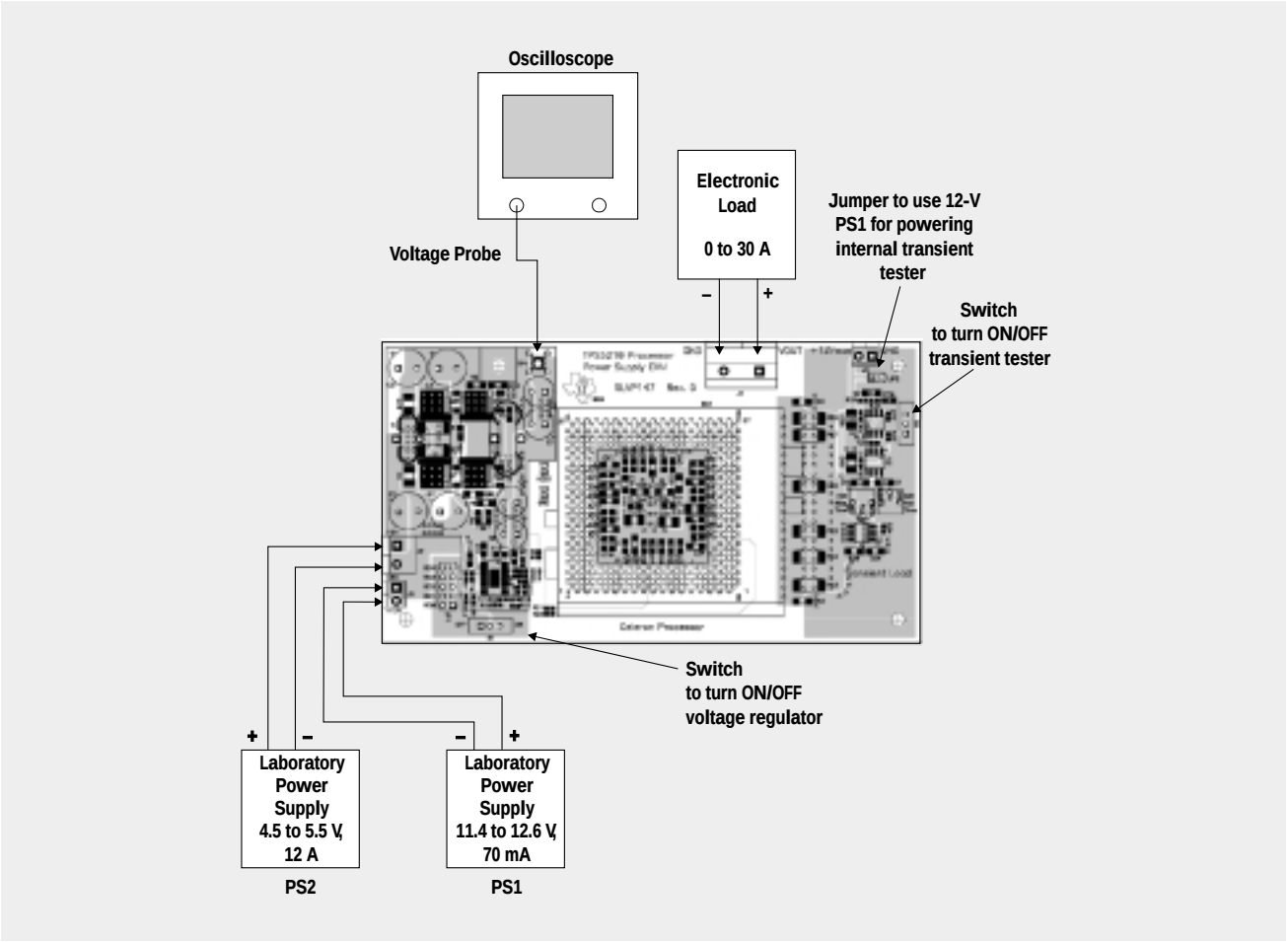
The schematic of the DC-DC synchronous buck converter is shown in Figure 1. The input filter includes four

Figure 1. Synchronous DC-DC buck converter schematic



For this application, R5, R6, and R12 are open; and R1 and R3 are 3 Mohm.

Figure 2. Test set-up for TPS5211EVM-154 EVM



10SP470M capacitors (C1–C4), 10-µF ceramic capacitors (C5, C78), and a 1-µH inductor (L1). The input capacitors can handle a total maximum RMS current as high as 18 A to increase the reliability of the power supply. The output filter has four OS-CON type capacitors 4SP560M (C6–C9) and a 1-µH inductor (L2). The fast hysteretic controller and active droop compensation reduce the number of capacitors while having a reliable margin for dynamic tolerance.

The power stage includes two 10-mohm high-side FETs (MTD3302) and two 7-mohm low-side FETs (SUD50N03) in DPAK packages (Q1, Q2, Q3, and Q5). The surface mount heat sinks from AAVID (part number 573100) have been used to improve temperature characteristics. All functions and features of the TPS5211 hysteretic controller are described in References 1–3.

Test results

The simplified block diagram of the test set-up and the EVM itself are shown in Figure 2.

All measurements were made at room temperature. The electrical and mechanical characteristics of the DC-DC converter are shown in Table 1.

Continued on next page

Table 1. Electrical and mechanical characteristics of the DC-DC converter

CHARACTERISTIC	MEASUREMENT
Input voltage	5 V ± 0.5 V
Input current	12 A max at V_{in} = 4.5 V and I_{out} = 27.5 A
V_{CC} voltage and current	12 V ± 0.6 V, 40 mA max
Nominal output voltage	1.65 V
DC and peak output current	22-A DC for temperature measurements and 26-A peak
Output voltage static tolerance	+0% and –3.65% including droop compensation
Output voltage dynamic tolerance	+3% and –4.8% at 25-A load-current step with 20-A/µs slew rate
Switching frequency	120 to 145 kHz
Efficiency	>84% at 22 A, 53.8% at 0.5 A
Occupied area	3.7 sq. in.

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Efficiency, power losses and temperature through components

The temperatures of components, the efficiency, and power losses were measured after 2 hours of operation when the temperatures of the PCB and components were stabilized. Results of these measurements are presented in Table 2 and Figure 3. The measurements were made at room temperature (22.8°C) with 5-V input voltage and 22-A load current. The cooling conditions were natural air convection in accordance with the specification. The two surface- mount heat sinks from AAVID (part number 573100) have been used for each pair of high- and low-side FETs to improve temperature characteristics. The maximum temperature rise was 56.7°C through the high-side FET, while the temperature rise of the PCB itself was 28.8°C. These are reasonable values because the real motherboard has a much larger cooling area for the components.

One can see that the temperatures of most components are very close to the PCB temperature, except for the FETs and output inductor.

Efficiency at 22.5-A load current is 83.7% and at 0.5 A is 53.8%. This exceeds the specification, which requires 80% and 40%, respectively. The maximum power losses at 22.5-A load current do not exceed 7.1 W.

The electrical requirements and cooling conditions might vary for different applications. To cover more potential applications, the power losses, efficiency, and temperature through high-side FETs have been investigated for different FETs and switching frequencies with and without heat sinks. Results of this investigation are presented in Table 3.

The switching frequency can be decreased using lower ESR (equivalent series resistance) capacitors like OS-CON type 4SP820M or by changing resistor R14 from 51 ohms to 75 ohms. In this case, the hysteresis window increases proportionally.

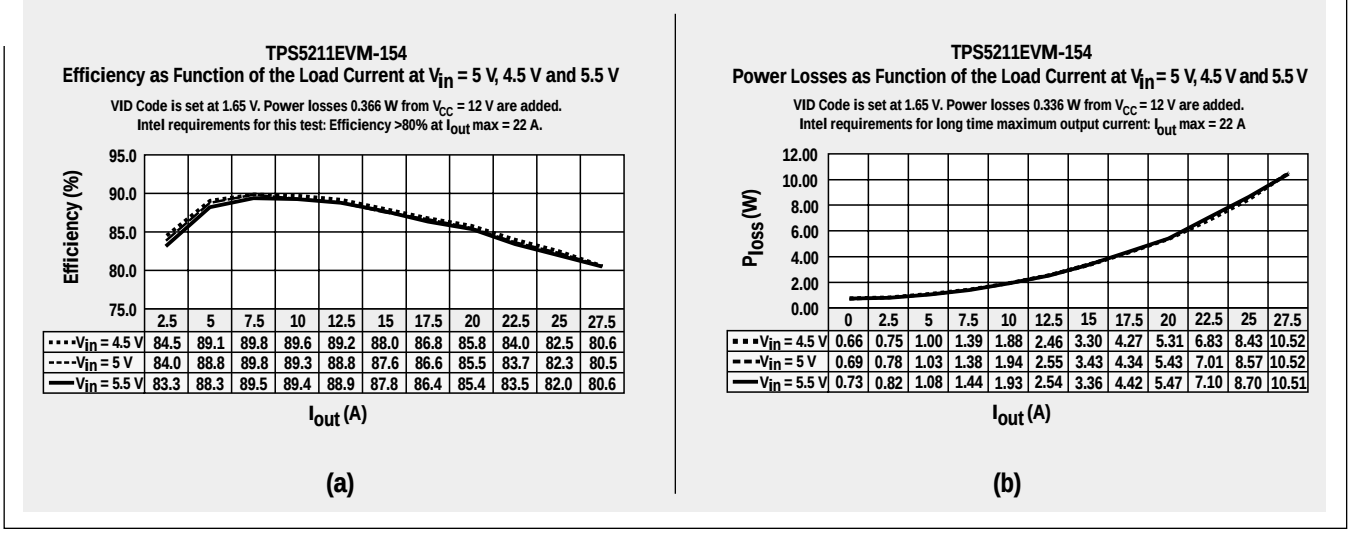
Table 2. Temperature measurement results

COMPONENT	PCB	Q1/Q5 HIGH-SIDE FETs	Q2/Q3 LOW-SIDE FETs	L1, INPUT IND.	L2, OUTPUT IND.	U1, IC	INPUT CAPACITORS				OUTPUT CAPACITORS			
							C1	C2	C3	C4	C6	C7	C8	C9
Temp. (°C)	51.6	78.5/79.5	66.3/70	47	62.3	45	47.8	46.2	43.5	52.5	38.5	45.3	46.8	47.6
Temp. rise (°C)	28.8	55.7/56.7	43.5/47.2	24.2	39.5	23.2	25	23.4	20.7	29.7	15.7	22.5	24	24.8

Table 3. Power losses, efficiency, and high-side FETs temperature for different FETs and frequencies with and without heat sinks. V_{in} = 5 V, V_{out} = 1.65 V, I_{out} = 22 A.

FETs, HIGH-/LOW-SIDE	F_{sw} (kHz)	P_{loss} (W)	EFF (%)	HEAT SINK (With/Without)	TEMPERATURE OF HIGH-SIDE FETs (°C)
MTD3302/SUD50N03-7	130	6.62	84.2	With	79.5
MTD3302/SUD50N03-7	87	6.24	84.9	Without	88
SUD50N03-7/SUD50N03-7	85	6.32	84.8	Without	89
PSMN005-25D/PSMN005-25D	86	5.97	85.5	Without	82

Figure 3. Efficiency (a) and power losses (b) over entire input voltage and output current range



Load-current transient response

The transient tests using the Voltage Transient Test Tool v.2.0 from Intel have been performed in accordance with the corresponding manual from Intel. The output-voltage transient waveforms during the load-current transitions are shown in Figure 4. The Test Tool was connected to the TPS5211EVM-154 evaluation module through the PGA-370 socket. The transient waveforms were measured near the output filter (TP1 on TPS5211EVM-154 module) and through the special test points J5–J7, J6–J8, and J2–J4 of the Test Tool, which are located at the microprocessor side of the PGA-370 connector.

The tests were made under the following conditions in accordance with VRM 8.4 requirements: I_{CC} bias = 2.15 A, I_{CC} max = 26 A, slew rate = 22.1 A/µs, transient duty cycle = 0.5, and transient frequency = 5.5 kHz. The peak-to-peak output voltage amplitude is 150 mV in the worst case with four OS-CON capacitors 4SP560M. The specification limit is 210 mV for this test.

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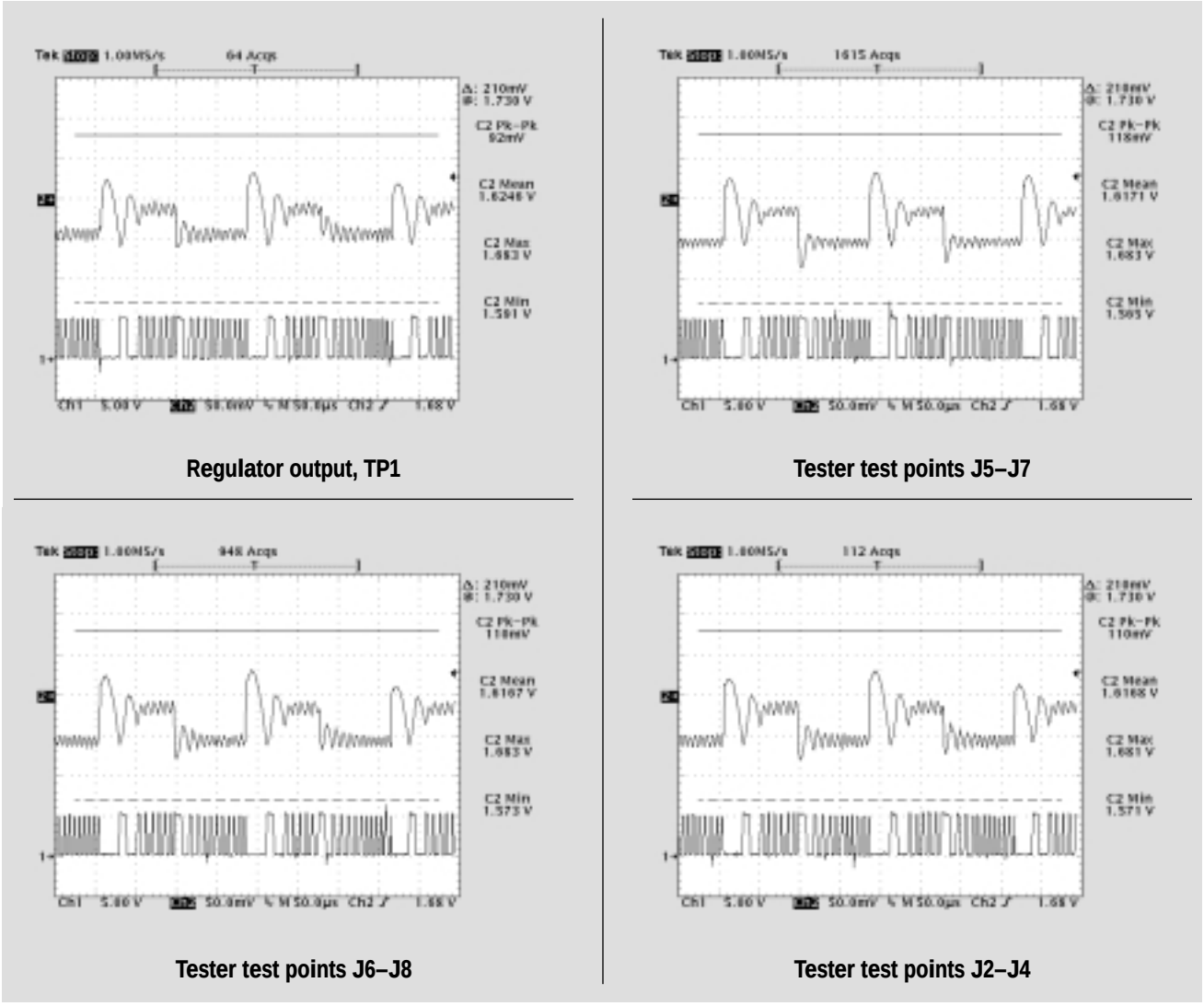
Figure 4. The output-voltage transient response with the Intel Transient Test Tool at transient frequency 5.5 kHz



The cursors show the output voltage limits for this test: 1.52 V minimum and 1.73 V maximum. Ch2 shows the output voltage (50 mV/div.), and Ch1 shows the drain-source voltage (5 V/div.).

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The output-voltage transient response using the internal load-current transient tester is shown in Figure 5. The load-current transition was between 2.2 A and 27.2 A, which corresponds to a 25-A step load. The peak-to-peak output-voltage amplitude for this test is 130 mV, which is also well below the allowable maximum of 210 mV.

Conclusions

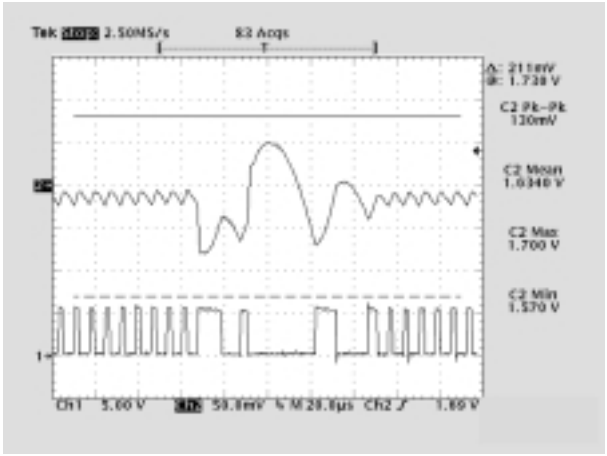
- The TPS5211EVM-154 evaluation module with the TPS5211 hysteretic controller meets the electrical requirements set forth in Reference 4.
- The load-current transient tests using the internal EVM transient tester and the Voltage Transient Test Tool v.2.0 from Intel have shown excellent dynamic characteristics of the TPS5211 hysteretic controller for up to 26-A core current desktop applications with the minimum number of bulk OS-CON capacitors.
- The component temperature measurements in worst-case cooling conditions have given reasonable results.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace "*lit number*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "TPS5211 High Frequency Programmable Synchronous-Buck Regulator Controller," September 1999	slvs243
2. R. Miftakhutdinov and P. Rogers, "Powering Celeron-type Microprocessors Using TI's TPS5210 and TPS5211 Controllers," *Analog Applications Journal*, February 2000, pp. 20-28	slyt012
3. "Designing Fast Response Synchronous Buck Regulator Using the TPS5210," Application Report, March 1999	slva044
4. "VRM 8.4 DC-DC Converter Design Guidelines," Rev. No. 1.6, Intel Corporation, November 1999, order number 245335-001.	—
5. R. Miftakhutdinov, "Analysis of Synchronous Buck Converter with Hysteretic Controller at High Slew-Rate Load Current Transients," *Proc. of High Frequency Power Conversion Conference*, 1999, pp. 55-69.	—

Figure 5. The output-voltage transient response at 25-A load-current step*



** With slew rate of 20 A/µsec during step up and 40 A/µsec during step down, measured at test point TP1.*

The cursors show the output voltage limits for this test: 1.52 V minimum and 1.73 V maximum. Ch2 shows the output voltage (50 mV/div.), and Ch1 shows the drain-source voltage (5 V/div.).

Related Web sites

www.ti.com/sc/docs/products/msp/pwrmgmt/index.htm

www.ti.com/sc/docs/tools/analog/powermanagementdevelopmentboards.html

Get product data sheets at:

www.ti.com/sc/docs/products/analog/tps5211.html

To order the TPS5211EVM-154 (SLVP154) evaluation module, call TI's toll-free order desk at 1-800-477-8924, ext. 5800, in North America. To order in other regions, contact the TI Product Information Center for your region (see page 32) or contact your local TI distributor.

LVDS: The ribbon cable connection

By E.D. Cole, P.E.
Application Engineer, Data Transmission

Introduction

As LVDS gains popularity, multi-channel applications are becoming common. In systems where cables are used to connect drivers to receivers, CAT5-type cable, usually containing unshielded twisted pairs (UTPs), has worked well. Now that 8-channel and 16-channel LVDS drivers and LVDS receivers are available in single packages, ribbon cable is being used successfully in these "wide-bus" applications. It has become much easier to implement 16-, 32-, or 64-channel-wide LVDS systems. But what happens to the performance? The most common cable used in LVDS applications is 4-pair CAT5 cable. When 16 or 32 twisted pairs are needed, can ribbon cable be used?

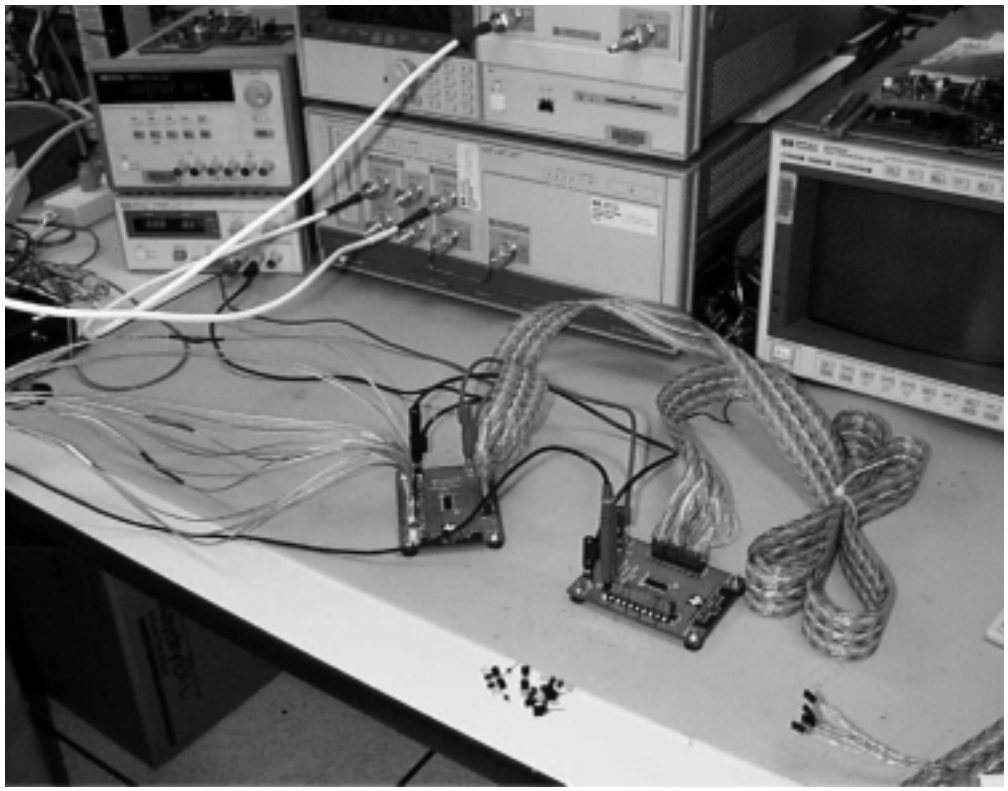
Test set-up

A customer requested our assistance to determine the feasibility of using ribbon cable for a 16-channel-wide point-to-point LVDS system. The customer, using a single LVDS387 driver connected to a single LVDS386 receiver, requested jitter and crosstalk data at 50 Mbps and 100 Mbps using 0.5-m and 3-m lengths of twisted ribbon cable. Similar data has already been published on a 4-channel system using CAT5 cable. A detailed description on the test equipment and test measurements can be found in Reference 1 or at

www.ti.com/sc/docs/psheets/abstract/apps/slla064.htm

For these tests, a generic evaluation module (EVM) was developed (one PWB that can be used for the LVDS387 or LVDS386). BergSticks™ were used for the signal I/O and ribbon cable connections. Amphenol Cable Type 843-132-2801-064 twisted ribbon cable was used. Figure 1 shows the bench test set-up with the EVMs connected using a 3-m length of ribbon cable. The inputs to the LVDS387 driver were provided by a Tektronix HFS-9009 Pattern Generator Mainframe configured with four HFS 9DG1 plug-ins cards.

Figure 1. Bench test set-up



For these measurements, all 16 channels were supplied with NRZ data. The pattern generator was set up with 16 channels supplying pseudo-random binary data to the '387 driver.

The programmable delays between source channels in the pattern generator were set to zero, so all channels would be switching at the same time.

Continued on next page

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Test results

Jitter was measured on the eye pattern at four points along the transmission path:

Point 1. Output of the receiver
Point 2. Input to the receiver
Point 3. Output of the driver
Point 4. Input to the driver

By collecting the jitter values at these four points, jitter added by each component could quickly be determined. For example, the jitter added by the receiver is simply the jitter measured at Point 2 minus the jitter measured at Point 1. Jitter added by the ribbon cable is Point 3 minus Point 2, and so on. Data was collected and loaded into a spreadsheet, and the jitter contribution was plotted for each of the four tests that were run (see Figures 2, 3, 4, and 5).

During the first test, the output jitter from Channel C2 was much higher than from any other channel. Similar problems were also observed on Channel C4. The problem was determined to be a short circuit between input pins on the driver EVM. This was caused by the author's soldering ability.

Data for Channels C2 and C4 were not collected for the remaining tests.

Figure 2. Jitter contributions using 0.5-m ribbon cable at 50 Mbps

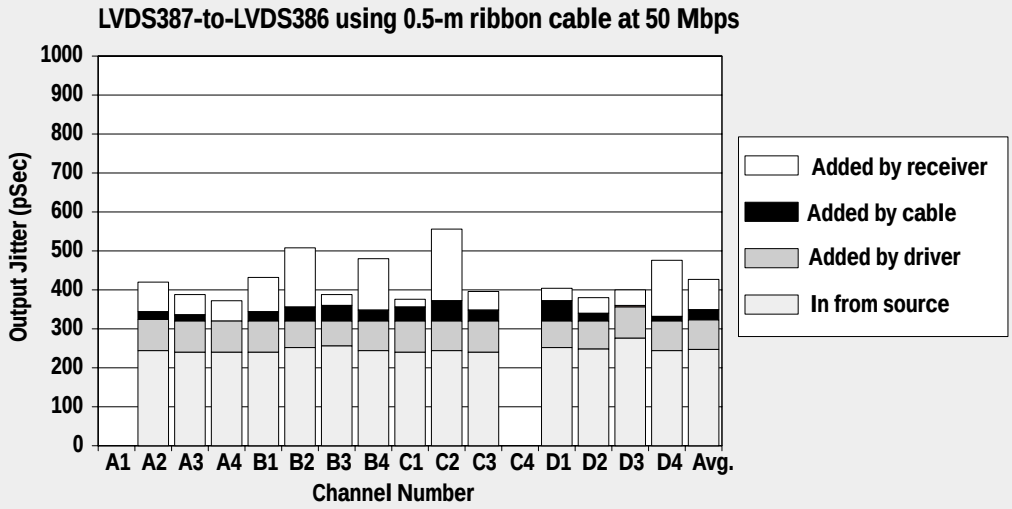
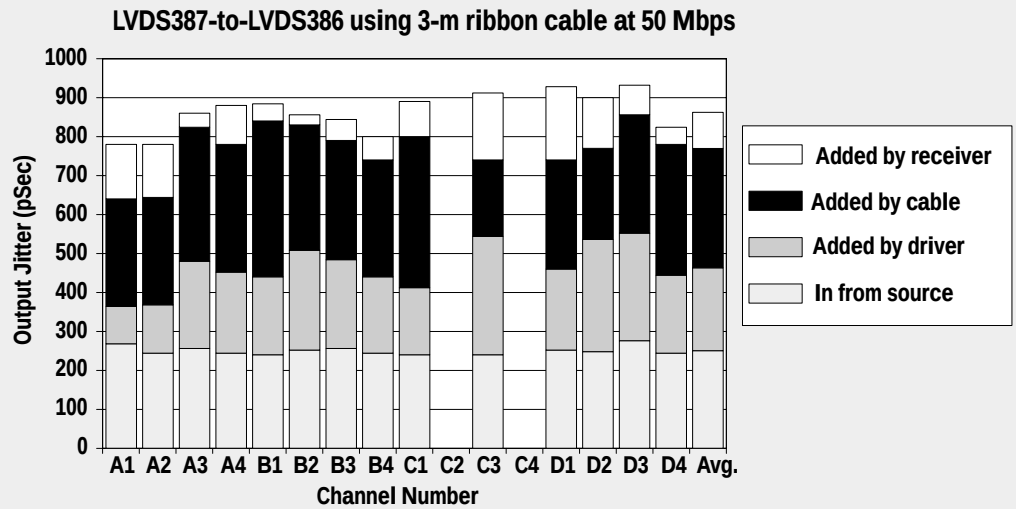


Figure 3. Jitter contributions using 3-m ribbon cable at 50 Mbps



Conclusion

The results show that short lengths of ribbon cable can be used successfully for interconnecting LVDS drivers and receivers. They suggest, however, that the length be kept short, as the increase in cable-generated crosstalk increased significantly between 0.5-m and 3-m lengths tested at 100 Mbps. It should also be noted that there is no significant increase associated with channels running in the middle of the ribbon cable compared to the channels along the edge of the cable.

Reference

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "Measuring Crosstalk in LVDS Systems" . . .	.slla064

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Get product data sheets at:

www.ti.com/sc/docs/products/analog/*device***.html**
Replace *device* with sn65lvds386 or sn65lvds387

Figure 4. Jitter contributions using 0.5-m ribbon cable at 100 Mbps

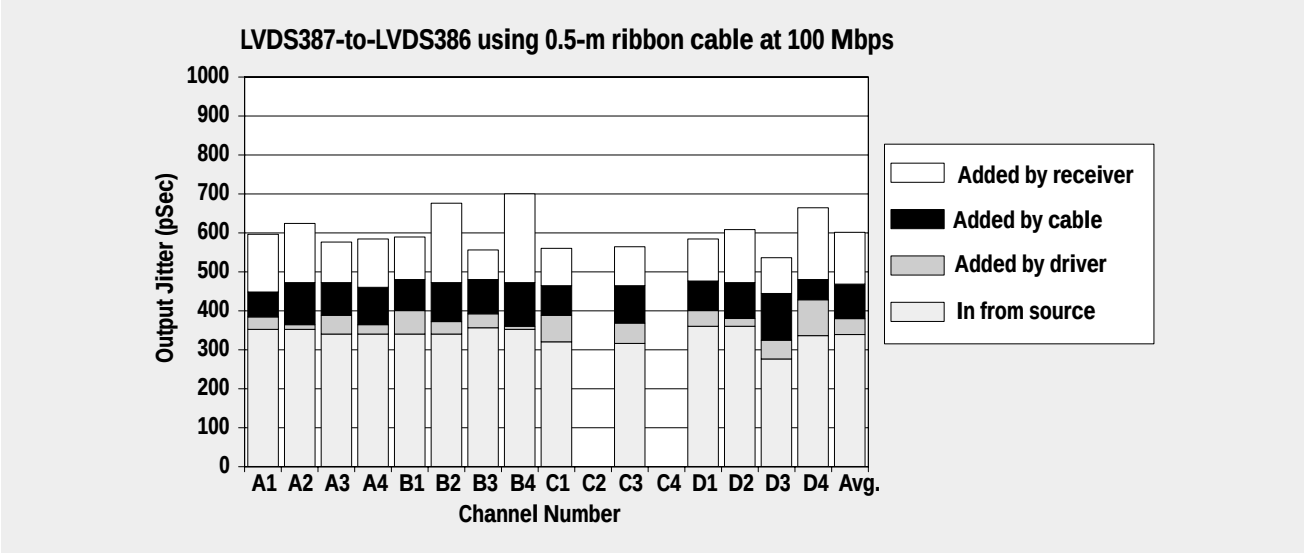
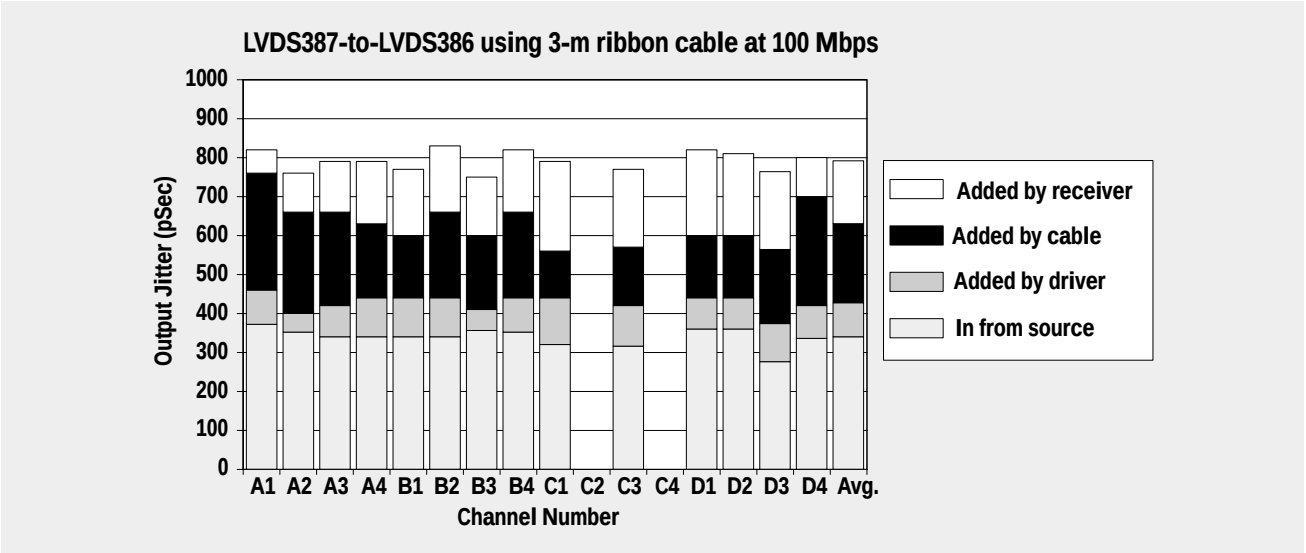


Figure 5. Jitter contributions using 3-m ribbon cable at 100 Mbps



Sensor to ADC—analog interface design

By Ron Mancini
Senior Application Specialist, Operational Amplifiers

Introduction

The sensor output voltage span seldom equals the analog-to-digital converter (ADC) input voltage span. Sensor data is lost and/or ADC dynamic range is not fully utilized because the spans are unequal, start at different DC voltages, or both. In Figure 1(a) the spans are equal but offset. This situation requires level shifting to move the sensor output voltage up by one volt so the spans match. In Figure 1(b) the spans are unequal, but no offset exists. This situation requires amplification of the sensor output to match the spans. When the spans are unequal and offset, as is often the case, level shifting and amplification are required to match the spans.

The spans must be matched to achieve optimum performance because mismatched spans lose sensor data or require an expensive increase in ADC dynamic range (higher bit converters). The op amp is the best analog circuit available for matching the spans because it level shifts and amplifies the input voltage to make the spans equal. The op amp is so versatile that it level shifts and amplifies the input signal simultaneously.

A similar but different problem exists in the digital-to-analog converter (DAC)/actuator interface. The DAC output voltage span must match the actuator input voltage span to achieve maximum performance. The procedure for matching the DAC output span to the actuator input span can be quite different from the procedure for matching the sensor output span to the ADC input span. The DAC/actuator interface will be covered in a later issue of this journal. Sensor outputs are usually low-level signals, thus care must be taken to preserve their signal-to-noise ratio. Actuator input signals may require significant power, thus robust op amps are required to drive some actuators.

If you don't have a good working knowledge of circuits and op amp equations, please refer to the "Understanding Basic Analog..." series of application notes available from Texas Instruments. Application Note SLAA068, entitled, "Understanding Basic Analog—Ideal Op Amps," develops the ideal op amp equations based on a set of ideal op amp assumptions that are tabulated in Table 1 for your reference.

Table 1. Ideal system parameter values

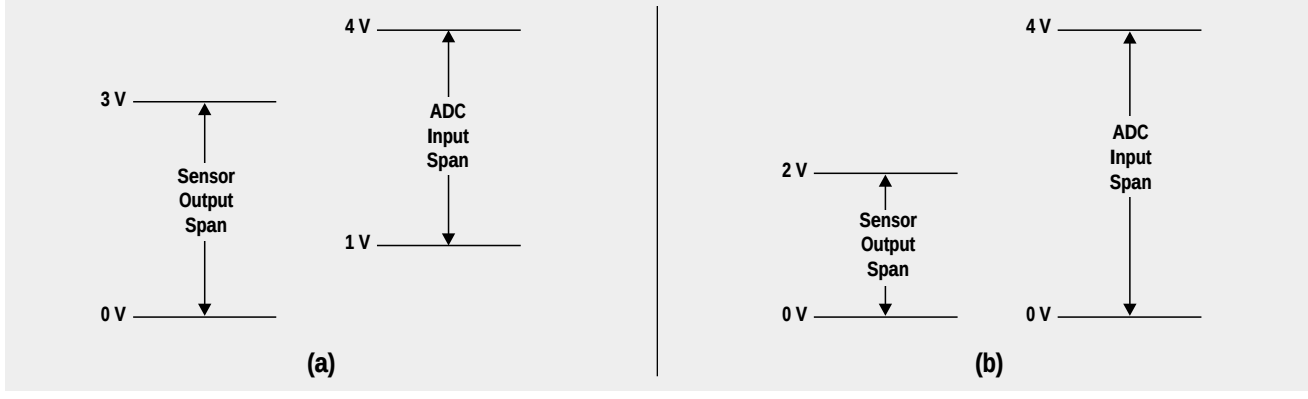
PARAMETER NAME	PARAMETER SYMBOL	VALUE
Input current	I_{IN}	0
Input offset voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Gain	a	∞

The circuit design gets complicated when amplification and level shifting are required. To simplify this article, the op amp equations used here are taken directly from Application Note SLOA030, entitled, "Single Supply Operational Amplifier Design Techniques."

Design procedure

A step-by-step design procedure that results in the proper op amp selection and circuit design begins on the following page. This design procedure works best when the op amp has almost ideal performance so that ideal op amp equations are applicable. The latest generation of rail-to-rail op amps makes the ideal assumption more valid than it ever was. No design procedure can anticipate all possible situations, and depending on the op amp selected, procedure modifications may have to be made to account

Figure 1. Example of spans that require correction



for op amp bias current, input offset voltage, or other parameters.

1. The sensor's output voltage range determines the op amp's required input voltage range (V_{IN1} to V_{IN2}).
2. The ADC's input voltage range determines the op amp's required output voltage swing (V_{OUT1} to V_{OUT2}).
3. Scan the sensor and ADC specifications, and put the data into the format of input/output pairs—V_{IN1}, V_{OUT1} and V_{IN2}, V_{OUT2}.
4. $\Delta V_{OUT}/\Delta V_{IN}$ determines the op amp gain. This is a good point to consider the effect of the input offset voltage.
5. Determine the output impedance of the sensor; this impedance sets the input impedance requirement for the op amp circuit. This is a good point to consider the effect of input bias current.
6. Determine the input impedance of the ADC; this impedance sets the output impedance requirement for the op amp circuit. This is a good point to consider the effect of op amp output impedance.
7. Characterize the reference voltage available, including initial tolerances and drift.
8. Consider noise, power, current drain, frequency response, and other variables that might affect the design.
9. Use the data to form simultaneous equations, and obtain the equation for the op amp circuit.
10. Use the op amp equation to determine the resistor values.
11. Build the circuit and test it.

Design example—reading the specifications

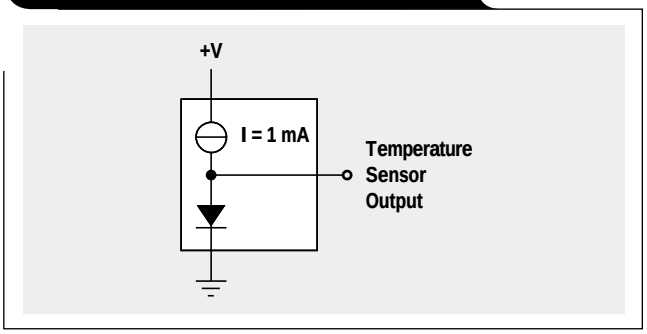
The sensor in this example is a diode temperature sensor (see Figure 2). The diode in this sensor is selected because it has a specified output voltage of 650 mV at 25°C ambient temperature. The sensor output voltage changes –2 mV/°C, and the application requires the sensor to measure temperatures ranging from –25°C to +100°C. Based on the application, the diode voltage is calculated as 650 – 150 = 500 mV at 100°C, and 650 + 100 = 750 mV at –25°C. This data is translated as V_{IN1} = 500 mV, V_{IN2} = 750 mV.

Systems engineering selected the TLV2544 ADC for this design. The analog input range for this ADC is 0 to 5 V. The sensor signal should completely fill the ADC input span; hence, the ADC input data is translated as the op amp output data V_{OUT1} = 0 V, and V_{OUT2} = 5 V (the circuit uses a single 5-V power supply). The highest temperature corresponds to the lowest ADC output number, so the input and output voltages are coupled as V_{IN1} = 500 mV at V_{OUT1} = 0 V, and V_{IN2} = 750 mV at V_{OUT2} = 5 V. This completes step one.

Determining the op amp input and output voltage ranges

The TLV247x product family is a candidate for the op amp slot, so its specifications are compared against the input and output requirements to determine suitability for the job. The common-mode input voltage range for the TLV247x is from –0.2 V to +5.2 V when V_{CC} = 5 V, and because this range exceeds the input signal range of V_{IN1} = 500 mV to V_{IN2} = 750 mV, the input voltage range

Figure 2. Diode temperature sensor



is adequate. The high-level output voltage capability of the TLV247x with a 2-kΩ load is 4.85 V minimum and 4.96 V nominal. The TLV247x low-level output voltage with a 2-kΩ load is 150 mV maximum and 70 mV nominal. I am not a fan of nominal data sheet specifications, but since the load is approximately 20 kΩ (this assumes that conversion and sampling are not coincident), the majority of the units built will be closer to the nominal output voltages than the guaranteed specifications.

The TLV2544 is a 12-bit ADC, and the voltage value of each bit is calculated below as 1.22 mV/bit.

$$\frac{\text{Input}}{\text{Resolution}} = \frac{5}{2^{12}-1} = 1.22\frac{\text{mV}}{\text{Bit}} \qquad \textbf{(1)}$$

The converter loses 150 mV + 150 mV = 300 mV of range because the op amp output voltage swing is limited when using guaranteed specifications. This translates into a loss of 246 bits out of 4095 bits because the full input range of the ADC is not used. The actual error will be closer to 50 mV + 30 mV = 80 mV (allowing for a larger load), and this translates into a loss of 66 bits out of 4095 bits.

The 5-V power supply feeds the op amp and ADC, and this guarantees that some range will be lost because no op amp can drive current into a load without incurring a voltage drop. The only way to preserve the converter's dynamic range is to power the op amp from a larger power supply. When converter cost was exorbitant, op amps driving 5-V ADCs were run from ±12-V power supplies, but this isn't required now in the day of moderately priced converters. Let the circuit be designed for an output range of 0 V to 5 V, knowing that the guaranteed range is 150 mV to 4.85 V and that the accuracy loss has to be accepted.

The op amp gain and impedances

The amplifier gain is approximately 5/0.25 = 20; and the TLV247x, with an open-loop gain in excess of 100,000, can accurately amplify with a closed-loop gain of 20 (especially at the low frequencies involved in temperature measurement). The op amp's input offset voltage (2.2 mV maximum) is multiplied by the gain, so the offset voltage presented to the converter input is 44 mV. This introduces a 36-bit error into the system.

The output impedance of the sensor is essentially the output impedance of a forward-biased diode. The equation

Continued on next page

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for a forward-biased diode is given below, where r_e is the diode resistance and I_{BIAS} is given in mA.

$$r_e = \frac{26}{I_{BIAS}} = 26\,\Omega \qquad (2)$$

The diode resistance, 26 Ω, forms a voltage divider with the op amp input resistance. The TLV247x input resistance is 10^{12} Ω nominal, but let's assume that circuit resistors lower the input resistance to 20 kΩ. A voltage divider is formed by the sensor output resistance and the circuit input resistance (see Equation 3). The diode resistance introduces a 1.3-mV error that is approximately one bit, so the diode resistance is neglected.

$$\text{Error} = \frac{R_{IN}}{R_{IN} + R_{DIODE}} = \frac{20{,}000}{20{,}000 + 26} = .9987 \qquad (3)$$

The input bias current (300 pA maximum) introduces an error by causing a voltage drop across the parallel combination of the feedback and input resistor. Assuming 20-kΩ input resistance and a gain of 20, the voltage drop at the converter input is $(400 \times 10^{3})(300 \times 10^{-12})$ = 0.12 mV, or less than one bit. The input current error is neglected.

The input impedance of the converter is very high most of the time, but it is 20 kΩ minimum when sampling. The output resistance of the TLV247x is 1.8 Ω nominal. The op amp output resistance and converter input resistance form a voltage divider that introduces a .09-mV error, which is less than one bit; thus the op amp output impedance is neglected.

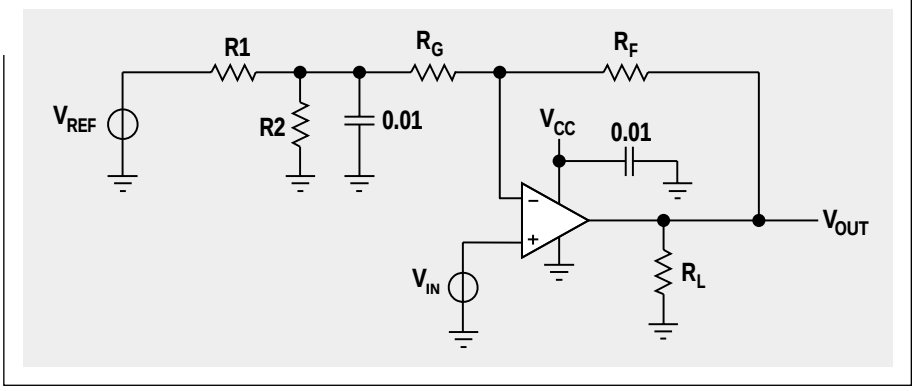
Selecting a reference

The reference is an input to the ADC, therefore any noise or disturbance on the reference input shows up as an error. The reference input is decoupled with a .01-µF capacitor to reduce noise. A reference diode is used because the power supply (5 V) has too much noise and drift to be used as a reference. A 2.5-V stable temperature-compensated reference diode is selected for the design. This diode has an initial tolerance of ±10 mV and a total drift of 10 mV. The converter range sacrificed to the diode inaccuracy is 25 bits.

Selecting the op amp

The TLV247x is a CMOS op amp, so it has low power and current drain. The op amp noise is low for a CMOS device, and it shouldn't cost one bit in accuracy. The biggest anticipated noise problem comes from the cable carrying the sensor voltage to the op amp input. Shielding the sensor input (by tying one end of the shield to ground) can reduce this noise, and if a ground plane circuit board is used, conducted noise should not be a problem. Temperature is a slowly changing variable, so the op amp frequency response is not important. The TLV247x satisfies all the requirements and justifies the ideal op amp assumption, so it is selected for the design.

Figure 3. Op amp circuit yielding $V_{OUT} = 20\,V_{IN} - 10$



Simultaneous equations

The equation of an op amp is the equation of a straight line; therefore, there are four potential solutions to the problem. One solution is correct for the problem at hand, and the method of finding that solution is to solve simultaneous equations because their solution yields the magnitude and sign of the slope and zero axis intercept (m, b). Use the input/output data to make the following two equations.

$$0 = .5m + b \qquad (4)$$

$$5 = .75m + b \qquad (5)$$

Equation 4 yields m = –2b. Substituting Equation 4 into Equation 5 yields Equation 6.

$$-\frac{m}{2} = 5 - .75m \qquad (6)$$

Equation 6 defines the slope as m = 20 and the zero axis intercept as b = –10. Substituting these values back into Equations 4 and 5 proves that the algebra is correct. The equation for an op amp has the form $V_{OUT} = mV_{IN} + b$; thus, substituting the values obtained from Equation 6 yields Equation 7.

$$V_{OUT} = 20V_{IN} - 10 \qquad (7)$$

Determining the resistor values

The op amp circuit that yields the transfer function given in Equation 7 is shown in Figure 3, and the transfer function for that circuit is given in Equations 8, 9, and 10.

$$V_{OUT} = V_{IN}\left(\frac{R_F + R_G + R_1 \| R_2}{R_G + R_1 \| R_2}\right) \cdots\cdots \qquad (8)$$

$$\cdots\cdots - V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1 \| R_2}\right)$$

$$m = \frac{R_F + R_G + R_1 \| R_2}{R_G + R_1 \| R_2} \qquad (9)$$

$$|b| = V_{REF}\left(\frac{R_2}{R_1+R_2}\right)\left(\frac{R_F}{R_G+R_1+R_2}\right) \quad \textbf{(10)}$$

Some simplification is desired prior to making the final calculations. If $R_G >> (R_1 + R_2)$ then $(R_1 + R_2)$ and $R_1 \| R_2$ can be neglected, and Equations 9 and 10 reduce to Equations 11 and 12.

$$m = 20 = \frac{R_F + R_G}{R_G} \quad \textbf{(11)}$$

$$|b| = \left(\frac{R_2}{R_1+R_2}\right)\frac{R_F}{R_G} \quad \textbf{(12)}$$

Let R_G = 27 k**Ω**; then Equation 11 yields R_F = 513 k**Ω**. Select R_F = 510 k**Ω** because it is the closest standard 5% value. Substituting the resistor values for R_F and R_G into Equation 12 yields $R_1 = .888R_2$. Select R_2 = 270 **Ω** and R_1 = 240 **Ω**. The error incurred by neglecting R_1 and R_2 is approximately .51/27 = .018; this error is much less than the resistor tolerances.

The resistors are selected from the 5% values, but that does not mean that they have to have 5% tolerances. The resistor tolerances in a 12-bit circuit are normally 1% or smaller because 1% metal film resistors have excellent drift and end-of-life tolerances.

Adjustments

Resistors with a 1% tolerance have about a 3% tolerance at the end of their life. A 3% tolerance equates to about 5-bit accuracy, so the circuit must be adjusted to obtain an initial accuracy close to 12 bits. R_2 is split into R_{2A} and R_{2B} as shown in Figure 4. If R_{2A} is 220 **Ω** and R_{2B} is a 100-**Ω** pot, the reference voltage can be adjusted from 1.19 V to 1.32 V, and this yields an adjustment range of approximately 14%.

The reference adjustment is easy to implement with a DAC. The inverting gain is R_F/R_G = 19. If R_F is changed to a fixed resistor, R_{FA} = 470 k**Ω**, and a pot, R_{FB} = 100 k**Ω**, the gain adjustment range is approximately 10%. The gain is hard to adjust with a DAC because a resistor value must be changed, but sometimes a DAC and multiplier are used to give a variable gain.

Set the gain first and the reference voltage second to minimize interaction between the adjustments.

Build and test

After the calculations are completed, build and test the circuit. The circuit should be built with off-the-shelf components, not with selected or hand-delivered samples. Sometimes samples must be used to build the circuit because samples are the only parts available. There is some element of risk using samples, so retesting is in order when components become available from production.

The performance test results should be closer to nominal than the extremes because randomly selected components should have close-to-nominal values. If the data is skewed from nominal, troubleshoot the circuit until you find the reason for the skew. Skewed data is often an indicator of an error in the calculations. Also, test for conditions well beyond the design specifications. Look for problems like latch-up, find out what happens when the input voltage goes out of range, and check the noise performance. The prudent engineer tests extensively and makes changes prior to production.

Summary

Start the design with a review of the design specifications, sensor specifications, and potential component specifications. Use the sensor and ADC specifications to formulate the op amp input and output voltages. Calculate the effects of the input and output impedances; insure that op amp imperfections don't interfere with the design; and select the reference, ADC, and op amp. Use simultaneous equations to determine what equation the op amp must implement. Use the op amp equation to select a circuit configuration from the reference, and calculate the resistor values using the reference equations. Build and test the circuit, and if the results are good, you are done.

References

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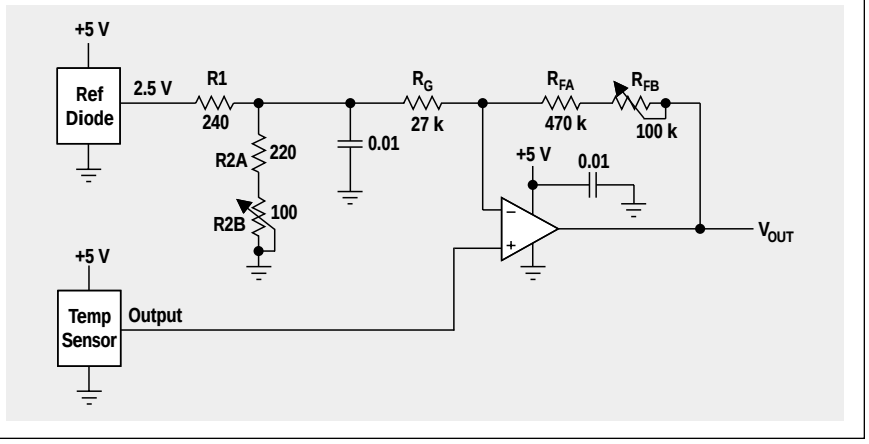
Get product data sheets at:

www.ti.com/sc/docs/products/analog/*device*.html
Replace *device* with tlv2470, tlv2471, tlv2472, tlv2473, tlv2474, tlv2475, or tlv2544

Figure 4. Final circuit diagram



Using a decompensated op amp for improved performance

By Jim Karki
Systems Specialist, High-Speed Amplifiers

Introduction

If your application requires optimum noise, slew rate, and distortion performance, you may want to use a decompensated or uncompensated op amp.

The THS4011 op amp uses emitter degeneration and dominant pole compensation to compensate the amplifier internally so that external compensation is not required. Placing resistors in the emitter leads of a differential amplifier pair results in negative feedback, which reduces the gain of the stage. This is referred to as emitter degeneration. A capacitor placed in the intermediate stage of the amplifier provides dominant pole compensation.

Figure 1. Open-loop gain and phase—THS4011 and THS4021

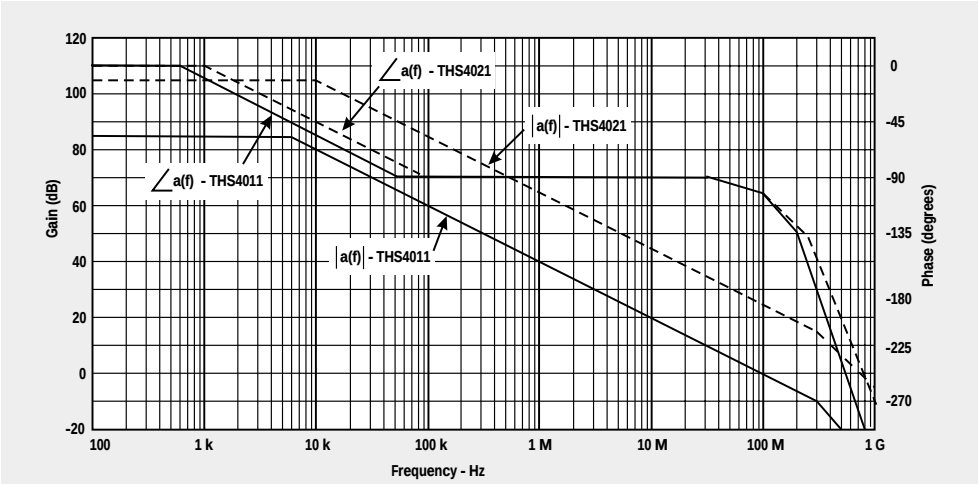
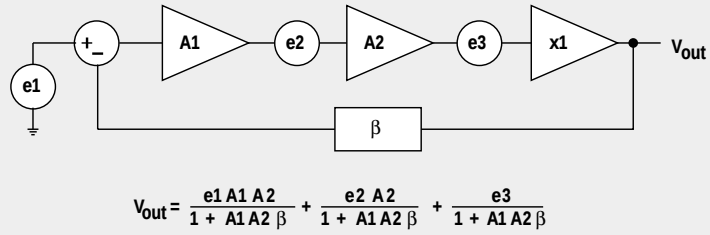
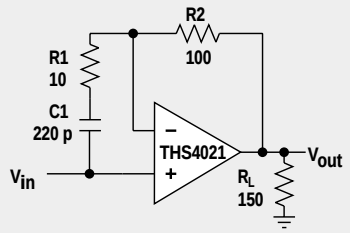


Figure 2. Model of op amp with negative feedback



$$V_{out} = \frac{e1\,A1\,A2}{1 + A1\,A2\,\beta} + \frac{e2\,A2}{1 + A1\,A2\,\beta} + \frac{e3}{1 + A1\,A2\,\beta}$$

Figure 3. Externally compensated THS4021—non-inverting amplifier



$$\beta = \frac{1 + sC1R1}{1 + sC1(R1 + R2)}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + \frac{1}{a(f)\beta}} = 1 \text{ if } a(f)\beta >> 1$$

The THS4021 does not use emitter degeneration in the input pair, and the dominant pole capacitance is reduced. The THS4021 is termed a decompensated op amp. Decompensation means the compensation is reduced, as opposed to uncompensated, where no compensation at all is used. The result is:

- higher open-loop gain,
- increased slew rate,
- lower input referred noise, and
- required external compensation for unity gain stability.

Figure 1 shows the open-loop gain, magnitude $|a(f)|$ and phase $\angle a(f)$, of the THS4011 and THS4021. Note that $|a(f)|$ is about 20 dB higher for the THS4021; and note the two spots on the graph where, for THS4011,

$$|a(f)| = 0 \text{ dB and } \angle a(f) \approx -105°$$

and, for THS4021,

$$|a(f)| = 20 \text{ dB and } \angle a(f) \approx -130°$$

So the THS4011 has 75° of phase margin at a closed-loop gain of +1 and requires no external compensation. The THS4021 has 50° of phase margin when compensated by giving it a closed-loop gain of +10 (or –9). If a gain lower than this is required, another means of compensation is used.

This article shows how to compensate the THS4021 externally for stable operation while maintaining a closed-loop gain of +1 or –1. To compare distortion, transient response, and noise performance, the THS4011 and THS4021, with external compensation, are tested. Also, practical component selection is considered. A quick presentation about feedback is given, but it is assumed that the reader is familiar with feedback theory, stability criteria, and compensation. If not, please see References 1 and 2.

Feedback and errors

Feedback theory predicts that error sources within an amplifier are reduced if the loop gain is increased.

Figure 2 shows a model of an op amp with negative feedback. The input stage is A1, the intermediate stage is A2, the output stage is the x1 buffer, and β is the feedback factor. The open-loop gain is $a(f) = A1A2$, and the loop gain is $a(f)\beta = A1A2\beta$. e1, e2, and e3 are generalized error sources within the op amp. The following discussion analyzes the output response due to the individual error sources.

e1 represents an error source at the input. It is amplified by the full open-loop gain of the amplifier. Setting all other sources to 0, if there were no feedback, $V_{out} = e1A1A2$, but with feedback,

$$V_{out} = \frac{e1}{\beta + \frac{1}{A1A2}} \approx \frac{e1}{\beta} \quad \text{if } A1A2 >> 1$$

e2 represents an error source at the intermediate stage. It is amplified only by A2. Setting all other sources to 0, if there were no feedback, $V_{out} = e2A2$, but with feedback,

$$V_{out} = \frac{e2}{A1\beta + \frac{1}{A2}} \approx \frac{e2}{A1\beta} \quad \text{if } A2 >> 1$$

e3 represents an error source at the output stage. It is buffered by a gain of +1 to the output. Setting all other sources to 0, if there is no feedback, $V_{out} = e3$, but with feedback,

$$V_{out} = \frac{e3}{1 + A1A2\beta} \approx 0 \quad \text{if } A1A2\beta >> 1$$

In general, feedback has no effect on reducing errors generated at the input, but it becomes effective with errors generated within the amplifier and is most effective in reducing errors at the output. By taking advantage of the increased open-loop gain of the THS4021, one can expect to reduce distortion products generated in the intermediate and output stages of the op amp.

Test circuits

Figures 3–7 show the test circuits. Circuits a, b, and c show the THS4021 with external

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Figure 4. Two-capacitor, externally compensated THS4021—inverting amplifier

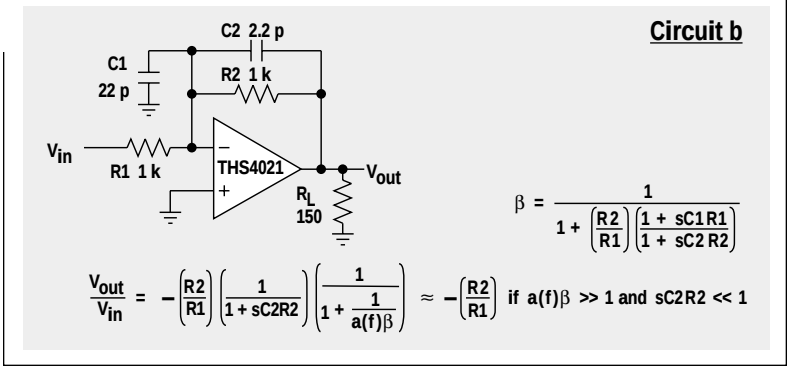


Figure 5. One-capacitor, externally compensated THS4021—inverting amplifier

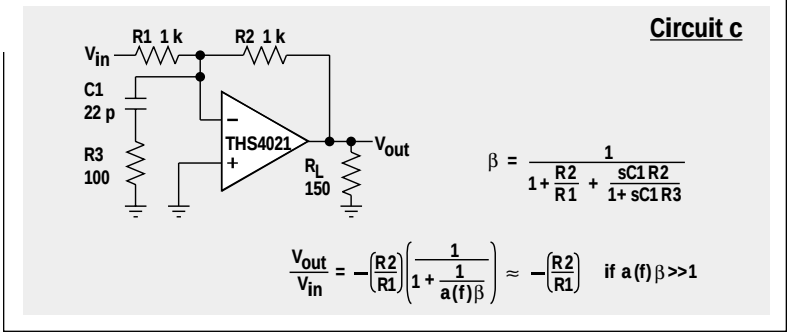


Figure 6. Internally compensated THS4011—non-inverting amplifier

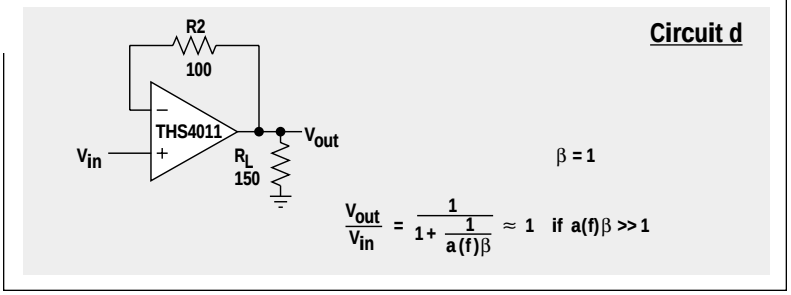
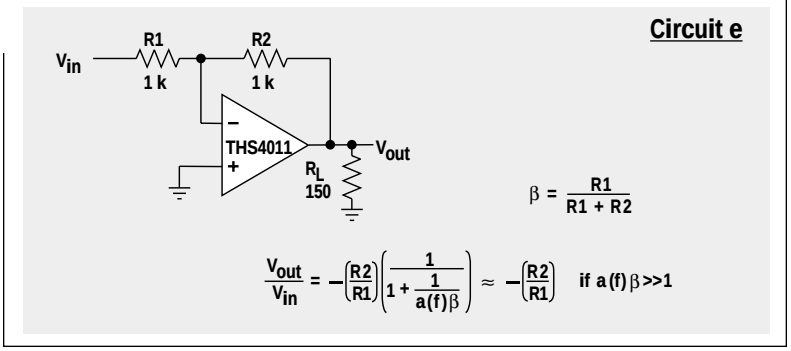


Figure 7. Internally compensated THS4011—inverting amplifier



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compensation. Circuits d and e show the THS4011. All circuits have ideal gains of either +1 or –1. The test data presented later is based on testing these circuits with the component values shown.

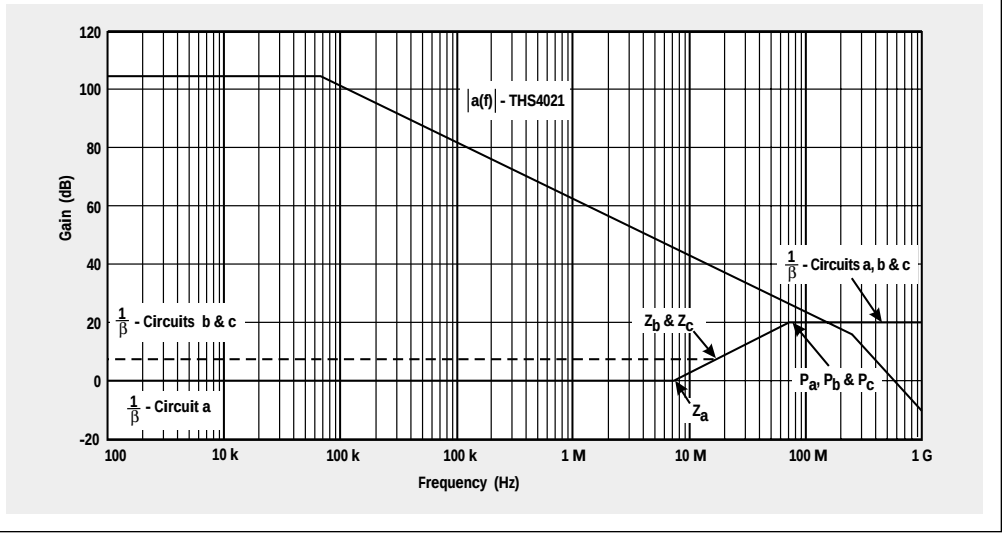
Analysis

In order to determine stability of circuits a, b, and c, we are interested in the loop gain, a(f)β, of the circuits. Figure 8 shows a Bode plot of the open-loop gain, a(f), of the THS4021 op amp and the inverse of the feedback factor, 1/β.

a(f)β can be seen graphically on the Bode plot as the difference between the a(f) and 1/β curves. Stability is indicated by the rate of closure at the intersection of a(f) and 1/β.

Figure 9 shows the same information from a slightly different view, with magnitude and phase of a(f)β. This makes it easier to determine phase margin—approximately 45°.

Figure 8. Bode plot of open-loop and inverse feedback factors of test circuits



Design

Design means choosing the placement of the poles and zeros in the feedback network. The following equations apply to the points noted on the Bode plot in Figure 8.

Circuit a: $Z_a = \frac{1}{2\pi C1(R1+R2)}$ and $P_a = \frac{1}{2\pi C1R1}$

Circuit b: $Z_b = \frac{2}{2\pi C1R1}$ and $P_b = \frac{1}{2\pi C2R2}$

(given R1 = R2)

Circuit c: $Z_c = \frac{2}{2\pi C1R2}$ and $P_c = \frac{1}{2\pi C1R3}$

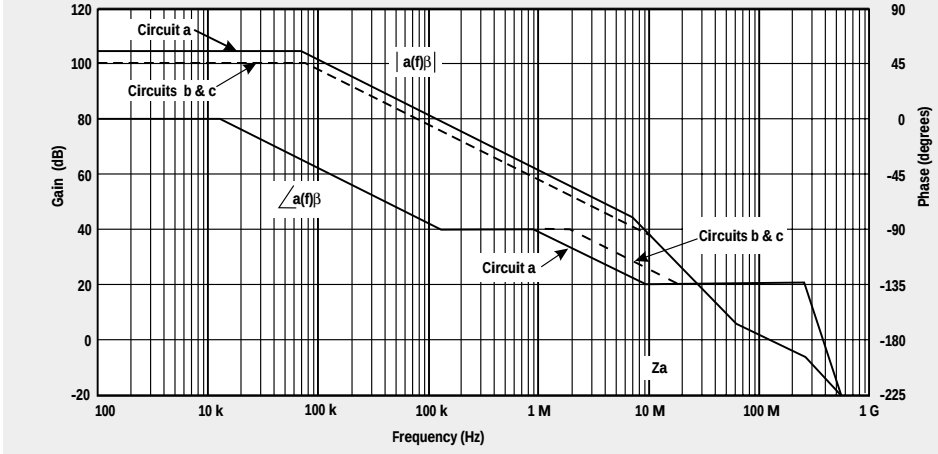
(given R1 = R2)

The poles and zeros are chosen to obtain the largest possible excess loop gain over the maximum frequency range and still maintain stability. The feedback must be reduced at high frequency in the externally compensated circuits so that 1/β = 20 dB at the point where it intersects a(f). This satisfies the minimum gain of 10 requirement for stability for the THS4021. That is to say, what is really meant by specifying a minimum gain of 10 is that 1/β ≥ 10 (or 20 dB) at its intersection with a(f).

Start the design by choosing the pole location and be sure to give a margin for process variations. In the examples shown here, the pole is chosen at about half the frequency at which a(f) equals the minimum gain specification (20 dB). The component values are calculated, and then convenient standard values are selected.

Once the pole is located, the zero is found by dividing the pole frequency by the difference between minimum gain specification of the amplifier and 1/β at low frequency—i.e.,

Figure 9. Bode plot of magnitude and phase of a(f)β—Circuits a, b, and c



$$Z_a = \frac{P_a}{10^{\frac{20}{20}}},\ Z_b = \frac{P_b}{10^{\frac{14}{20}}},\ \text{and}\ Z_c = \frac{P_c}{10^{\frac{14}{20}}}$$

Alternately, you can look at the circuits with a little intuition and arrive at the following relationships: In Circuit a, the high-frequency feedback factor is set by the ratio of R1 to R2. Therefore R1 = R2/10. In Circuit b, the high-frequency feedback factor is set by the ratio of C1 to C2. Therefore C1 = C2 x 10. In Circuit c, the high-frequency feedback factor is set by the ratio of R1 || R3 to R2. Therefore R3 = R2/10. So once the pole is located, the complete solution is quickly found.

Component selection

Selection of component values should be looked at with an eye to practicality. Since the amplifiers are high-speed, capable of operation into the hundreds of MHz, resistance values need to be kept low so that parasitic capacitors do not overly influence results. The designer should be careful about resistor values that are too low, which will load the amplifier too much. The following comments are based on observations made while testing the circuits.

- In Circuit a, feedback resistor values in the range of 100 Ω to 500 Ω provided the best results. Values of 49.9 Ω and 1 kΩ resulted in diminished performance.
- In Circuits b and c, feedback resistor values in the range of 200 Ω to 1 kΩ provided the best results. A value of 100 Ω resulted in diminished performance. Values above 1 kΩ result in capacitor values that are too small (less than 2.2 pF*) and were not tested.

*Approximately 0.6-pF parasitic is measured across the feedback so that parasitic capacitance on the EVM becomes a significant percent when low-value capacitors are used.

THD

The next question to answer is what actually happens when the circuits are tested in the lab. The circuits are built and tested using the THS4011 and THS4021 EVMs, available from Texas Instruments. Figure 10 shows the basic test set-up used to measure THD.

The filters are sixth-order elliptic filters that have approximately 80-dB out-of-band rejection. The purpose of the low-pass filter, LPF, between the generator and the test circuit is to reject harmonics coming from the sine generator. The high-pass filter, HPF, between the test circuit and the spectrum analyzer is there to reject the high-amplitude fundamental and to prevent generation of harmonics in the input circuitry of the spectrum analyzer. Table 1 shows the fundamental frequencies and corner frequencies of the filters used.

Table 1. Filter cut-off frequencies

FUNDAMENTAL (Hz)	LPF (Hz)	HPF (Hz)
1 M	1.1 M	1.9 M
2 M	2.2 M	3.8 M
4 M	4.4 M	7.6 M
8 M	8.8 M	15.2 M
16 M	17.6 M	30.4 M

Figure 11 shows the test results for the non-inverting amplifiers. Circuit a has better distortion performance than Circuit d at lower frequencies, but the advantage

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Figure 10. THD test set-up

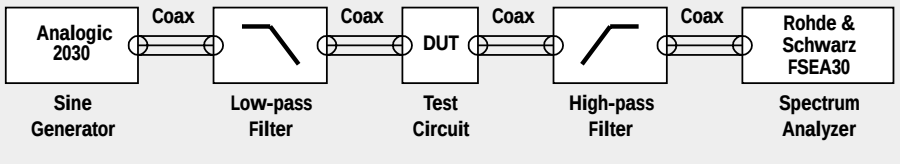
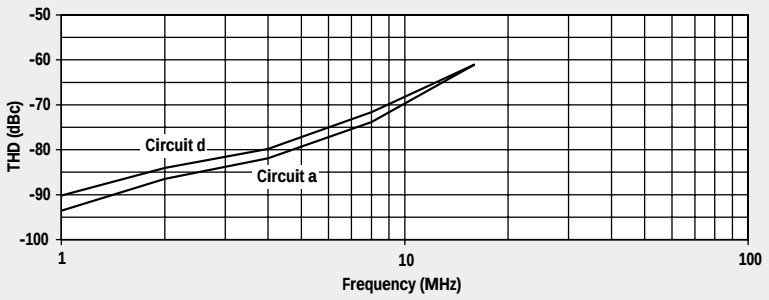


Figure 11. THD vs. frequency—non-inverting amplifiers, V_{out} = $2V_{p–p}$



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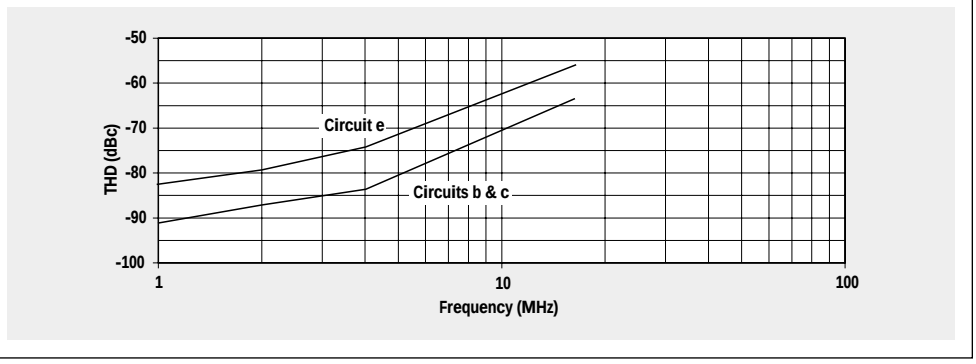
decreases at higher frequencies. Figure 12 shows the test results for the inverting amplifiers. Circuits b and c have better distortion performance than Circuit e across all the frequencies tested.

In general, the externally compensated THS4021 circuits have better distortion performance due to their increased loop gain compared to the circuits using the internally compensated THS4011.

Figure 12. THD vs. frequency—inverting amplifiers, $V_{out} = 2V_{p-p}$



Transient response

Figures 13 and 14 show the transient response of Circuits a, b, d, and e resulting from a positive 2-V input pulse with 0.9-ns rise and fall times. Circuit c is not shown but is very similar to Circuit b.

Circuits a and d appear to have similar slew rates, but Circuit a responds more quickly to the input pulse. Circuit a exhibits about 30% overshoot, but settling times appear to be about the same.

Circuit b reacts more quickly to the input pulse and has approximately twice the slew rate of Circuit e. It appears to settle slightly faster as well.

Noise

The input-referenced white noise specification for the op amps is

$$\frac{1.5\,\text{nV}}{\sqrt{\text{Hz}}}$$

for the THS4021 and

$$\frac{7.5\,\text{nV}}{\sqrt{\text{Hz}}}$$

for the THS4011. Given that the circuits have essentially the same noise gain over most of the frequencies of operation and that the resistor noise is about the same, the noise performance should be 5 times better for the externally compensated circuits.

To measure the noise directly with unity gain is not very practical. For comparison purposes, noise is measured by configuring each op amp in non-inverting gain of 1000 and measuring the output with an RMS voltmeter. Figure 15 shows the test set-up.

The expected output noise is estimated by the formula:

$$\text{En} = \text{en} \times \text{A} \times \sqrt{\text{LPF}}$$

En is the RMS output noise, en is the input-referenced white noise specification for the op amp, A is the ideal closed-loop gain, and LPF is the corner frequency of the low-pass filter (137.5 kHz).

Estimated noise using the THS4011 is 2.78-mV RMS, and 2.47 mV is measured. Estimated noise using the THS4021 is 0.56-mV RMS, and 0.57 mV is measured. As expected, about a 5:1 ratio is seen.

Figure 13. Transient response—non-inverting amplifiers

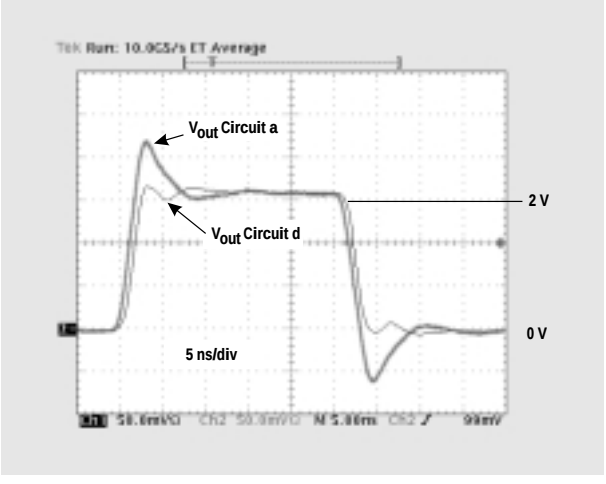
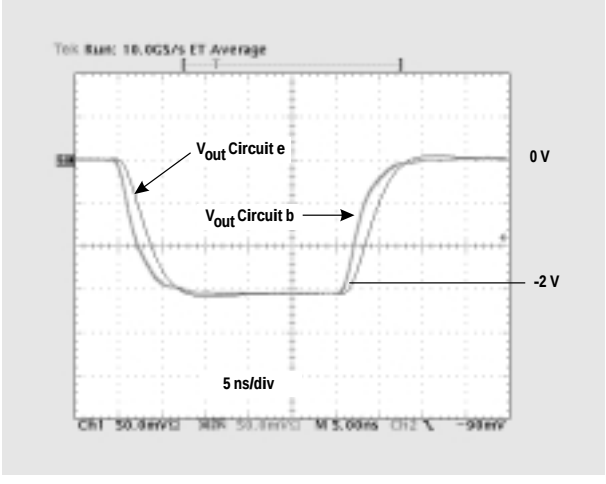


Figure 14. Transient response—inverting amplifiers



Conclusion

Five different circuits have been tested for distortion, transient response, and noise performance. By comparison of the non-inverting amplifiers, Circuit a vs. Circuit d, and inverting amplifiers, Circuits b and c vs. Circuit e, the following conclusions about using an externally compensated THS4021 vs. using the internally compensated THS4011 have been drawn (see Table 2).

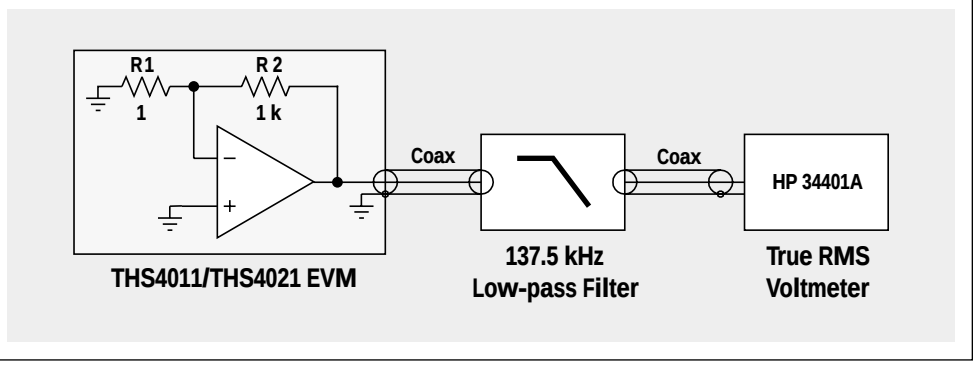
In the inverting amplifiers, Circuits b and c vs. Circuit e, significant improvement in THD performance was seen across the frequencies tested. There was no significant difference between Circuits b and c.

For the non-inverting amplifiers, Circuit a vs. Circuit d, improvement in THD performance was also seen but diminished with frequency, with no advantage seen at 16 MHz.

Transient performance showed mixed results. Slew rate and settling time were somewhat better when comparing the inverting topologies but appeared to be little changed for the non-inverting amplifier. The non-inverting amplifier, Circuit a, showed considerable overshoot, which may be undesirable.

Given that the circuits have essentially the same noise gain over most of the frequencies of operation and that the resistor noise is about the same, the noise performance should be better for the externally compensated circuits. Lab data shows about a 5:1 ratio—in line with the difference in the noise specification of the op amps.

Figure 15. Noise test set-up



References

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Table 2. Comparison of test results

CIRCUIT	DESCRIPTION	TEST PARAMETER	COMMENTS
a	THS4021 non-inverting amplifier with external compensation	Distortion	4-dB improvement seen at 1 MHz with decreased improvement at higher frequencies
		Transient response	Faster initial response, but comparable slew rate and settling time
		Noise	5x improvement
b	THS4021 inverting amplifier with two-capacitor external compensation	Distortion	7- to 9-dB improvement at all frequencies tested
		Transient response	Faster initial response, slew rate, and settling time
		Noise	5x improvement
c	THS4021 inverting amplifier with one-capacitor external compensation	Distortion	7- to 9-dB improvement at all frequencies tested
		Transient response	Faster initial response, slew rate, and settling time
		Noise	5x improvement

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