PCM Codec/Filter Combo Family

Device Design-In and Application Data

Design Considerations

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1 Introduction

A combo is a codec (COder/DECoders) combined with a voice-band filter on a single chip. It converts analog voice-band signals into PCM (pulse code modulated) data, and provides all the functions necessary to interface a 4-wire analog telephone circuit with a TDM (time division multiplexed) system. The most common application for combos is in central office line-card design. However, combos are suitable for many other applications requiring voice-band, bidirectional, analog/digital conversion. Combos are also commonly referred to as 'line-card codecs' or 'voice-band codecs'. A generalized block diagram is shown in Figure 1.

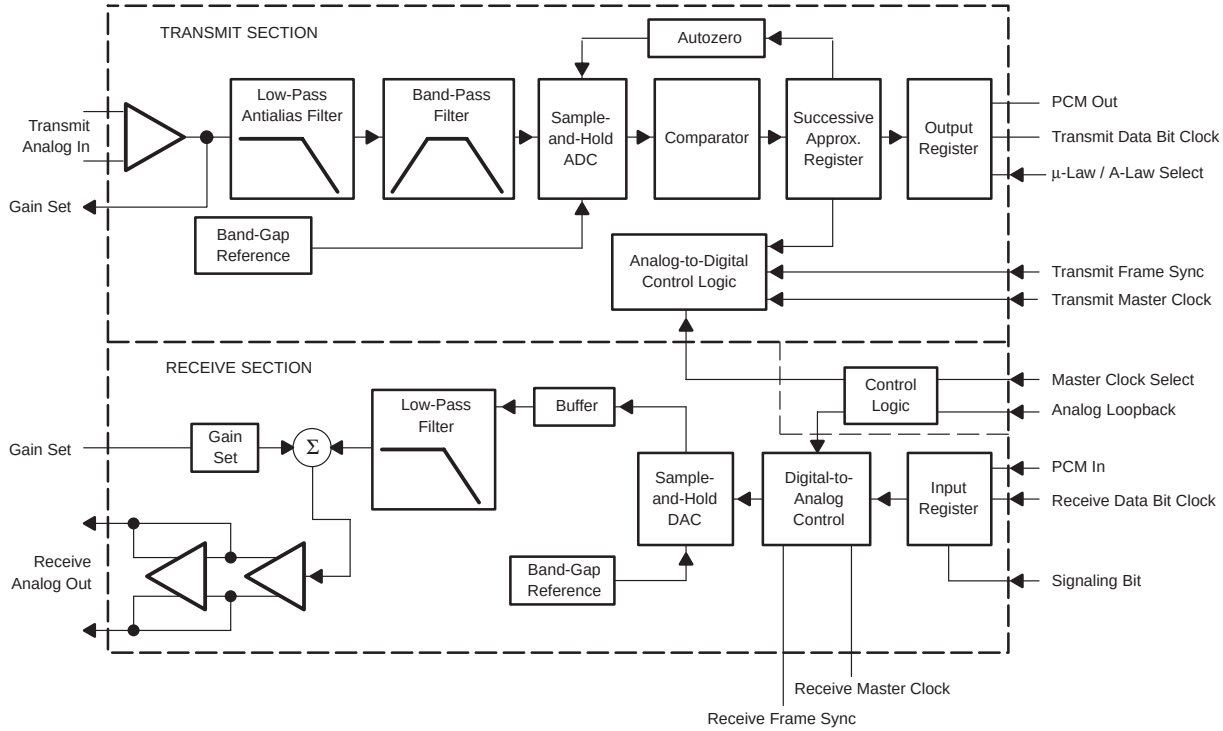


Figure 1. Generalized Combo Block Diagram

Texas Instruments offers a broad range of combos, differentiated by clock speeds, companding options, noise reduction, and other characteristics. The entire TI combo line can be divided into two groups. The first, the TCMxxCxx family, was originally based on the Intel TCM2913. The second, the TP30xx family, was originally based on the National Semiconductor TP30xx family. The two families differ primarily in the way they implement timing, in addition to configurational differences. Since becoming involved in the combo market in 1979, TI has greatly improved its original product offering. Most notably, TI has achieved the lowest idle-channel noise in the combo industry. This has contributed to TI becoming the leading combo manufacturer.

In 1995, TI began development of the Advanced Combo product line, the purpose of which is to provide new, select solutions for customers who require increased integration, features, and performance. These devices are spinoffs from the current TI combo family. The first of these products is the Combo III™ family of devices (TCM37C13A, TCM37C14, and TCM37C15). These parts combine the standard, proven core of TI's TCM29C13 with the added functionality of programmable gain. The next device, QCombo™ (TCM38C17), places four codec/filter channels on a single chip. It also is based on the TCM29C13, but requires only a single 5-V power supply and maintains solid audio performance through TI's advanced 4Vt technology. The QCombo provides lower power consumption and more reliable operation through the use of the new LinEPIC™ 0.8-μm process.

1.1 Document Objective and Scope

The purpose of this document is to expand upon the information presented in TI combo device data sheets by giving additional details on device function and operation, suggestions and recommendations for device application, and troubleshooting guidelines. It is recommended that the reader carefully follow the pertinent data sheets while using this document.

While many of the concepts described in this document apply to the QCombo (TCM38C17), those that depend on detailed filter and converter characteristics do not. This is because the QCombo is based on new ∑Δ (sigma-delta) converter/filter technology, while other combos rely on more mature switched-capacitor filter technology. The internal structure of the ∑Δ devices differ from that of the other combos. Be aware that sections that discuss details about filtering and conversion characteristics may not apply to the QCombo. Specifically, sections 2.1.2 *Transmit Filters*, 2.1.3 *Encoding (A/D Conversion)*, 2.1.4 *Transmit Autozero*, 2.2.1 *Decoding (Companding D/A Conversion)*, and 2.2.2 *Receive Filters* apply only to switched-capacitor-based combos. Also, some of the principles under section 2.3.2 *The Relationship Between Master Clocks, Data Bit Clocks, and Frame Syncs*, depend on filtering technology and, therefore, are different.

1.2 Notational Conventions

This document is targeted at the TCM29Cxx, TP30xx, and the TCM37Cxx TI combo families. While the terminal names of all devices within the TCMxxCxx combo family are consistent, and within the TP30xx combo family are consistent, terminal names differ somewhat between the two families. The majority of terminal functions, however, are similar. Wherever possible, subjects applicable to both families are addressed together, and terminals are referenced by all applicable names, separated by a slash (/). For example, "An analog signal is applied to the transmit analog inputs ANLGIN–/VFXI– and ANLGIN+/VFXI+," where the ANLGIN terminals belong to the TCMxxCxx combo family and the VFXI terminals belong to the TP30xx combo family. The TCM320AC54 is based upon the TP30xx family (the actual relationship is described in the next section), so when references are made to the TP30xx line of TI combos, the TCM320AC54 should be included in this reference.

1.3 TI Combo Family

Figure 2 shows TI combo devices that use National Semiconductor timing and Figure 3 shows TI combo devices that use Intel timing. The devices are further arranged by function and features to aid in selecting the combo that best matches a given application. Page numbers given for the devices indicate the location of the first page of that data sheet in the 1996 edition of the *Wireless and Telecommunications Products Data Book*. Literature numbers given for the devices can be used to obtain standalone data sheets from TI.

TP30xx — National Timing								
For Central Office Equipment Use								Interface For DTAD/DSP
Direct National Replacement				Reduced Noise (by 50% using a patented TI process)				
Differential Output		Single Ended Output		Single Ended Output		Differential Output		Single Ended
μ-Law	A-Law	μ-Law	A-Law	μ-Law	A-Law	μ-Law	A-Law	μ-Law
1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz
TP3064A	TP3067B	TP3054A	TP3057B	TP3054B	TP3057A	TP3064B	TP3067A	TCM320AC54
			PAGE NO. 2–161 LIT. NO. SCTS042A					PAGE NO. 6 – 43 LIT. NO. SCTS029A
		PAGE NO. 2–145 LIT. NO. SCTS026C						
	PAGE NO. 2–197 LIT. NO. SCTS031D							
PAGE NO. 2–177 LIT. NO. SCTS025C								

Figure 2. TI Combo Selection Chart — National Timing

TCMxxCxx														
Intel Timing														
For Central Office Equipment Use												**Analog Interface For DSP**		
Direct Intel Replacement				Reduced Noise (by 50% using a patented TI process)				Programmable Gain			Quad channel QCOMBO	Low Cost		Extended Frequency
		Both μ-Law and A-Law				Both μ-Law and A-Law								
μ-Law	A-Law	8th Bit Signal	Stand-ard	μ-Law	A-Law	8th Bit Signal	Stand-ard	μ-Law	A-Law	μ-Law and A-Law	μ-Law and A-Law Single Voltage Supply (+5V)	μ-Law	μ-Law	μ-Law and A-Law
2.048 MHz	2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	2.048 MHz	2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	2.048 MHz	2.048 MHz	1.536 1.544 2.048 MHz	2.048 MHz	2.048 MHz	1.536 MHz	up to 4.096 MHz
TCM 29C16	TCM 29C17	TCM 29C14	TCM 29C13	TCM 29C16A	TCM 29C17A	TCM 29C14A	TCM 29C13A	TCM 37C13A	TCM 37C15	TCM 37C14	TCM38C17	TCM 29C18	TCM 29C19	TCM 29C23
PAGE NO. 2–3 LIT. NO. SCTS011G				**PAGE NO. 2–27 LIT. NO. SCTS030D**				**PAGE NO. 2–105 LIT. NO. SLWS018**			**PAGE NO. 2–125 LIT. NO. SLWS040**	**PAGE NO. 2–51 LIT. NO. SCTS021C**		**PAGE NO. 2–69 LIT. NO. SCTS029A**

Figure 3. TI Combo Selection Chart — Intel Timing

TI combos are designed to be completely compliant with CCITT and Bellcore recommendations. The TCM29C18, TCM29C19, TCM29C23, and their derivatives, however, are versions of the TCM29Cxx line that have a more relaxed specification. Likewise, the TCM320AC54 is a version of the TP3054 that also has a more relaxed specification. These devices make excellent low-cost solutions for applications that do not need to meet stringent CCITT and Bellcore requirements, such as DTAD (digital telephone answering device), analog interface to DSPs (digital signal processors), and other voice-band systems that are not part of a telephone central office system.

1.4 Device Nomenclatures

All members of the TCM29Cxx and TP30xx families are available in an extended temperature range (–40°C to 85°C). These parts are indicated by a "1" in the part number, as in TCM129C13 and TP13054A. The standard temperature range (0°C to 70°C) parts that correspond to these are the TCM29C13 and the TP3054A. The QCombo (TCM38C17) is currently available in the extended temperature range, and the Combo III (TCM37Cxx) is available in the standard temperature range.

In addition, most TCM29Cxx and all TP30xx devices are available with or without a supplementary, TI-patented, idle-channel noise reduction circuit. This circuit provides improved noise performance. (Details on the operation of this circuit appear in section 2.1.5, *Enhanced Noise-Reduction Algorithm*.) Members of the TCM29Cxx family that end with an "A" contain this circuit. For example, the TCM29C14A contains the enhanced noise-reduction circuit, while the TCM29C14 does not.

Noise-reduced members of the TP30xx line are not as easily identified and are better classified in table form. Table 1 shows which TCM29Cxx and TP30xx devices have the noise-reduction algorithm and which do not.

Table 1. TCM29Cxx and TP30xx Combo Devices With and Without Enhanced Noise Reduction

COMBOS WITH NOISE REDUCTION	COMBOS WITHOUT NOISE REDUCTION
TP3054B/TP13054B	TP3054A/TP13054A
TP3057A/TP13057A	TP3057B/TP13057B
TP3064B/TP13064B	TP3064A/TP13064A
TP3067A/TP13067A	TP3067B/TP13067B
TCM29C13A/TCM129C13A	TCM29C13/TCM129C13
TCM29C14A/TCM129C14A	TCM29C14/TCM129C14
TCM29C16A/TCM129C16A	TCM29C16/TCM129C16
TCM29C17A/TCM129C17A	TCM29C17/TCM129C17
	TCM29C18/TCM129C18
	TCM29C19/TCM129C19
	TCM29C23/TCM129C23
TCM37C13A	TCM37C14
	TCM37C15

While most applications benefit from the enhanced noise-reduction algorithm, certain applications show better performance using devices without the algorithm. See section 2.1.5, *Enhanced Noise-Reduction Algorithm*, for more information about which device is more suitable for a given application.

1.5 TI Combo Development Roadmap

TI continues to expand and improve its combo offering. A roadmap for TI combo development is shown in Figure 4.

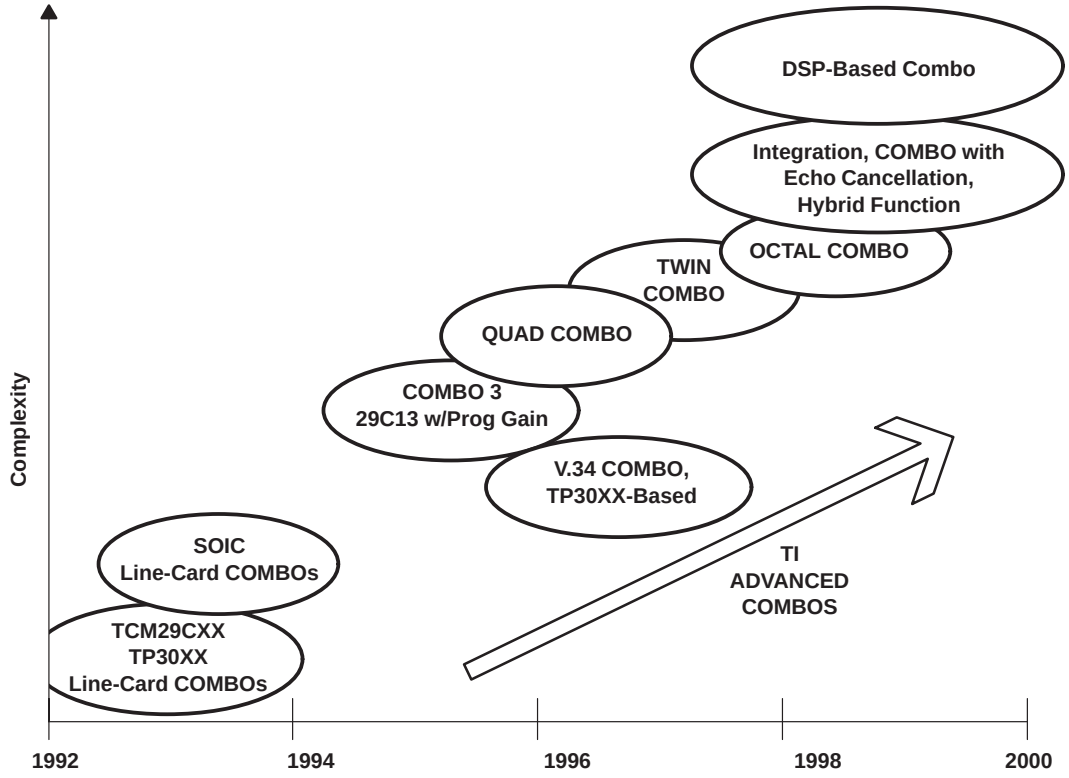


Figure 4. TI Combo Roadmap

1.6 Typical Application Environments

To better understand the nature of combo device application, it is helpful to understand the different kinds of environments in which they operate.

1.6.1 Central Office Line-Card Applications

Combos are designed for use on telephone company central office line cards. Line cards provide the signal and control interface between a telephone subscriber and the telephone company central office (Class 5 office). They convert the analog subscriber signal to digital PCM (pulse code modulation) data in the appropriate format (see section 1.6.2, *Public Telephone PCM Formats*) for out-going signals, and from PCM to analog for in-coming signals sent to the subscriber. Line-cards may be located at the central office, or they may be located at a line concentrator between the subscriber and the central office (see Figure 5).

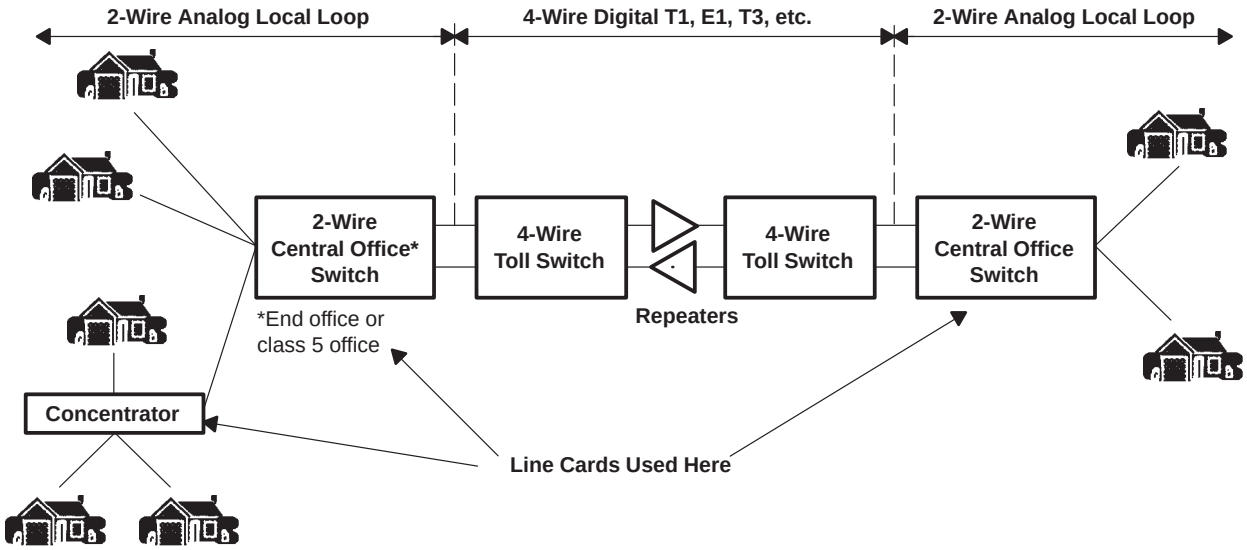


Figure 5. Line-Card Locations in a Telephone System

The basic functions of a line card are known as the BORSCHT functions, which are Battery Feed, Overvoltage Protection, Ringing, Supervision, Coding, Hybrid, and Test:

- **Battery Feed:** The line card must provide a dependable supply voltage to the subscriber, typically – 48 Vdc. The two wires that run to the subscriber are called TIP and RING. These wires form a circuit between the central office and the subscriber phone. When the subscriber phone is taken off of the hook, the circuit is completed. This circuit is called a *local loop* and the resulting current is called the *loop current.*
- **Overvoltage Protection:** The system must be protected from dangerous transient voltages caused by lightning, surges, and influences from electric utility power lines, such as induced voltages and short circuits. Good overvoltage protection must be reliable over the long term, does not false-trigger or clip, automatically resets when the transient subsides, presents low line-loading during normal operation, and remains low-maintenance. The TI TCM1030 and TCM1060 Dual Transient Voltage Suppressors meet these criteria and are recommended for line-card design. See the 1996 edition of the TI *Wireless and Telecommunications Products Data Book* for further information.
- **Ringing:** When the subscriber is being called, the line card must send a voltage on TIP and RING that causes the telephone to ring. The ringing voltage is typically 90 Vrms at 20 Hz.
- **Supervision:** Line cards must be able to detect changes in the loop current, such as on-/off-hook detection**.**
- **Testing:** On-board test functions allow the line card to verify that the local loop is operating correctly.
- **Hybrid Balance:** Digital telecommunications networks operate on four wires, two wires for the transmit direction and two wires for the receive direction. In contrast, subscriber telephone lines use only two wires (TIP and RING), and the signals going in both directions are fully duplexed on these two wires. The hybrid function interfaces the 2-wire and 4-wire analog systems on the line-card.
- **Coding/Filter:** The line card must perform bidirectional analog/digital conversion and the filtering necessary to prevent aliasing in the conversion, interfacing the 4-wire analog signals to the 4-wire digital PCM highway. This is accomplished with a combo circuit, such as TI's TCMxxCxx and TP30xx devices, which is the subject of this document.

A block diagram of a line card is shown in Figure 6.

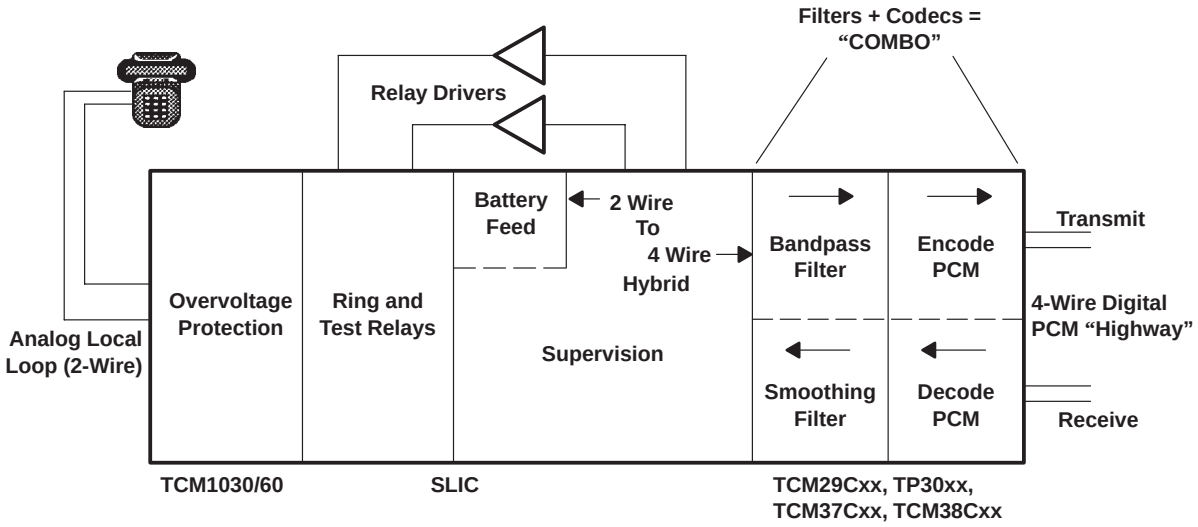


Figure 6. Line-Card Block Diagram and Functions

1.6.2 Public Telephone PCM Formats

Combos are designed to be interfaced to digital PCM telephone networks, which can be either of two types. A T1 network operates at 1.544 MHz and provides time-division-multiplexing (TDM) of 24 voice-band channels. Each of these channels contributes 8 bits of data, 8000 times in 1 second, in its appropriate time slot. Therefore, a single T1 frame (also known as a DS–1 frame) consists of $24 \times 8 = 192$ bits, plus a synchronization bit. This means that 193 bits are transmitted 8000 times a second, for a total of 1 544 000 bits (see Figure 7).

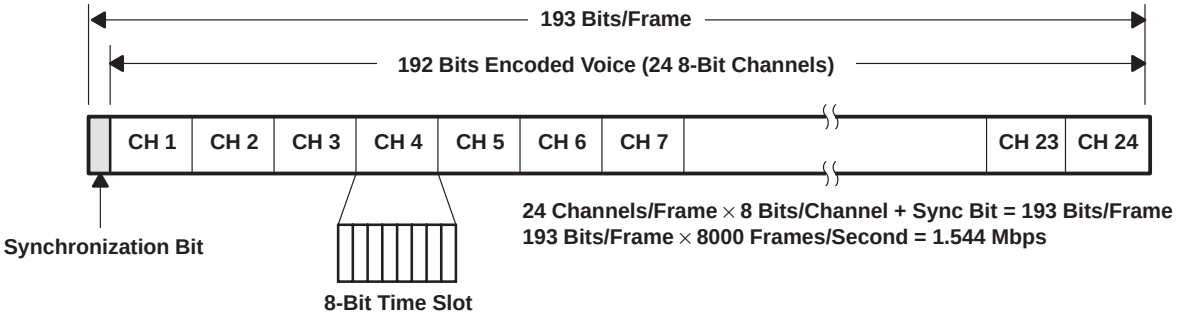


Figure 7. A T1 PCM Frame

T1 networks are used primarily in North America and Japan.

In contrast, much of the rest of the world uses a network known as PCM–30, which operates at 2.048 MHz. This system is also known as an E1 system and multiplexes 30 voice-band channels, each contributing 8 bits of data, 8000 times in 1 second, in its appropriate timeslot. A PCM–30 frame consists of thirty-two 8-bit bytes. The first byte is a framing byte, and is used for synchronization. The next 15 bytes belong to the first 15 voice-band channels. Following this is a byte used for signaling and then the remaining 15 voice-band channel bytes. As with T1, this is the format for a single frame, and it occurs 8000 times a second (see Figure 8).

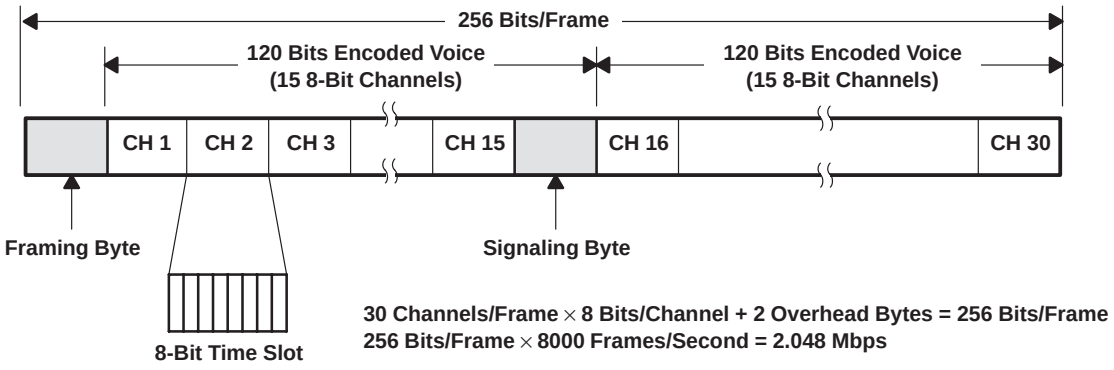


Figure 8. A PCM–30 Frame

All networks connected to the PSTN (public switched-telephone network) operate synchronously at the appropriate rate for their type (T1 or E1). At a digital end office, where the digital data is converted to analog, this clock is divided down to generate frame syncs. The frame sync assigns a channel its time slot within the frame.

Upon receiving a frame sync, a combo sends its 8 bits of data at 1.544 MHz or 2.048 MHz (depending on the system), and then waits for its next frame sync. During this time, frame-sync pulses are being generated for the remaining channels, each in the appropriate time slot. While the combo waits, it samples the analog signal and converts it to digital data, which is placed in the output buffer until the next frame sync.

1.6.3 PABX Applications

Combos are also used in PABX (Private Automated Branch eXchange) systems. A PABX is a local digital telephone network that provides telephone service for a building or contained area. Since these systems are digital and must communicate with the outside world, which uses the conventional 2-wire TIP and RING interface, they must contain all BORSCHT functions in-system, much like a central office line card. For this reason, PABXs also require combo functionality. However, they do not need to meet all CCITT recommendations.

1.6.4 Other Applications

Other common combo applications include DTAD (digital telephone answering device), voicemail systems, and other voice-band communications systems.

2 DEVICE OPERATION

Each combo channel has both a transmit path and a receive path. The transmit path has an analog input, ANLGIN/VFXI, and digital output, PCMOUT/DX. Analog data applied to the input is converted to digital PCM format and transmitted out of the digital output. Each receive path has a digital input, PCMIN/DR, and an analog output, PWRO/VPO. Digital data applied to the digital input is converted to an analog signal and transmitted out of the analog output. To minimize crosstalk, TI combo designs use independent converters, filters, and voltage references for the transmit and receive paths.

2.1 Transmit Path

The transmit path includes an analog input amplifier, filters, A/D conversion and encoding, and an autozero circuit. A block diagram of the transmit path is shown in Figure 9.

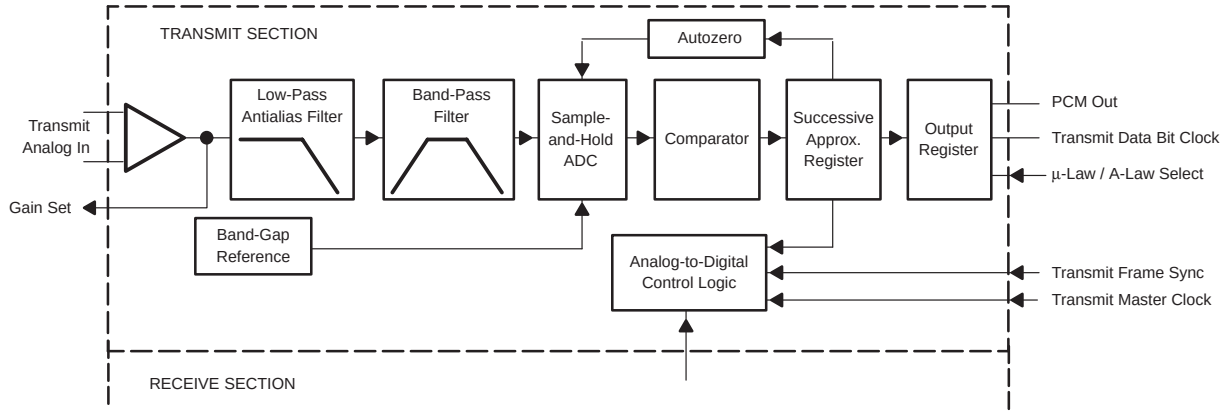


Figure 9. Transmit Path Block Diagram

2.1.1 Analog Input Amplifier

The analog input signal is first amplified by an uncommitted operational amplifier with its output signal also connected to the GSX terminal. The amplifier gain can be set by creating a feedback loop. For example, Figure 10 shows a typical application in which two external resistors, the GSX terminal, and the inverting input terminal are used to create an inverting input amplifier. Gain (A_V) can be set by changing the RF/RI ratio.

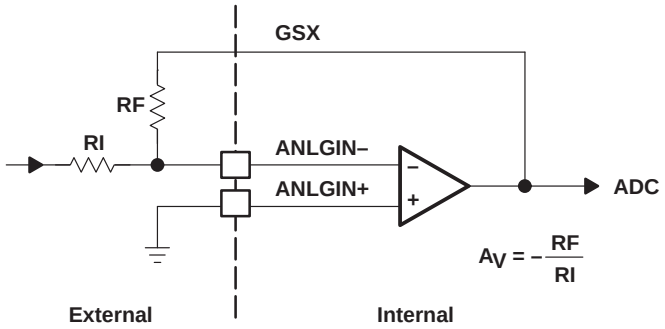


Figure 10. Typical Transmit Path Gain Setting Circuitry

2.1.2 Transmit Filters

The amplified signal is passed through antialiasing and band-pass filters. The antialiasing filter is an analog (continuous time) third-order low-pass filter with a cutoff frequency of 20 kHz. It is used to attenuate any modulation components above one-half of the sampling frequency of the next stage to avoid aliasing artifacts (Nyquist sampling theorem). Since the next filter stage samples at 256 kHz, the antialiasing filter is designed to provide attenuation greater than 27 dB at one-half of that sampling frequency, or 128 kHz.

The band-pass filter is composed of two switched-capacitor filter stages that are oversampled to avoid the effects of aliasing. The first stage is a sixth-order low-pass filter with a 3-dB cutoff frequency of 3.5 kHz, sampled at 256 kHz. The second stage is a third-order high-pass filter with a cutoff frequency of 100 Hz sampled at 8 kHz. The effective 0-dB pass band of these filters is 300 Hz to 3.4 kHz. The oversampling and the clocks used by these filters are synchronous so that antialiasing products can be easily controlled and virtually eliminated.

2.1.3 Encoding (A/D Conversion)

All digital data transmitted by a combo device is companded (and it expects all received data to be companded also). The filtered analog input signal is applied to a compressing analog-to-digital converter (COADC) where it is encoded into an 8-bit digital representation using either the μ-law or A-law encoding schemes set forth by CCITT G.711. See section 2.4, *Companding*, for more information on companding formats and section 2.3, *Timing and Clocking*, for more information on how data is clocked into and out of the device.

The encoder samples the filtered analog signal at the middle of the frame and holds the sample on an internal sample-and-hold capacitor. The encoder uses a switched-capacitor array to convert the analog sample to digital data, a process that also starts in the second half of the frame. To minimize the delay across the combo device, the actual conversion process does not complete until immediately before the next frame. Digital data representing the sample is then transmitted at the start of the next frame. Transmit data is clocked out of the PCMOUT/DX terminal on consecutive positive transitions of the transmit data clock. For the TCMxxCxx combo family, this terminal is CLK or MCLK in the fixed-data-rate mode and DCLKR in the variable-data-rate mode. For the TP30xx combo family, the terminal is BCLKX.

The sign bit is transmitted first, followed by the MSB, with the LSB transmitted last (see section 1.6.2, *Public Telephone PCM Formats*, for a more in-depth description of the output digital data). Since the A/D conversion rate is equal to the master clock rate and the switched-capacitor band-pass filter clocks are integer submultiples of the master clock, unwanted aliasing products are prevented.

2.1.4 Transmit Autozero

The autozero circuit corrects for any dc offset on the input signal to the encoder using a sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and then subtracted from the input to the encoder. This acts as a form of feedback to track and correct changing dc offsets. The autozero circuitry is implemented after the high-pass transmit filter so that it does not mistakenly track low-frequency audio signals. It takes approximately 5 frames for the autozero circuitry to respond after device powerup, or when the device goes from standby to active mode.

2.1.5 Enhanced Noise-Reduction Algorithm

In some TI combo devices, a patented noise-reduction algorithm reduces idle-channel transmit noise to extremely low levels (see section 1.4, *Device Nomenclatures*, for a list of the devices that contain this circuit). This circuit reduces the transmit path audio when the analog input falls below a certain level. The level at which the noise-reduction circuit is enabled is approximately −55 dBm0 to −60 dBm0. Hysteresis in this threshold allows the noise-reduction circuit to dynamically adjust to the input signal level. When the device detects these very-low-level audio input conditions, it outputs a zero code (1111 1111 in μ-law, 0101 0101 in A-law, in accordance with CCITT G.711 recommendations). When operated with very low input signals, devices without this noise-reduction circuit typically output a random sequence of codes around zero (LSB and/or second LSB, and MSB sign bit toggling arbitrarily). The purpose of this circuit is to reduce or eliminate noise generated internally within the combo transmit path when it is idle. It is not intended to reduce noise already present in signals applied to the transmit input.

In most applications, particularly line cards, the combo devices that contain this circuit provide the best performance. However, some applications perform better using combo devices that do not have the reduced-noise algorithm. In general, it is recommended that the noise-reduced versions be used in all applications except those in which input signal levels lower than –55 dBm0 are critical to device performance.

2.2 Receive Path

For the TCM29Cxx family of codecs, data can be received in either a fixed- or variable-data-rate mode. The TCM37Cxx family and the TCM38C17 receive data in fixed-data-rate mode only. The TP30xx family can receive data in synchronous or asynchronous modes (that is, transmit clocks can be operated synchronously or asynchronously with the receive clocks).

The receive path includes a D/A converter, receive filters, and an audio output amplifier. A block diagram of the receive path is shown in Figure 11.

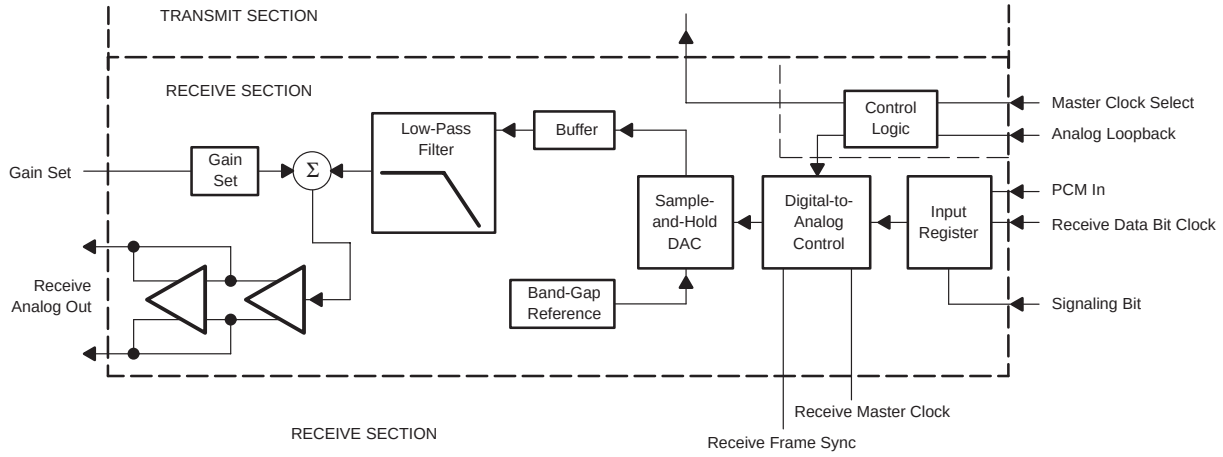


Figure 11. Generalized Combo Block Diagram

2.2.1 Decoding (Companding D/A Conversion)

For all combo device families, the serial data word is received at terminal PCMIN/DR. The decoding section converts the received 8-bit PCM data into an analog signal with 12 bits of dynamic range, in accordance with CCITT G.711. Input data is clocked in on the first 8 negative transitions of the receive clock following FSR. The receive clock is CLKR for the TCMxxCxx combo device family in the fixed-data-rate mode, DCLKR for the TCMxxCxx family in the variable-data-rate mode, and BCLKR for the TP30xx family of combo devices. D/A conversion is then performed and the resulting analog sample is held on an internal sample-and-hold capacitor. The sample is then transferred to the receive filter during the next frame.

2.2.2 Receive Filters

The receive filter is a switched-capacitor sixth-order low-pass filter with a 3 dB-down cutoff frequency of approximately 3.5 kHz and provides pass-band flatness and stop-band rejection that fulfills both the AT&T D3/D4 specifications and CCITT recommendation for G.712. The filter also contains correction for the (sin x)/x response of such decoders.

2.2.3 Receive Output Amplifier

All TI combo devices incorporate a versatile analog output power amplifier that can drive transformer hybrids or low-impedance loads. Devices in the TCMxxCxx and TP306x families have output amplifiers that can operate in either a single-ended or differential configuration. TP305x devices use only a single output terminal, VFRO, to transmit the received analog signal, and the gain of their output amplifiers is not adjustable.

The output amplifier stage of the TCMxxCxx and TP306x devices, however, can have their gain adjusted by the connection of a resistor chain to the output terminals of the device. The inverting operational amplifier can drive a 600-Ω load in parallel with 100 pF. The details of setting the gain of the receive output amplifier are different for TCM29Cxx, TCM37Cxx, TCM38C17, and TP306x combo devices, and they are addressed separately in the following paragraphs.

2.2.3.1 TCM29Cxx and TCM38C17 Receive Output-Amplifier Gain Setting

Figure 12 is a representation of the internal structure of the output amplifier of TCMxxCxx combo devices.

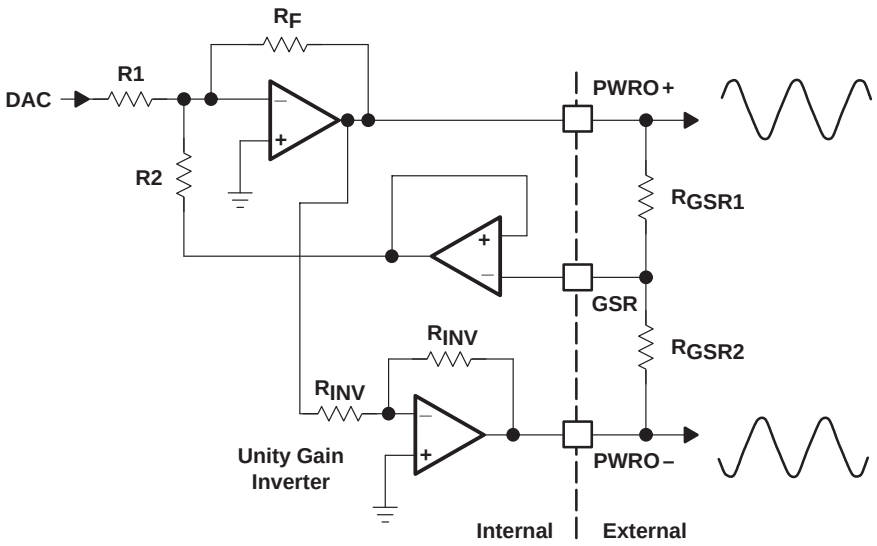


Figure 12. Output-Amplifier Architecture of the TCMxxCxx Family

Various receive output-amplifier configurations are detailed in the following paragraphs.

2.2.3.1.1 Differential Configuration

For connection to a transformer, the fully-differential configuration is recommended to provide maximum possible output (voltage swing) to the primary of an attached transformer. Figure 13 shows the combo in a fully differential mode.

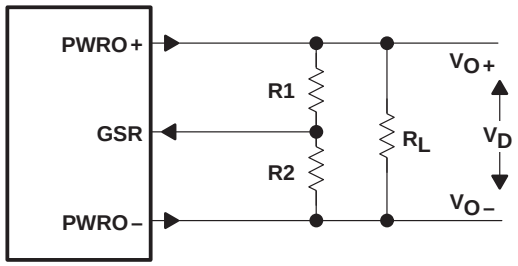


Figure 13. Fully Differential Gain-Setting Configuration

PWRO+ and PWRO– are low-impedance complementary outputs. The total output available for the output load (R_L) is then $V_D = V_{O+} - V_{O-}$. R1 and R2 form a gain-setting resistor network with a center tap connected to the GSR input.

R1 + R2 should be greater than 10 kΩ and less than 100 kΩ because the parallel combination R1 + R2 and R_L sets the total loading. The total parasitic capacitance of the GSR input, along with the parallel combination of R1 and R2, define a time constant that must be minimized to avoid inaccuracies in the gain calculations.

The resistor gain control actually consists of attenuating the full differential output voltage. The equation to determine the value of the attenuation constant is given in equation 1.

$$A = \frac{1+\left(\frac{R1}{R2}\right)}{4+\left(\frac{R1}{R2}\right)} \quad (1)$$

which can also be expressed as shown in equation 2.

$$A = \frac{R1+R2}{4\left(R2+\frac{R1}{4}\right)} \quad (2)$$

where A = attenuation constant

Depending on the values of gain-setting resistors R1 and R2, the attenuation constant (A) can have a value of 0.25 to unity (1), or approximately 12 dB of voltage adjustment.

Maximum output (A = 1) can be obtained by maximizing R1 and minimizing R2. This can be done by letting R1 = infinity and R2 = 0 Ω (common GSR and PWRO–), as shown in Figure 14. Approximately 6.14 Vpp of output can be expected in this configuration. See section 2.5, *Analog Signal Levels and Gain Analysis*, for more detail on the digital in required for maximum analog output.

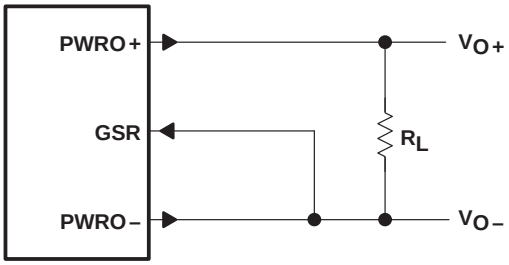


Figure 14. Fully Differential Maximum Gain-Setting Configuration (A = 1)

Figure 15 illustrates the combo device with the resistor gain-control setting for an attenuation of A = 0.625.

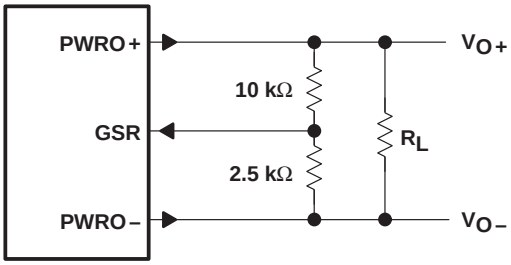


Figure 15. Fully Differential Mid-Gain-Setting Configuration (A = 0.625)

As shown in Figure 16, a minimum output (A = 0.25 dB) can be obtained by letting R1 = 0 Ω (common GSR and PWRO+), and R2 = infinity.

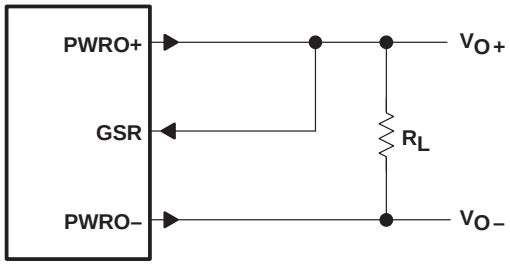


Figure 16. Fully Differential Minimum-Gain-Setting Configuration (A = 0.25)

2.2.3.1.2 Single-Ended Configuration

Figure 17 shows the combo device in a typical single-ended configuration. Either of the outputs can be connected through the load to ground, achieving an output voltage swing that is one-half of the fully differential output voltage swing. Gain is set by manipulating the resistor network in the same way as detailed for the differential mode. The single-ended mode is most commonly used when interfacing to a succeeding stage that is referenced to ground.

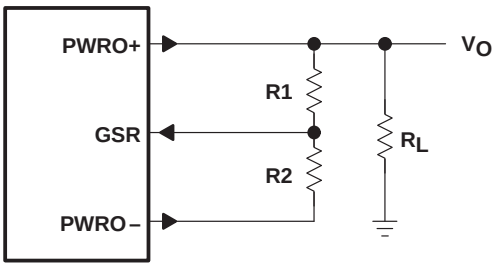


Figure 17. Single-Ended Configuration

2.2.3.2 TCM37Cxx Receive Output-Amplifier Gain Setting

The TCM37Cxx (Combo III) devices employ a programmable gain setting technique by which three different gain settings can be selected using a 2-pin parallel logic scheme. The designer selects an external resistor network, the individual resistors of which are then switched into or out of the feedback loop in various combinations by internal logic switches controlled by the two control input terminals, GS0 and GS1. By changing the logic signals on GS0 and GS1, the system can be configured for varying degrees of gain or attenuation.

Gain setting for the Combo III is covered in detail in the TCM37Cxx data sheet.

2.2.3.3 TP306x Receive Output-Amplifier Gain Setting

Figure 18 is a representation of the internal structure of the output amplifier of the TP306x combo family.

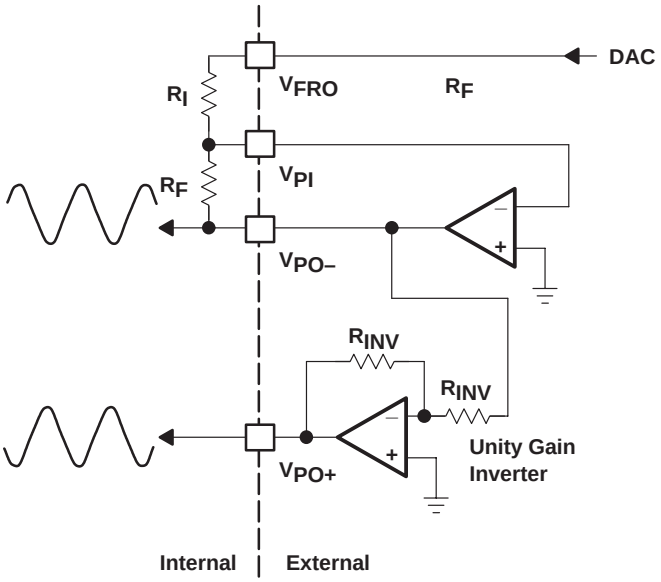


Figure 18. Output-Amplifier Architecture of the TP306x Family

The primary amplifier uses R_F and R_I to set the gain in an inverting amplifier configuration. The output signal is also routed through an inverting amplifier with unity gain. Together, they create an output with a gain determined by equation 3.

$$A = 2\left(\frac{R_F}{R_I}\right) \tag{3}$$

R_I should have a minimum resistance of 10 kΩ.

2.3 Timing and Clocking

Combos require three distinct clock signals: the master clock, the data bit clock, and the frame sync. The master clock is used internally for various functions. In particular, it is required for the on-chip switched-capacitor filters and the A/D and D/A conversion processes. The master clock signal should be applied to the MCLK/(CLKX/CLKR)/MCLKX terminal.

Three standard master clock rates (1.536 MHz, 1.544 MHz, and 2.048 MHz) are used with TI combo devices. Some devices support all three master clock rates, which are selectable by applying different voltage levels to clock-select terminal CLKSEL, while others support only a single clock rate, which is usually 2.048 MHz or 1.536 MHz (see Figure 2 and Figure 3).

The data bit clock is used to clock data into and out of the device. In the TCMxxCxx devices, this is only necessary in variable-data-rate mode, since a device operating in fixed-data-rate mode uses the master clock for this function. TP30xx devices require the data bit clock to be applied to the BCLKX terminal, but this terminal can easily be tied to the master clock externally to create the equivalent of a TCMxxCxx fixed-data-rate mode. In general, this type of configuration is easier to implement.

Frame sync pulses signal the combo device to begin clocking digital data into or out of the device. At the same time, the frame sync pulses control the sampling frequency. The standard frequency for the frame sync clock is 8 kHz. This 8 kHz rate is based on the Nyquist rate for voice band, which is 300 Hz to 3.4 kHz.

2.3.1 Effect on Pass-Band Parameters

Internally, the master clock is divided down to a signal that drives the switched-capacitor filters. The divide ratio is selected with the CLKSEL terminal. Since this clock originates from the master clock, the filter characteristics are directly related to the master clock. Operating a combo device at the master clock rate specified by the CLKSEL terminal yields an effective 0 dB pass band of 300 Hz to 3.4 kHz in the transmit channel, which corresponds to 3-dB cutoff points of 120 Hz and 3.5 kHz. Increasing or decreasing the master clock frequency linearly scales this pass band up or down the frequency domain. For example, if a combo device is configured for a 2.048-MHz master clock, and instead it is fed a 4.096-MHz clock, the high-pass cutoff shifts from 300 Hz to 600 Hz, and the low-pass cutoff shifts from 3.4 kHz to 6.8 kHz, as shown in Figure 19.

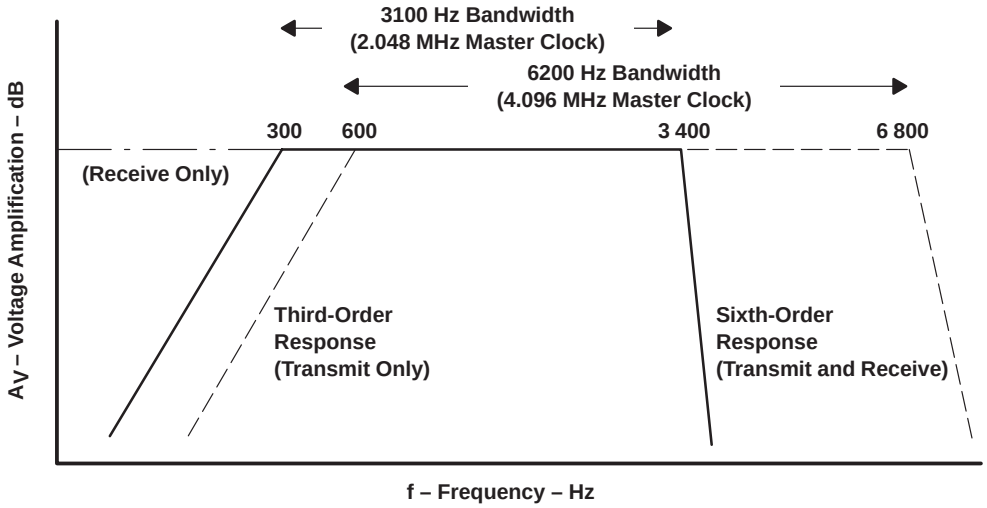


Figure 19. Master Clock Frequency Effect on Filter Characteristics

The receive channel is the same as the transmit channel in regard to filter effects related to master clock frequency, except there is no high-pass filter and the combo device has approximately 0 dB filter response at frequencies below 300 Hz.

By using the formula given in equation 4, the absolute cutoff frequency can be found for any new master clock frequency.

$$\text{Absolute cutoff frequency (kHz)} = \frac{(\text{normalized cutoff freq in kHz}) \times (\text{new MCLK})}{\text{original MCLK}} \quad (4)$$

where:
Absolute cutoff frequency is the new scaled cutoff frequency
Normalized cutoff frequency is the specified cutoff frequency at the original master clock
New MCLK is the new master clock frequency

A designer wishing to use nonspecified master clock frequencies should take this change in filter characteristics into consideration during system design. However, other clocks must be changed simultaneously in order to maintain acceptable performance. See section 2.3.2, *The Relationship Between Master Clocks, Data Bit Clocks, and Frame Syncs* for more details.

2.3.2 The Relationship Between Master Clocks, Data Bit Clocks, and Frame Syncs

Since much of combo device configuration involves the clocking and timing of the device, it is important for the designer to understand how the master clock, data clock, and frame syncs interact. TI specifies that master clocks be 1.536 MHz, 1.544 MHz, or 2.048 MHz depending on which TI combo device is under consideration and how is configured with the CLKSEL input. Data bit clocks are specified to operate between 64 kHz and 2.048 MHz, and frame syncs are specified to operate at 8 kHz. Combos are optimized to operate within these specifications and improper device behavior may be observed if the guidelines in this section are not followed. However, the designer may at times wish to use clock speeds other than those specified. The principles in the following sections govern the interaction between combo device clock signals.

Note that for TCMxxCxx devices operating in fixed-data-rate mode, references to data bit clocks also refer to the master clock, since these clocks are shared in that mode.

2.3.2.1 Data Bit Clock vs. Frame Syncs

The data bit clock is not specified to be run at less than 64 kHz. The reason is that a combo device, sampling at 8 kHz, generates 8 bits of data, 8000 times a second, resulting in 64 000 bits a second. A data bit clock of less than 64 kHz would not permit the combo to transmit all of its data. The only way it would be possible to run a data clock at less than 64 kHz is to slow the sampling rate (frame syncs) down proportionally. For example, if the frame syncs are to be operated at 6 kHz, the data bit clock could be slowed to $8 \times 6000 = 48$ kHz. Note that the minimum data-clock-to-frame-sync ratio remains 8:1, as in 64 kHz ÷ 8000 Hz.

If the designer decides to use this procedure, it is imperative that the master clock rate is lowered proportionally to the decrease in frame sync frequency. In addition to the reasons listed in section 2.3.2.3, *Master Clock vs. Frame Syncs*, it is required to prevent frequencies greater than half of the sampling frequency from entering the ADC.

2.3.2.2 Master Clock vs. Data Bit Clock

Data clocks do not need to be submultiples of the master clock. However, they must be synchronized at the beginning of each frame.

2.3.2.3 Master Clock vs. Frame Syncs

There is an important relationship between the master clock and frame sync rates due to the role that master clocks play in the conversion and filtering processes.

2.3.2.3.1 The Need for Proper Master-Clock-to-Frame-Sync Ratio

It is strongly recommended that a fixed ratio be maintained between master clock and frame sync frequencies (see section 2.3.2.3.2, *Calculating the Correct Master-Clock-to-Frame-Sync Ratio*, for more information). Deviating from this guideline will induce one or both of the following effects.

The first effect occurs when the ratio is too low. The clock that operates the codec is subdivided from the master clock. If the rate produced by this divide operation is too low relative to the frame sync rate, the converter will not finish before the next frame sync arrives. This will be seen in the form of blank data at the end of each output PCM byte. To prevent this from happening, the ratio should not be lowered beyond the one specified.

The other effect occurs when this ratio is either too high or too low. The receive filter has built-in (sin x)/x correction to compensate for sampling-induced pass-band droop. This droop pattern is a function of the sampling frequency (frame sync). If the frame sync frequency and master clock frequency are not kept in the correct ratio, the (sin x)/x compensation will occur at the wrong frequencies, impacting performance.

2.3.2.3.2 Calculating the Correct Master-Clock-to-Frame-Sync Ratio

To ensure that these negative effects do not occur, the designer must calculate the correct master-clock-to-frame-sync ratio for a given master clock selection (selected with CLKSEL). For example, a combo device configured for 2.048 MHz master clock operation has a ratio of 2.048 MHz ÷ 8 kHz, or 256. It is possible to use a sampling rate higher or lower than 8 kHz, assuming the master clock rate is increased or decreased to maintain the master-clock-to-frame-sync ratio. To increase the sampling (frame sync) rate to 9.6 kHz, the device must be configured for 2.048 MHz master clock operation, and the master clock applied must be increased according to the ratio as given in equation 5.

$$\frac{2.048\ \text{MHz}}{8\ \text{kHz}} = 256 = \frac{\text{new MCLK}}{9.6\ \text{kHz}} \tag{5}$$

and the master clock becomes 2.458 MHz.

Note that as the master clock (and frame sync) frequency increases beyond two times the selected rate, degradation in performance occurs. This corresponds to a sampling rate of 16 kHz, a master clock of 4.096 MHz, and a pass band of 600 Hz to 6.8 kHz. For some applications, the combo device may be considered usable when operating with a master clock of up to three times the selected rate.

2.3.2.4 Transmit Clocks vs. Receive Clocks

The TCM29C14, TCM29C14A, TCM129C14, and TCM129C14A at one time were specified as supporting asynchronous operation; the transmit and receive clocks could operate independently. However, this option is no longer supported. It is now recommended that CLKX and CLKR be connected externally. Other TCMxxCxx devices combine CLKX and CLKR on a single terminal. Also, better performance may be obtained when DCLKX and DCLKR operate synchronously with each other.

While asynchronous operation is possible with TP30xx devices, it is not recommended. MCLKX and MCLKR can be internally tied together by applying only a logic low to MCLKR (or high when the device is to be powered down). For best performance, BCLKX and BCLKR should operate at the same rate (synchronous mode).

2.3.3 Intel vs. National Timing

TCMxxCxx combo devices and TP30xx combo devices use different frame sync formats. Timing for the TCMxxCxx family is called *Intel timing*, while timing for the TP30xx family is called *National timing*. The timing specifications for these devices were originated by Intel and National Semiconductor respectively. Neither format is superior to the other, even in specific applications. Rather, the modes and frame syncs of the families simply differ. The best way to see this difference is to study the data sheets for a TCMxxCxx and a TP30xx device. However, some differences are noted here.

TCMxxCxx devices allow the master clock to be used as the data bit clock, eliminating the need for an external data clock connection. This is fixed-data-rate mode (for TCM37Cxx devices and the TCM38C17, this is the only mode supported). Data clock terminals DCLKR/DCLKX are also supplied on TCM29Cxx devices, and these are used in variable-data-rate mode. In this mode, a separate data clock within the range of 64 kHz to 2.048 MHz can be used to transmit and receive the data. In contrast, all TP30xx devices effectively run only in variable-data-rate mode, since they always require a bit clock on terminal BCKLX and allow data transfer at rates between 64 kHz and 2.048 MHz.

TP30xx devices have separate transmit and receive clock terminals, which can be internally tied together forcing the device into the synchronous mode. When the designer wishes to operate the transmit and receive data bit clocks at different rates, separate clocks may be applied to BCLKX and BCLKR, and the device operates in asynchronous mode. In contrast, TCM29Cxx devices operating in variable-data-rate mode effectively run only in asynchronous mode, in that the data bit clocks DCLKX and DCLKR terminals both require a clock when operating in the variable-data-rate mode. TCM29Cxx devices operating in fixed-data-rate mode effectively run only in synchronous mode because CLKX and CLKR are the same terminal on most TCM29Cxx devices (On the TCM29C14, it is recommended that the separate CLKX and CLKR terminals be externally tied together). This is true of TCM37Cxx devices and the TCM38C17 as well because these devices only operate in fixed-data-rate mode.

Frame syncs are used differently by Intel and National timing combo devices. On TCMxxCxx devices, short frame syncs, only one master clock period long, are used for fixed-data-rate mode. In effect, it triggers the transfer of eight data bits out of the PCMOUT terminal or into the PCMIN terminal. On a TCM29C14 device (or derivative), when a short frame sync is two master clock periods long, this indicates a signaling frame. This means that the frame being transmitted is carrying a data signal on the eighth bit, which is input on the SIGX terminal of a transmitting combo and output on terminal SIGR of a receiving combo. Long frame syncs are used in variable-data-rate mode. While the frame sync is high, data is clocked in or out on the next eight consecutive positive transitions of the master clock or data clock (depending on the operating mode).

TP30xx devices also use short and long frame syncs, but they are defined differently and indicate different modes. Like the Intel-timing devices, a short frame sync is one master clock period long. It triggers the data transfer in much the same way as the Intel-timing devices operating in fixed-data-rate mode. When a TP30xx combo receives a long frame sync (three or more bit clock periods long), it enters the long frame sync mode. In this mode, the output terminal DX or input terminal DR remain active until after the eighth bit is transmitted/received, or until the frame sync returns low, whichever occurs later. This is quite similar to the way long frame syncs are used on Intel-timing combos, except that for an Intel-timing combo, a long frame sync must be used with variable-rate-mode, and short frame syncs must be used with fixed-data-rate mode. National-timing combos can use either short or long frame syncs in any mode.

2.4 Companding

Compander is a shortened term for COMpressor/exPANDER. It is a way of processing PCM data before it enters the PCM highway, and is used in essentially all PSTN (public switched telephone network) systems. North American and Japanese systems use the μ-law companding algorithm, while European networks use the A-law companding algorithm.

2.4.1 Purpose of Companding

The reason companding is widely implemented in digital communications networks is that it reduces the data flow necessary to reproduce the analog signals from which the data was generated. It redistributes conversion resolution more efficiently so that less conversion resolution is used at higher amplitudes; and more resolution is used at lower amplitudes. This reduces the total number of bits per sample.

As an example of how this is more efficient, consider listening to someone whispering on the phone. Clarity is very important. Any noise present on the line seems large relative to the voice signal (due to smaller signal-to-noise ratio). On the other hand, imagine listening to someone shouting over the phone. Noise is relatively insignificant, because it is small compared to the large amplitude of the person shouting. Clarity is not as necessary because of the high volume, and any noise is small relative to the signal.

Quantization noise is the natural result of codec operation (sampling and reconstruction). The higher the resolution, the lower the noise, and vice versa. Since clarity and high signal-to-noise are more important at low amplitudes than at high ones, why not distribute resolution (and, therefore, low noise) accordingly? This is what companding does. Instead of having high resolution across the amplitude range, high resolution is only used at low amplitudes. Lower resolution is used at high amplitudes, reducing the number of bits (and, consequently, bandwidth) necessary to reproduce the signal.

2.4.2 Companded Byte Structure

For both μ-law and A-law formats, a PCM byte is arranged as shown in Figure 20.

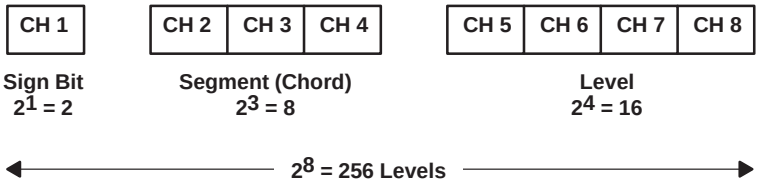
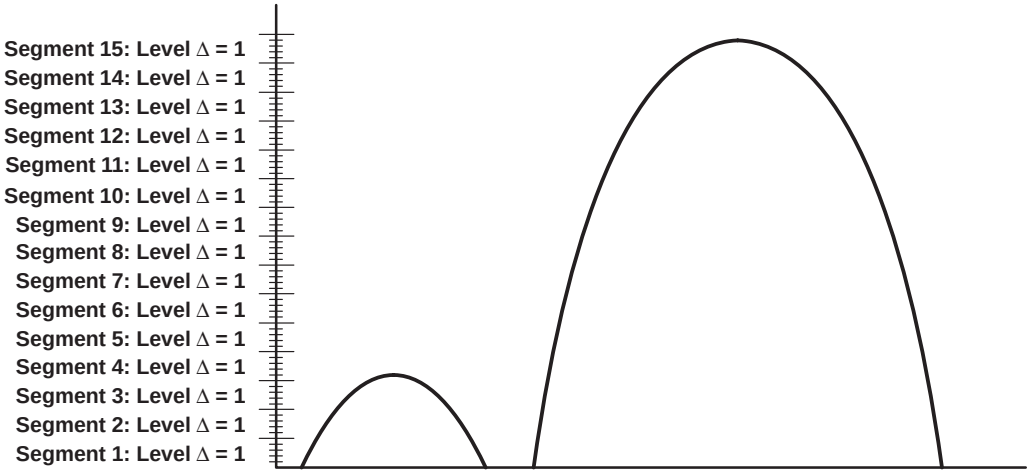


Figure 20. A Companded PCM Byte

The first bit is a sign bit. For both formats, a sign bit of "1" indicates a positive value, while a "0" indicates a negative value. Bits 2–4 represent the segment (also known as the chord). Both formats have a total of eight segments in both the positive and negative regions ($2^3 = 8$) for a total of 16 segments. Within each segment, resolution is continuous. That is, for a given segment, all A/D and D/A decision levels are equally spaced. At segments closest to the middle of the signal range, the resolution is the highest. Each segment moving outward to the upper and lower amplitude extremes uses lower resolution.

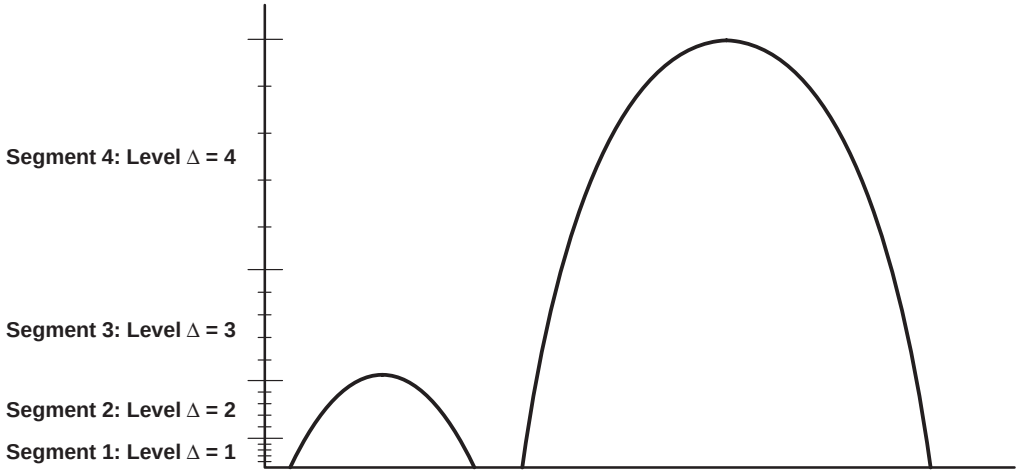
To view this graphically, see Figure 21, which represents a generalized linear conversion scheme. Note that all decision levels are equidistant and that in order to maintain this equidistance, a total of 75 decision levels are required. A 7-bit data word would be necessary to represent this value. The number of decision levels could be lessened (evenly) in order to reduce the number of bits required in the signal. But reducing the number of decision levels excessively would have severe effects on the reconstruction of small signals, as the signal-to-quantization-noise ratio would begin to increase.



NOTE A: Total number of levels = 75. It requires 7 bits.

Figure 21. Decision-Level Resolution for a Linear Scheme

Compare Figure 21 to Figure 22, which represents a generalized companding scheme. Note that decision levels are equidistant within each segment but that each segment moving upward uses lower resolution. As a result, only 16 decision levels are needed. A 4-bit data word would be sufficient to represent one sample.



NOTE A: Total number of levels = 16. It requires 4 bits.

Figure 22. Decision-Level Resolution for a Generalized Companding Scheme

Note that companding does not change the amplitude of the signals. The reconstructed signal will be an accurate reproduction of the original source. Companding is not related to the frequency of the incoming analog signal — all frequencies are companded in the same manner. Companding simply distributes resolution to where it is needed for higher signal quality.

2.4.3 Standard Formats Currently In Use

As mentioned earlier in this section, the μ-law format is in use in North America and Japan. Most other countries use the A-law format. The difference between these standard formats is in the way the redistribution of resolution takes place. The μ-law format places higher resolution at lower amplitudes than the A-law format does, which leaves less resolution for higher amplitudes.

These formats are defined by CCITT recommendation G.711, found in Volume III of *CCITT Digital Networks, Transmission Systems and Multiplexing Equipment, Recommendations G.700–G.956.* The digital sequences representing the low, mid, and high points of an input analog signal are shown in Table 2.

Table 2. PCM Encoding Format Low, Mid, and High Points

ANALOG INPUT	μ-LAW ENCODING	A-LAW ENCODING (includes even-bit inversion)
V_I = + Full Scale	10000000	10101010
V_I = 0	11111111 01111111	11010101 01010101
V_I = – Full Scale	00000000	00101010

2.5 Analog Signal Levels and Gain Analysis

It is important for the designer to understand the amplitude and gain associated with the signals to be applied to the analog transmit input and the signal received at the analog output. This is especially true if the end system is to be used in a central office governed by CCITT recommendations. The concepts discussed in the following section apply to both the TCM29Cxx and TP30xx combo device families. The corresponding information, however, is expressed differently in the data sheets of each family. Aspects particular to each family are discussed separately in subsequent sections.

2.5.1 TCM29Cxx and TP30xx Amplitude and Gain Considerations

Amplitude and gain considerations common to all TI combo devices are discussed in the following paragraphs.

For both device families, a precision band-gap reference voltage is generated internally and supplies all references required for operation of both the transmit and receive paths. The gain in each path is trimmed during the manufacturing process, ensuring very accurate, stable gain performance over the variations in supply voltage and temperature.

2.5.1.1 Zero Transmission Levels

First, it is necessary to understand the concept of the zero transmission level, or 0 dBm0 reference level. The zero-transmission level is the signal level at the receiver analog output of a codec when a digital milliwatt (DmW) sequence is input to the device. A digital milliwatt, or digital milliwatt sequence, is a PCM sequence defined by CCITT spec G.711. This specification is found in Volume III of *CCITT Digital Networks, Transmission Systems and Multiplexing Equipment, Recommendations G.700–G.956.*

The digital milliwatt is defined in the following manner in Vol. III:

"A sinewave signal of 1 kHz at a nominal level of 0 dBm0 should be present at any voice frequency output of the PCM multiplex when the periodic sequence of the character signals of the Table 5/G.711 for the A-law and of Table 6/G.711 for the μ-law is applied to the decoder input."

In other words, a digital milliwatt is a PCM sequence that, when converted to analog, produces a 0 dBm0 signal. This is the definition of the dBm0 unit. Table 3 combines both of the CCITT tables and shows the sequence of the eight 8-bit words for both A-law and μ-law that are defined as a digital milliwatt (bit 1 is MSB, bit 8 is LSB, and the words are input from top to bottom).

Table 3. Digital Milliwatt Sequences, A-Law and μ-Law

A–Law									μ–Law							
1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
1	0	1	1	0	1	0	0		0	0	0	1	1	1	1	0
0	0	1	0	0	0	0	1		0	0	0	0	1	0	1	1
0	0	1	0	0	0	0	1		0	0	0	0	1	0	1	1
0	0	1	1	0	1	0	0		0	0	0	1	1	1	1	0
0	0	1	1	0	1	0	0		1	0	0	1	1	1	1	0
1	0	1	0	0	0	0	1		1	0	0	0	1	0	1	1
1	0	1	0	0	0	0	1		1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0		1	0	0	1	1	1	1	0

This is the sequence defined by the CCITT; however, there are many other sequences that could define a digital milliwatt.

As stated earlier, the zero-transmission level (0TL) is the analog receiver output of the combo when the digital milliwatt sequence is applied as the receiver input. If absolute gain within the receiver path were unity, the output level 0 dBm0 would be equal to 0 dBm. Because the receiver imposes a gain on the signal, this is not the case. For this reason, the combo device data sheets specify a receiver output signal level that is generated by a digital milliwatt input with the output amplifier configured for unity gain. It is labeled as the zero-transmission-level point (0TLP). Similarly, a transmit input level is specified such that the combo generates a digital milliwatt sequence with the input amplifier configured for unity gain (which, when applied to a codec, causes 0 dBm0 to be output on the analog receiver). This is referred to as the zero-transmission-level point for the transmit path. The Bellcore LSSGR recommendation refers to the transmit zero-transmission-level point as the Encoder Level Point (ELP) and the receiver zero transmission-level-point as the Decode Level Point (DLP).

Note the different units used in describing these analog signals:

- dB is a relative measurement used for gain.
- dBm can be considered to be an absolute measurement since it is always relative to a fixed level (1 mW).
- dBm0 can also be considered to be an absolute measurement since it is always relative to a fixed level (0TL point).
- 0 dBm and 0 dBm0 are both used to specify signal power. However, they are not equivalent since their references are not equivalent. The zero-transmission-level point is not equal to 1 mW (for most codecs).

2.5.1.2 Maximum Analog Input and Output

In telephone line-card applications, maximum analog input level and output level is defined by the CCITT as 3.17 dBm0 for μ-law and 3.14 dBm0 for A-law. This means that the maximum signal that can be transmitted through a transmit or receive path is 3.17 dB relative to the zero-transmission-level point in the μ-law configuration, and 3.14 dB in the A-law configuration.

2.5.2 TCM29Cxx and TCM37Cxx

Amplitude and gain considerations for the TI TCM29Cxx and TCM37Cxx lines of combo devices are discussed in the following paragraphs.

2.5.2.1 Zero Transmission Levels for the TCM29Cxx and TCM37Cxx Lines

As an example of the TI TCM29Cxx and TCM37Cxx lines of combo devices, the TCM29C13 has been selected. In the data sheet for this device, in the *gain and dynamic range* table of the *electrical characteristics* section, the receive channel zero transmission level is specified with respect to a reference load of 600 Ω or 900 Ω for μ-law and A-law configurations. Consider a μ-law configuration with the signal referenced to a 600-Ω load. This value is specified as 5.76 dBm. This means that when the digital milliwatt is applied to the receive digital input, and the receive analog amplifier is configured for single-ended unity gain (see Note 6 of the *gain and dynamic range* table), a 5.76 dBm signal appears at the PWRO+ output as shown in Figure 23.

This power level, referenced to a 600-Ω load, can be converted to a peak-to-peak voltage as follows:

$$P_{(dBm)} = 10\log\left(P_{(mW)}\right)$$

$$P_{(mW)} = 10^{P_{(dBm)}/10}$$

$$P_{(mW)} = 10^{5.76/10} = 3.77 \text{ mW}$$

$$P_{(W)} = \frac{V_{(rms)}^{2}}{R_L} \rightarrow V_{(rms)} = \sqrt{P_{(W)} \times R_L}$$

$$V_{(rms)} = \sqrt{3.77 \times 10^{-3}\text{W} \times 600\Omega} = 1.50 \text{ V}_{rms}$$

$$V_{(pp)} = V_{(rms)}\, 2\sqrt{2}$$

$$V_{(pp)} = 4.25 \text{ Vpp}$$

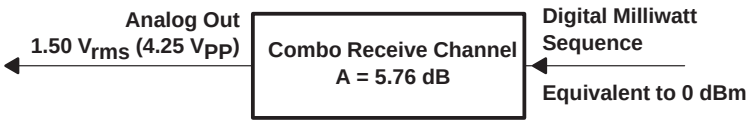


Figure 23. Combo Reference-Level Receive Gain, μ-Law

The transmit channel zero transmission level is specified in a similar manner. For a μ-law configuration with the signal referenced to a 600-Ω load, a 2.76 dBm signal is required to generate a digital milliwatt sequence (see Figure 24). Using the method shown previously, calculations show that 2.76 dBm into a 600-Ω load is equal to 1.06 Vrms, or 3.01 Vpp.

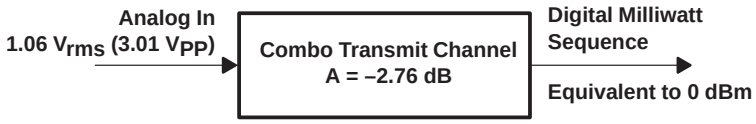


Figure 24. Combo Reference-Level Transmit Gain, μ-Law

This analysis can also be performed using the parameters for 900-Ω load references and A-law configurations. Note that for any load or configuration, when a TCMxxCxx device is configured for digital loopback (PCMOUT/DX externally connected to PCMIN/DR), the output signal from the receive path is 3 dB higher than the transmit input signal level.

2.5.2.2 Analog Transmit Input That Produces Maximum Digital Output

As discussed earlier, the CCITT defines the maximum analog input level and output level as 3.17 dBm0 for μ-law and 3.14 dBm0 for A-law. This means that the maximum signal that can be transmitted through a transmit or receive path, relative to the zero transmission level points, is 3.17 dB or 3.14 dB.

For an example, consider again the TCM29C13 in μ-law configuration referencing power levels to a 600-Ω load. The zero transmission level for the transmit path is 2.76 dBm. To determine the maximum peak-to-peak voltage that can be applied to the transmit inputs, the 3.17 dB gain must first be applied:

2.76 dBm + 3.17 dB = 5.93 dBm

Next, this reference must be converted to a peak-to-peak voltage level, using the method described in the previous section. The value is calculated to be 1.53 Vrms, or 4.34 Vpp, as in Figure 25.

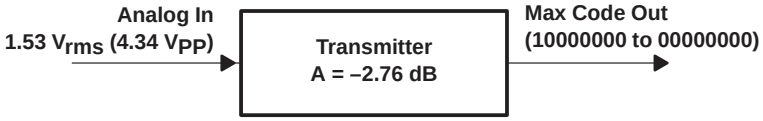


Figure 25. Maximum Digital Output, TCM29C13, μ-Law

2.5.2.3 Maximum Analog Receiver Output

As mentioned above, the maximum signal transmission allowed by the CCITT G.711 specification is 3.17 dBm0, or 3.17 dB above the zero-transmission-level point. For the receive side, the zero-transmission-level point for a μ-law transmission, referenced to a 600-Ω load, is 5.76 dBm. Using the same techniques as above, the maximum peak-to-peak signal from the analog receiver outputs is found to be 2.17 Vrms, or 6.14 Vpp, as shown in Figure 26.

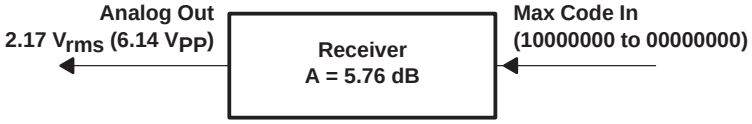


Figure 26. Maximum Analog Output, TCM29C13, μ–Law

2.5.3 TP30xx

Amplitude and gain considerations for the TI TP30xx line of combo devices are discussed in the following paragraphs.

2.5.3.1 Zero Transmission Levels for the TP30xx Family

In the *operating characteristics* section of the TP30xx data sheets, the double-dagger note under the *filter gains and tracking errors* table states that the 0 dBm0 level is equal to 4 dBm referenced to 600 Ω. Using the methods described in the TCM29Cxx and TCM37Cxx section, this can be shown to equal 1.23 Vrms, or 3.47 Vpp. In other words, a 3.47 Vpp input signal generates a digital milliwatt sequence at the transmit digital output. This applies to both μ-law and A-law configurations.

The TP30xx combo devices impose –4 dB of gain on the transmit path and 4 dB of gain on the receive path. Therefore, application of a digital milliwatt sequence on the receive input (equivalent to an analog 0 dBm signal) causes a 4 dBm signal to appear at the receive analog output.

2.5.3.2 Analog Transmit Input That Produces Maximum Digital Output

The CCITT specifies the maximum signal transmission allowed by the CCITT G.711 specification for μ-law transmissions as 3.17 dBm0 and 3.14 dBm0 for A-law transmissions. In other words, μ-law analog input signals are not allowed to exceed 3.17 dB above the zero-transmission-level point for the transmit channel. Since the transmit zero-transmission-level point is specified as 4 dBm, the maximum transmit input level for μ-law is:

4 dBm + 3.17 dB = 7.17 dBm

Using the methods described in section 2.5.1.1, *Zero Transmission Level* for the TCM29Cxx and TCM37Cxx Lines, it is calculated that 7.17 dBm into a 600-Ω load is 1.768 Vrms, or 5.002 Vpp. For an A-law transmission (limited to 3.14 dBm0), the maximum input voltage is 1.762 Vrms, or 4.984 Vpp.

2.5.3.3 Maximum Analog Receiver Output

Since the gain of the receive path is inverse to the gain of the transmit path (net unity gain), the maximum output voltage should be the same as the maximum input voltage.

2.6 Power-Down and Standby Operations

To minimize power consumption, power-down and standby modes are provided. All TI combo devices offer a power-down mode, which reduces power consumption to 3 mW for the TCM29Cxx, TCM37Cxx, and TP30xx. For the TCM38C17, which is based on the new advanced LinEPIC process, power consumption is only 1 mW per channel. In addition to power-down modes, the TCM29Cxx and TCM37Cxx offer standby modes that enable the user to selectively put the transmit and/or receive channels on standby, which also reduces power consumption. The details of power-down and standby operation can be found in the data sheets for these devices.

3 APPLICATION INFORMATION

The following sections contain information on preventing latch-up, noise and power supply design considerations, and describes example circuits.

3.1 Latch-Up Prevention

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and continues to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

TI continues to improve the latch-up protection of its devices. However, even though TI combos are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

3.1.1 Implementing Schottky Diode Protection

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent) between each power supply and GND (see Figure 27). If it is possible that a combo-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

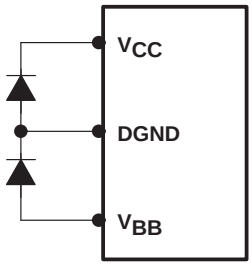


Figure 27. Latch-Up Protection Diode Connection

3.1.2 Device Power-Up Sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence be used.

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power-down condition in the device.
6. Connect the master clock.
7. Release the power-down condition.
8. Apply FSX and/or FXR synchronization pulses.
9. Apply signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

While this power-up sequence is recommended for all systems, systems incorporating the external Schottky diode protection should be safe from most latch-up situations.

3.2 Design Considerations

The following sections discuss noise, grounding, and power supply design considerations.

3.2.1 Noise

Noise in combo-based systems can be reduced by following some basic guidelines. In addition to this section, see sections 3.2.2, *Grounding/Decoupling*, and 3.2.3, *Power Supply*, since these aspects of system design also affect the presence of noise.

As with most linear semiconductor devices, combos can be susceptible to noise from the power supply rail. Any noise on the power supply couples directly into the switched-capacitor filters and can be detected on the output. Optimum design technique practices should be followed on the power supply to minimize noise. See section 3.2.3, *Power Supply*, for additional power supply guidelines.

The best noise performance (S/N ratio) can be expected when the maximum analog input is used. See section 2.5, *Analog Signal Levels and Gain Analysis*, for details on determining the correct peak-to-peak voltages. The value presented to the transmit filter can be measured at the GSX terminal, which is the output of the transmit input amplifier. The gain of this amplifier can be adjusted to achieve minimum peak-to-peak voltage.

3.2.2 Grounding/Decoupling

A separate ground plane on the printed circuit board should be used for digital and analog ground. They should cover as much unused area as possible. A third ground path should be implemented for a transient suppressor, if present. A separate earth ground path will prevent damage due to transients as a result of lightning strikes or contact between local loop lines and power lines.

The circuit board should be arranged in such a way that the analog and digital signals are as isolated from each other as possible. Otherwise, coupling between the traces could bring high-frequency transients in the digital signals into the analog audio signal.

Bypass each of the combo power supply terminals with a high-quality 0.1-μF ceramic capacitor (such as a CK05). Do this by connecting the capacitor between ground and V_{CC} and between ground and V_{BB}. Connections should be made as close as physically possible to the combo device terminals. Ceramic capacitors have a low ESR (equivalent series resistance), or high Q, and are able to react to fast changes in voltage and are used to suppress high-frequency transients. These high-frequency transients result from instantaneous high current consumption during digital device switching. Since all power supplies have an internal impedance that prevents infinite current sourcing, power supply voltage ripple (noise) results from digital device switching. Capacitive loading on the power supply rail regulates the voltage of the supply.

3.2.3 Power Supply

A voltage regulator should always be used, even when using battery power. In particular, batteries have a high internal impedance that allows the dc voltage to vary in response to instantaneous current consumption during digital switching. The resultant change in voltage manifests itself as noise on the power supply rail.

Use a 10-μF capacitor across the power supply rails on the PCB. This serves the same purpose as the ceramic capacitor, except that it responds well to lower-frequency transients.

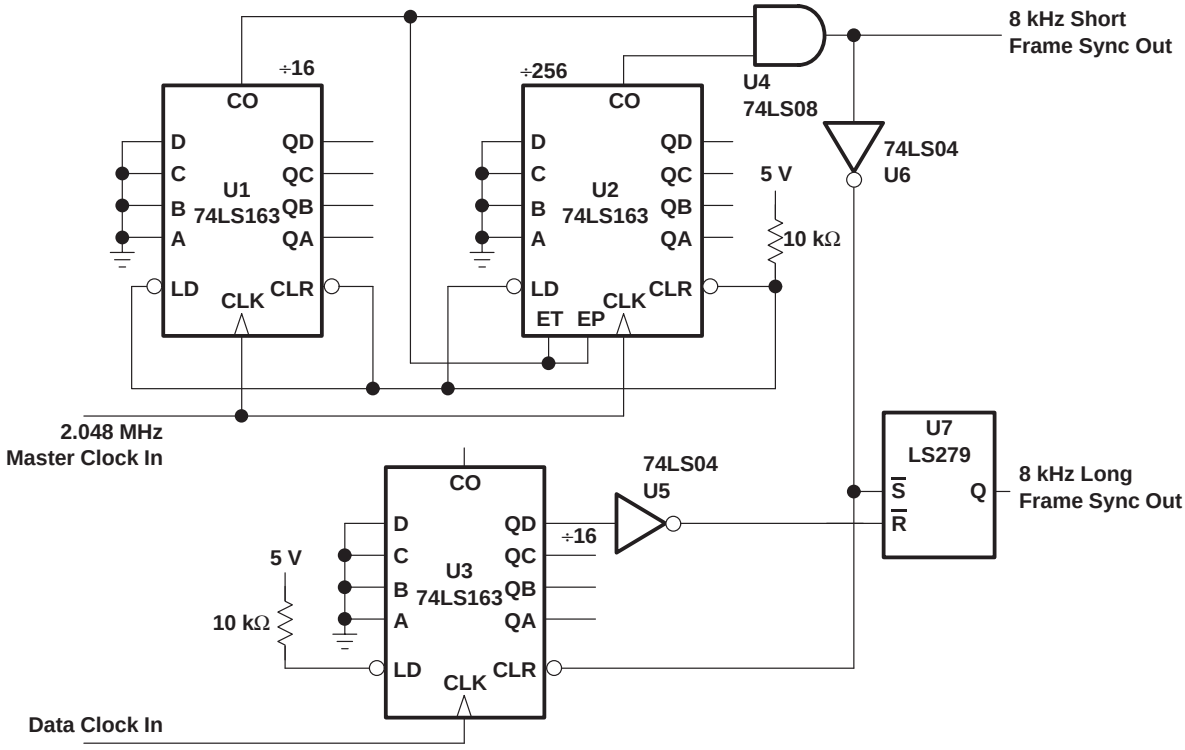
All power supply traces should be as close to the ground plane as physically possible. The close proximity to the ground plane adds parallel capacitance.

3.3 Circuit Examples

The following circuit examples illustrate a variety of TI combo applications.

3.3.1 Frame Sync Generator

Most combo/line-card applications use clocks/frame syncs generated from a DSP (digital signal processor) or ASIC (application-specific integrated circuit) clock divider. However, other applications may require generating these clocks from discrete components. The circuit in Figure 28 correctly generates both short and long frame syncs for a combo with a master clock of 2.048 MHz. Short frame syncs can be used with TCMxxCxx combos operating in fixed-data-rate mode, and long frame syncs can be used with TCMxxCxx combos operating in variable-data-rate mode. TP30xx combos can use either frame sync in any mode (see section 2.3.3, *Intel vs. National Timing*).



NOTE A: 74LS163 Counters are fully synchronous.

Figure 28. Combo Short and Long Frame Sync Circuit with 2.048-MHz Master Clock

The top part of the circuit generates a short frame sync pulse. The U1 and U2 74LS163 4-bit counters are clocked synchronously by Master Clock In. U2 is cascaded with U1 so that together they divide the master clock by 256, and provide an output pulse one master clock period long. This is the length required by TP30xx combo devices using short frame syncs and TCMxxCxx combo devices operating in fixed-data-rate mode. The AND gate (U4) is necessary to eliminate a glitch produced by the CO (carry out) terminal of 74LS163 counters. This glitch occurs immediately before the carry-out pulse, and since the combo frame sync input is edge triggered, the combo would identify both the true carry-out pulse and the glitch as frame syncs. By ANDing the carry-outs of the U1 and U2 timers as shown, only the true carry-out pulse is seen at the short frame sync output.

The lower part of the circuit is used to generate a long frame sync pulse. The RS (set/reset) latch U7 is set by the short frame sync output after the first 256 master clock pulses. Counter U3 is clocked by the data bit clock and connected to the U7 RS latch so that the latch resets after eight data bit clocks have been counted. The Q output of the RS latch, then, is high for the duration of the eight data bits required for a long frame sync.

3.3.2 Telephone Interface Example

Figure 29 shows a typical combo application circuit that uses a DSP and transformer hybrid functions. It is used to interface a DSP-based system to a standard analog POTS (plain old telephone service) line, indicated by TIP and RING. The circuit uses TI TCM29C16 combos, but the circuit could be built with any TI combo by making the necessary adaptations for gain setting and other minor differences.

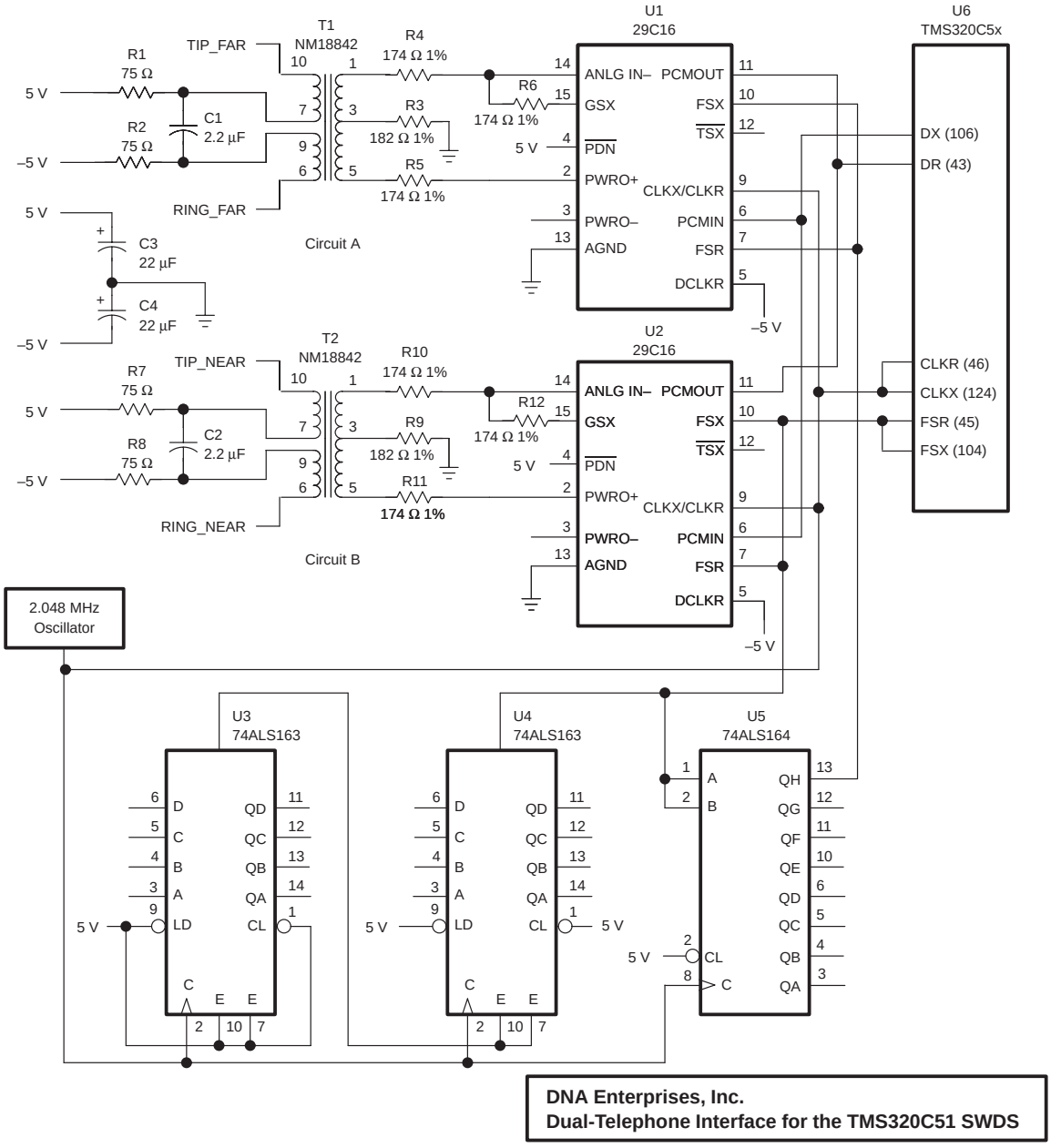


Figure 29. Telephone Interface Circuit Using DSP and Hybrid Functions

By connecting DCLKR to –5 V, the device is configured for fixed-data-rate operation. The analog transmit input amplifiers are configured for unity gain. The 2.048 MHz clock is fed directly to the master clock terminal of each combo device. It is also fed to a logic chain that generates frame syncs, similar to the one discussed in section 3.3.1, *Frame Sync Generator.* An 8-kHz frame sync signal is generated and is used for the combo in Circuit B (U2). This frame sync clock is also fed to an 8-bit shift register (U5), which delays each pulse by eight master clock periods. This creates a frame sync clock for the combo in Circuit A (U1). Therefore, the combos transmit their data in succession; U2 goes first, and U1 follows immediately. The first frame sync pulse is also fed to the DSP (U6) so that data transfer is synchronized.

Transformers T1 and T2 perform the hybrid function, interfacing 2-wire TIP and RING signals to the 4-wire combos. Network balancing is provided by R1, R2, and C1 for Circuit A and R7, R8, and C2 for Circuit B.

3.3.3 TCM29Cxx: Variable-Data-Rate Mode Using Common Master and Data Clocks

In some applications it is desirable to operate a TCM29Cxx combo device in the variable-data-rate mode while using the same clock source for both the master clock and data clock. This provides the designer with the advantages of the variable-data-rate mode, such as repeated data while frame sync is high, while still running at the maximum data rate, as occurs in fixed-data-rate mode.

If the device is to be operated this way, the DCLKX and CLKX terminals cannot be directly connected externally. A buffer must be used for the DCLKX connection because the TCM29Cxx always powers up in the fixed-data-rate mode, and for the first several clock cycles, the DCLKX terminal is actually an output ($\overline{\text{TSX}}$ — see data sheet). The $\overline{\text{TSX}}$ output is an open-drain transmit time strobe and if connected directly to MCLKX, it will pull that terminal low, which will corrupt the MCLKX input. Only after the first several master clock cycles does the device begin to operate in variable-data-rate mode (as selected by the DCLKR), and the DCLKX terminal becomes an input. Therefore, it is suggested that a buffering stage be inserted between the MCLKX/DCLKX common point and the DCLKX terminal, as shown in Figure 30.

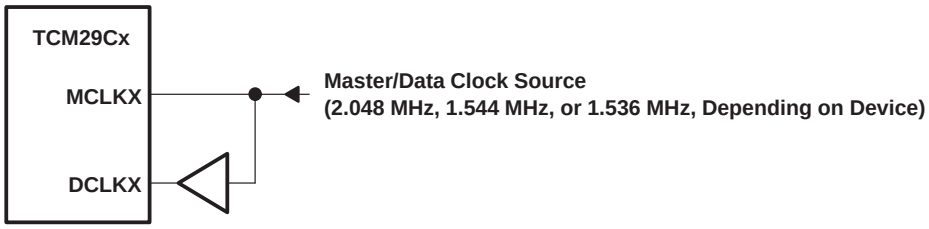


Figure 30. TCM29Cxx Variable-Data-Rate Mode with Common MCLKX and DCLKX

4 TROUBLESHOOTING the TCMxxCxx and the TP30xx Combos

Table 4 lists possible problems with the TCMxxCxx and TP30xx combos along with possible solutions for each one.

Table 4. TCMxxCxx and TP30xx Troubleshooting

Symptom	Possible Cause	TCMxxCxx Solution	TP30xx Solution
No signals on digital output terminal (PCMOUT/DX)	• Device is powered down	• Ensure that $\overline{\text{PDN}}$ has a logic low applied to it. • If a frame sync is missed, the path (TX or RX) of the missing frame sync goes into standby mode.	• Ensure that MCLKX/PDN has either a clock or logic low applied to it. • If a frame sync is missed, the device goes into power-down mode. • The master clock signals must be applied for power-down circuitry to work properly.
Frequency response does not appear to be correct	• Master clock frequency is incorrect	• CLKX/CLKR/MCLK are recommended to match the value selected by CLKSEL (1.536 MHz, 1.544 MHz, or 2.048 MHz). See section 2.3.1, *Effect on Pass-Band Parameters*, to understand the effects of incorrect master clocks.	• MCLKX/MCLKR are recommended to match the value selected by CLKSEL (1.536 MHz, 1.544 MHz, or 2.048 MHz). See section 2.3.1, *Effect on Pass-Band Parameters*, to understand the effects of incorrect master clocks.
	• Frame sync frequency is incorrect	• See section 2.3.2, *The Relationship Between Master Clocks, Data Bit Clocks, and Frame Syncs.*	• See section 2.3.2, *The Relationship Between Master Clocks, Data Bit Clocks, and Frame Syncs.*
Digital output signal (at PCMOUT/DX terminal) is distorted	• Overdriving input to transmit filter section	• See section 2.5.3.2, *Analog Transmit Input That Produces Maximum Digital Output.*	• See section 2.5.3.2, *Analog Transmit Input That Produces Maximum Digital Output.*
	• Transmit input offset voltage is out of specification	• DC offset voltage at transmit input should not exceed ±25 mV. AC coupling may be needed to block the offset voltage.	• DC offset voltage at transmit input should not exceed ±25 mV. AC coupling may be needed to block the offset voltage.
	• GSX output is overloaded	• Feedback resistor at GSX should be at least 10 kΩ.	• Feedback resistor at GSX should be at least 10 kΩ.
	• Timing problem	• Analyze device timing and make sure that the clocks in use meet data sheet specifications. • Perform a digital loopback by routing PCMOUT data to PCMIN. Compare the input analog transmit signal to the output analog receiver signal. The output signal should be 3 dB higher than the input. If it is, the device is working properly. However, the timing may be incompatible with the rest of the system. • Check device logic inputs. Verify that the signal does not exceed specified limits due to noise, etc. Low signals must be less than 0.6 V, high must be greater than 2.2 V.	• Analyze device timing and make sure that the clocks in use meet data sheet specifications. • Perform a digital loopback by routing DX data to DR. Compare the input analog transmit signal to the output analog receiver signal. The output signal should be approximately equivalent to the input. If it is, the device is working properly. However, the timing may be incompatible with the rest of the system. • Check device logic inputs. Verify that the signal does not exceed specified limits due to noise, etc. Low signals must be –0.3 V to 0.6 V, high must be 2.2 V to V_{CC} + 0.3 V. • If possible, avoid asynchronous clocks.

Table 4. TCMxxCxx and TP30xx Troubleshooting (Continued)

Symptom	Possible Cause	TCMxxCxx Solution	TP30xx Solution
Analog receive output is distorted (at PWRO/VFRO terminals)	• Overdriving receive output amplifier	• Load must be at least 600 Ω.	• Load must be at least 600 Ω.
	• Timing problem	• Analyze device timing and make sure that the clocks in use meet data sheet specifications. • Perform a digital loopback by routing PCMOUT data to PCMIN. Compare the input analog transmit signal to the output analog receiver signal. The output signal should be 3 dB higher than the input. If it is, the device is working properly. However, the timing may be incompatible with the rest of the system. • Check device logic inputs. Verify that signal does not exceed specified limits due to noise, etc. Low signals must be less than 0.6 V, high must be greater than 2.2 V.	• Analyze device timing and make sure that the clocks in use meet data sheet specifications. • Perform a digital loopback by routing DX data to DR. Compare the input analog transmit signal to the output analog receiver signal. The output signal should be approximately equivalent to the input. If it is, the device is working properly. However, the timing may be incompatible with the rest of the system. • Check device logic inputs. Verify that signal does not exceed specified limits due to noise, etc. Low signals must be –0.3 V to 0.6 V, high must be 2.2 V to V_{CC} + 0.3 V. • If possible, avoid asynchronous clocks.
Analog receiver output signal contains high-frequency noise (low-volume whistling, for example)	• Clocks or frame syncs contain jitter	• If the amount of jitter is large enough and if its frequency is in the voice-band range, it may be detectable in the transmission signal. An analog PLL can be used to eliminate jitter.	• If the amount of jitter is large enough and if its frequency is in the voice-band range, it may be detectable in the transmission signal. An analog PLL can be used to eliminate jitter.
	• Inadequate power supply decoupling or grounding	• See sections 3.2.2, *Grounding/Decoupling,* and 3.2.3, *Power Supply.*	• See sections 3.2.2, *Grounding/Decoupling,* and 3.2.3, *Power Supply.*
Crosstalk attenuation is out of specification	• Inadequate power supply decoupling	• See sections 3.2.2, *Grounding/Decoupling,* and 3.2.3, *Power Supply.*	• See sections 3.2.2, *Grounding/Decoupling,* and 3.2.3, *Power Supply.*
Combo gets hot, draws unusually high current, or ceases to operate	• Latch-up	• See section 3.1, *Latch-Up Prevention.*	• See section 3.1, *Latch-Up Prevention.*

Table 4. TCMxxCxx and TP30xx Troubleshooting (Continued)

Symptom	Possible Cause	TCMxxCxx Solution	TP30xx Solution
Excessive idle-channel noise or signal-to-distortion ratio is out of specification	• Inadequate power supply decoupling or grounding	• See sections 3.2.2, *Ground/Decoupling,* and 3.2.3, *Power Supply.*	• See sections 3.2.2, *Ground/Decoupling,* and 3.2.3, *Power Supply.*
	• Use of enhanced noise-reduced device in an application for which it is not well suited	• TCMxxCxx devices with part numbers ending in “A” (as in TCM29C13A) use an enhanced noise-reduction algorithm. Although this algorithm provides improved noise performance in most cases, some applications perform better without it. See section 2.1.5, *Enhanced Noise-Reduction Algorithm*, for details.	• Some TP30xx devices use an enhanced noise reduction algorithm. Although this algorithm provides improved noise performance in most cases, some applications perform better without it. See section 1.4, *Device Nomenclature*, and Table 1 for a list of devices using the enhanced noise-reduction algorithm, and section 2.1.5, *Enhanced Noise-Reduction Algorithm* for details.
	• Received PCM data contains eighth-bit signaling (all combos except TCM29C14 and derivatives)	• Eighth-bit signaling replaces the last bit of the data frames with a signaling bit. Combos other than the TCM29C14 and derivatives (which are capable of extracting these bits) interpret them as data, slightly affecting noise and distortion performance.	• Eighth-bit signaling replaces the last bit of the data frames with a signaling bit. Combos other than the TCM29C14 and derivatives (which are capable of extracting these bits) interpret them as data, slightly affecting noise and distortion performance.
	• Noisy SLIC†	• Noise introduced in the SLIC is passed along to the combo. If high gain is applied to this signal by the combo, noise is amplified as well.	• Noise introduced in the SLIC is passed along to the combo. If high gain is applied to this signal by the combo, noise is amplified as well.
	• Timing problem	• Analyze device timing and make sure that the clocks in use meet data sheet specifications. • Perform a digital loopback by routing PCMOUT data to PCMIN. Compare the input analog transmit signal to the output analog receiver signal. The output signal should be 3 dB higher than the input. If it is, the device is working properly. However, the timing may be incompatible with the rest of the system. • Check device logic inputs. Verify that the signal does not exceed specified limits due to noise, etc. Low signals must be less than 0.6 V, high must be greater than 2.2 V.	• Analyze device timing and make sure that the clocks in use meet data sheet specifications. • Perform a digital loopback by routing DX data to DR. Compare the input analog transmit signal to the output analog receiver signal. The output signal should be approximately equivalent to the input. If it is, the device is working properly. However, the timing may be incompatible with the rest of the system. • Check device logic inputs. Verify that the signal does not exceed specified limits due to noise, etc. Low signals must be –0.3 V to 0.6 V, high must be 2.2 V to V_{CC}+0.3 V. • If possible, avoid asynchronous clocks.

† SLIC = subscriber line interface circuit

Table 4. TCMxxCxx and TP30xx Troubleshooting (Continued)

Symptom	Possible Cause	TCMxxCxx Solution	TP30xx Solution
Others	• Damaged device	• Use a device known to be functional.	• Use a device known to be functional.
	• Wrong power supply voltages	• V_{BB} and V_{CC} must be –5 V and +5 V, respectively, with 5% tolerance.	• V_{BB} and V_{CC} must be –5 V and +5 V, respectively, with 5% tolerance.
	• Device is improperly wired	• Double–check all connections to make sure they match device and application specifications. Check all input signals and power supplies with an oscilloscope. • Perform these checks directly on the terminals, as the problem could lie in the physical wiring. If signal inputs to the terminals are incorrect, trace the problem to the source of the signals.	• Double check all connections to make sure they match device and application specifications. Check all input signals and power supplies with an oscilloscope. • Perform these checks directly on the terminals, as the problem could lie in the physical wiring. If signal inputs to the terminals are incorrect, trace the problem to the source of the signals.

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