Application Note

Understanding Transient Drive Strength vs. DC Drive Strength in CMOS Output Buffers

Michael Ikwuyum, Sahil Garg, and Debayan Chakraborty

ABSTRACT

Two important parameters that characterize the performance of CMOS output buffers are Transient drive strength and Static drive strength. Understanding the differences between these two parameters are essential for selecting the correct device for system designers.

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1 Transient Drive Strength

Transient drive strength refers to the ability of the CMOS output buffer to deliver high current during short-duration transient events, such as switching transitions. It is primarily influenced by the output stage's ability to charge and discharge the load capacitance associated with the output node. This indicates the ability of the output to supply or sink current by quickly charging or discharging the output capacitance, while switching from LOW to HIGH or HIGH to LOW.

Transient drive strength is critical for ensuring fast rise and fall times of output signals, which directly impact the system's speed and signal integrity. A faster transition indicates a higher transient drive strength. In high-speed applications, such as clock distribution and data transmission, a strong transient drive capability is essential to minimize signal propagation delays and reduce the risk of signal distortion.

Design considerations for enhancing transient drive strength includes optimizing the output stage's sizing – width of the transistors used in the pull-up and pull-down networks and minimizing parasitic capacitance in the output network to increase response at higher frequencies.

However, careful system considerations are recommended as some systems may not be able to handle very strong outputs due to sensitivities to transmission line effects. Some symptoms can include overshoots, undershoots, reflections (commonly known as ringing). Simply using series dampening resistors on the outputs may help adjust accordingly, per system requirements.

Rise or Fall times are good indicators of a device’s transient drive strength.

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2 Static Drive Strength

Static drive strength refers to the ability of the CMOS output buffer to maintain a stable output voltage level under static steady-state conditions, with higher current load. It determines the maximum load current that the output buffer can reliably drive without significant voltage droop or distortion and is generally measured using IOH and IOL of the buffer.

This is the current needed by the output to source or sink while maintaining the voltage at the specified high-level (logic ‘1’) or low-level (logic ‘0’). Transient drive is significant for how fast the output gets to a logic 1 (rise time) or logic 0 (fall time) while static drive maintains or keeps the output steady for a specified high-level (logic ‘1’) or low-level (logic ‘0’) voltage respectively.

This static current strength is crucial for ensuring the stability and reliability of digital systems, especially in applications where the output buffer drives resistive loads, LED loads, and so on.

To enhance static drive strength, designers typically focus on optimizing the biasing conditions of the output transistors and minimizing output impedance across various supply voltages and process parameters.

IOH and IOL are good indicators of a device’s DC drive strength.

3 Tradeoff Analysis

While transient current drive strength emphasizes the ability to handle rapid changes in output voltage, static current drive strength focuses on maintaining voltage levels under steady-state conditions. Both parameters are interrelated but address different aspects of output buffer performance and thereby need different design approaches.

It is essential for application or system engineers to balance transient and static current drive strength requirements based on the specific application's speed, load conditions, and power constraints. In some cases, optimizing for one parameter may lead to compromises in the other.

For applications like driving an LED, motor, or driving a I2C device where there is a demand for high static current, system designers should consider static current drive strength. Whereas, rise or fall times act as a measure of transient drive strength for system designers when the load is purely capacitive and there is a low static current requirement. Therefore, careful consideration and trade-off analysis are necessary during the design phase to meet the desired performance specifications of rise or fall times and static current drive requirements.

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4 Why High DC Strength Does Not Always Mean High Transient Strength

To make sure to have a high static current strength, large MOSFETs are deployed with wider routing and connections to avoid reliability concerns like electro-migration. These large size FETs poses two challenges to designers:

- Wider routing produce large parasitic capacitance which slows down transient response.
- Additionally, large FETs with high DC strength can lead to higher amplitude of ringing at the output during transients, thus posing reliability and signal integrity concerns.

To control ringing, current limiter circuits are added in CMOS buffers to limit the transient current and thus reduce ringing. Hence, the buffer with high static current strength may have a low transient strength.

Figure 4-1 and Figure 4-2 compares SN74AVCxT245 (faster transient drive - rise or fall times, lower static drive - specified for up to 12mA) and SN74LXCxT245 (slower transient drive - rise or fall times, higher static drive - specified for up to 32mA).

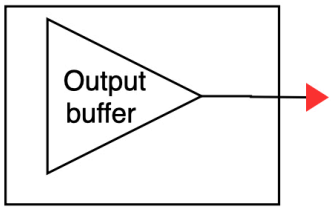

Figure 4-1. High Transient Drive Strength Buffer (AVC)

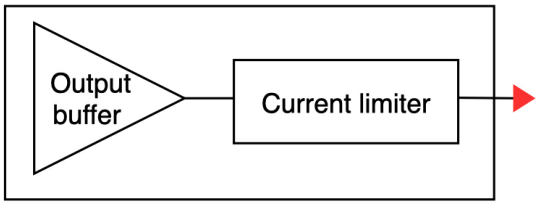

Figure 4-2. High DC Drive Strength Buffer With Transient Current Limiter Circuit (LXC)

Figure 4-1, compares AVC and LXC transient drive strengths. AVC switches faster than LXC, indicating a higher transient drive strength.

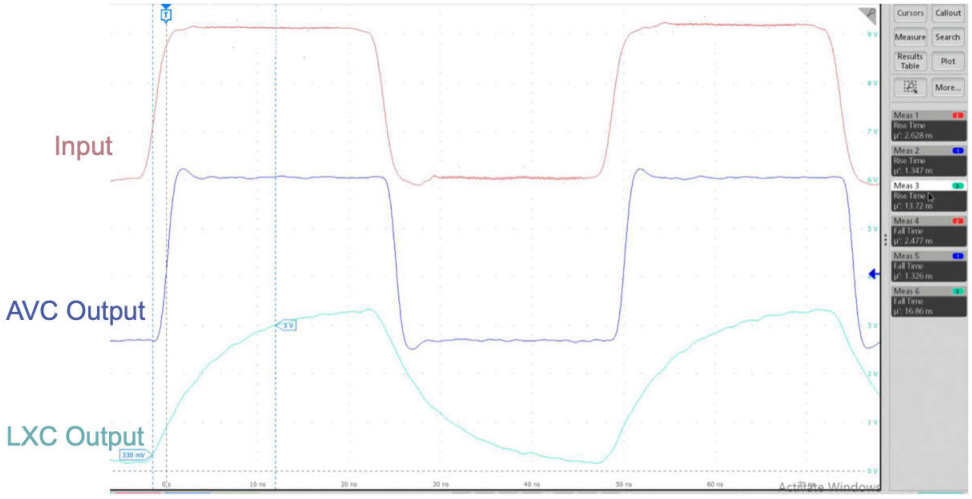

Figure 4-3. Rise or Fall Times of SN74AVCxT245 and SN74LXCxT245

Note

CMOS level shifter output buffer examples showing transient transitions of AVC and LXC level shifter buffers with the same conditions.

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Figure 4-4, compares AVC and LXC transient currents required for their switching transitions. Although specified for a lower static current, the faster AVC device requires higher transient currents to switch between the fast HIGH or LOW transitions.

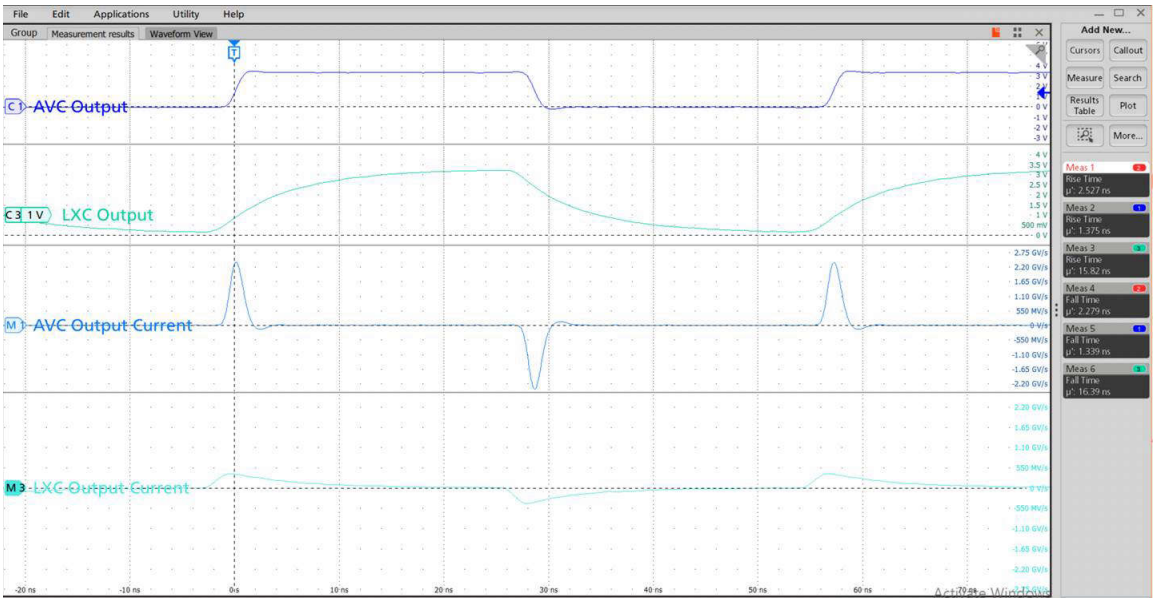

Figure 4-4. Transient Switching Current for SN74AVCxT245 and SN74LXCxT245

Note

CMOS level shifter output buffer examples showing output switching currents for AVC and LXC level shifter buffers with the same conditions.

5 Summary

Static current drive strength focuses on providing a strong and steady signal during normal operating conditions.

Transient current drive strength emphasizes the ability to quickly and effectively drive the load capacitance during signal transitions.

Both static and transient current drive strengths are essential for reliable and high-performance digital system design. However, they both address different aspects of signal integrity and performance.

6 References

- Texas Instruments, *Voltage Translators and Level Shifters* product folders.

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