UCC28730-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Application Report

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This document contains information for UCC28730-Q1 (SOIC (7) package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

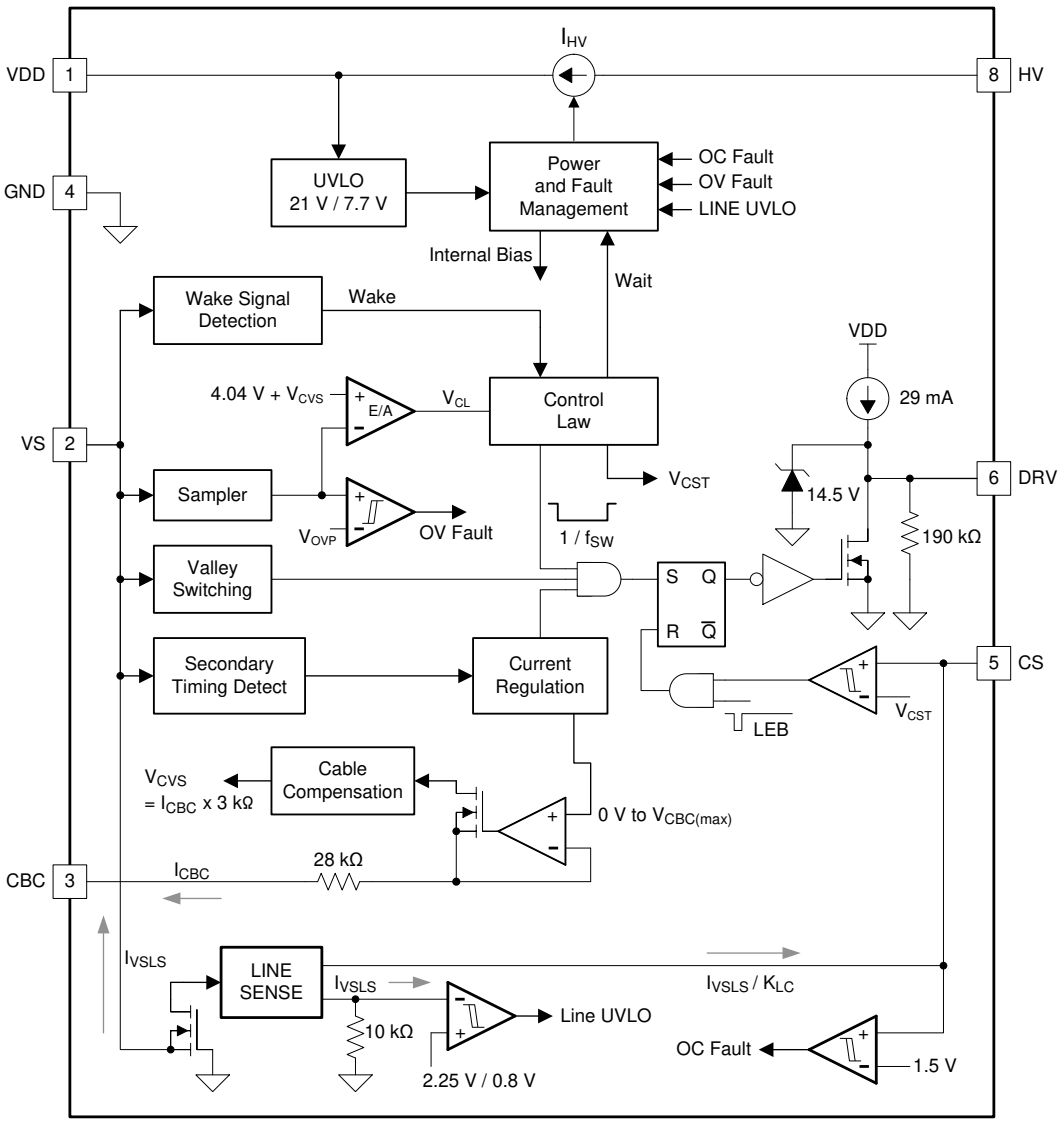

Figure 1-1. Functional Block Diagram

UCC28730-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

Chapter 2

Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for UCC28730-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (50 mW, 100 mW, 150 mW)	10, 11, 13
Die FIT Rate (50 mW, 100 mW, 150 mW)	3, 4, 5
Package FIT Rate (50 mW, 100 mW, 150 mW)	7, 7 , 8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW, 100 mW, and 150 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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Chapter 3

Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC28730-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
DRV stuck low	34
DRV stuck high	20
Incorrect Vout regulation	17
No effect	29

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Chapter 4

Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC28730-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the UCC28730-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC28730-Q1 data sheet.

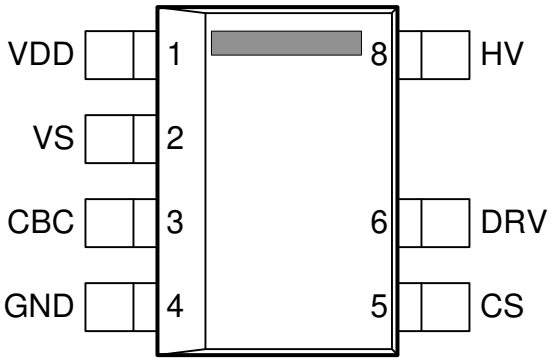

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The UCC28730-Q1 is connected according to UCC28730-Q1 datasheet Figure 8-1 Simplified Application With Ground-Referenced Diode
- The VDD is considered as supply pin

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Device is not function system will not startup.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VS	2	IC remains in input under voltage protection mode. The output of the Flyback converter remains at zero.	B
CBC	3	Cable compensation will be set at its highest value.	C
GND	4	No effect.	D
CS	5	When CS pin is shorted before the IC start-up, CS pin short protection. The output of the Flyback converter remains at zero.	B
		When CS pin is shorted after the IC already in operation, DRV remains high. Potential power stage damage and it might cause IC damange.	A
DRV	6	DRV remains low. The output of the Flyback converter remains at zero.	B
N/A	7		
HV	8	The VDD capacitor cannot be trickle charged and the converter will never startup.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No positive supply applied to device, device is not functional.	B
VS	2	IC remains in input under voltage protection mode. The output of the Flyback converter remains at zero.	B
CBC	3	Cable compensation is reduced to It's minimal value.	C
GND	4	Device damage	A
CS	5	When CS pin is shorted before the IC start-up, CS pin short protection. The output of the Flyback converter remains at zero.	B
		When CS pin is shorted after the IC already in operation, DRV remais high. Potential power stage damage and it might cause IC damange.	A
DRV	6	The output of the Flyback converter remains at zero.	B
N/A	7		
HV	8	The VDD capacitor cannot be trickle charged. Output of the converter remains at zero volts.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	VS	VS max voltage rating exceeded, device damaged, possible Flyback switch damage	A
VS	2	CBC	Cable compensation will not be stable, output voltage will not regulate correctly	C
CBC	3	GND	Cable compensation will be set at its highest value.	C
GND	4	N/A		
CS	5	DRV	CS max voltage rating will be exceeded, device damage, possible Flyback switch damage	A
DRV	6	N/A		
N/A	7	N/A		
HV	8	N/A		

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No Effect.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VS	2	DRV remains low. Possible IC damage.	A
CBC	3	DRV remains low. Possible IC damage.	A
GND	4	No positive supply applied to device. Device is non-functional.	B
CS	5	DRV remains low. Possible IC damage.	A
DRV	6	DRV remains high. Possible IC damage and Flyback switch damage.	A
N/A	7		
HV	8	The max rating of VDD will be exceeded, possible device damage and Flyback switch damage.	A

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