UCC28056X Selection Guide

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The UCC28056A, UCC28056B, and UCC28056C are PFC controllers that work in a dual-mode configuration where it operates in transition mode at heavier load conditions and transitions to discontinuous conduction mode at lighter load conditions. When used with the LLC controller, these 6-pin devices, thanks to its high efficiency at light-load conditions, eliminate the need for an auxiliary flyback converter while achieving less than 80 mW no-load input power at 230 Vac. This application note addresses the new variants of the UCC28056 device family and showcases the changes implemented on each variant and highlights the advantages that they serve.

Feature Differentiation

Table 1 showcases the differences among the various versions of the UCC28056 devices.

Table 1. Feature Variation of the UCC28056X Family

FEATURE	UCC28056	UCC28056A	UCC28056B	UCC28056C
ZCD Improvement	No	Yes	Yes	Yes
Burst Mode Threshold	10%	15%	15%	10%
OVP1 Threshold	10%	8%	10%	10%
OVP2 Threshold	Yes	No	Yes	Yes

ZCD Improvement

Integration of the zero current detection (ZCD) and the current sense (CS) pins helps reduce the pin count and produce a smaller package. This makes this pin sensitive to the layout of the PCB. The noise can be injected in the ZCD/CS pin either from the downstream DC/DC converter (flyback/LLC) or the parasitic capacitance of the layout. A traditional approach is to introduce an auxiliary winding and sense the ZCD event by monitoring this smaller current and moving the traces away from the high switching nodes of the primary FET. The disadvantage of using this approach is increased cost and component count since a custom PFC inductor and external components are required.

The UCC28056A, UCC28056B, and UCC28056C address this issue and make the controller more robust and immune to layout, thus more tolerant and less sensitive to downstream noise.

Burst Mode Threshold

The UCC28056 transitions to burst mode operation when the load is below 10% of its maximum output power. As the output load decreases, the controller starts to operate in discontinuous conduction mode and its switching frequency is decreased up to 18 kHz at high line conditions.

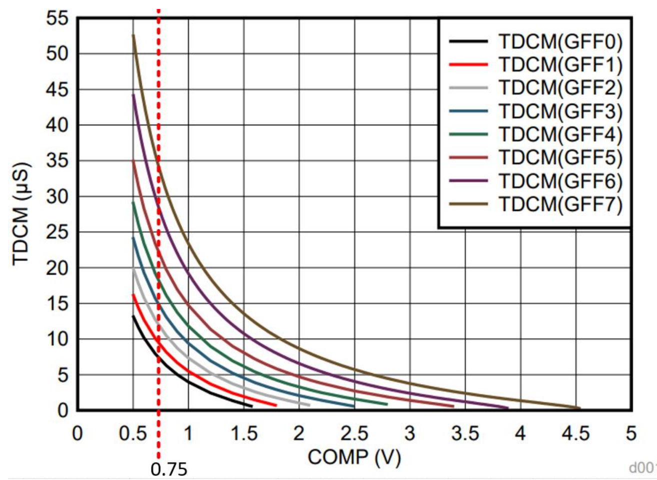

Figure 1. Modified Minimum Burst Mode Fall Threshold

The UCC28056A and UCC28056B implement a higher burst threshold which prevents the frequency from dropping into the audible noise band. The UCC28056A and UCC28056B enter the burst mode operation at 15% of the maximum output load which maintains the minimum frequency of the controller at 22 kHz and prevents any intrusion into the audible range. The red line in Figure 1 indicates the increased burst mode threshold.

Table 2. Burst Mode Threshold Variation

FEATURE	UCC28056	UCC28056A	UCC28056B	UCC28056C
Burst Mode Threshold	10%	15%	15%	10%
$V_{BSTFall}$	0.5 V	0.75 V	0.75 V	0.5 V
$V_{BSTRise}$	0.625 V	0.875 V	0.875 V	0.625 V

Over Voltage Protection OVP1

The OVP1 protection is triggered when there is excessive voltage on the output capacitors. This is achieved by monitoring the voltage on the VOSNS pin through a resistive divider. When the VOSNS pin rises above the $V_{OVP1Rise}$ threshold, the controller stops switching to prevent the further increase of output voltage. The output voltage that trips the OVP1 fault can be calculated with Equation 1:

$$V_{OUTOvp1} = V_{OSOvp1Rise} \times \frac{Ros1 + Ros2 + Ros3}{Ros3} \tag{1}$$

where

- $V_{OSOvp1Rise}$ is the VOSNS over voltage threshold, rising threshold
- Ros1/2/3 are the resistor values of the VOSNS resistor divider from the UCC28056EVM

$$V_{OUTOvp1} = 2.75 \times \frac{9.72M + 27.99k + 62.9k}{62.9k} = 428.9V \tag{2}$$

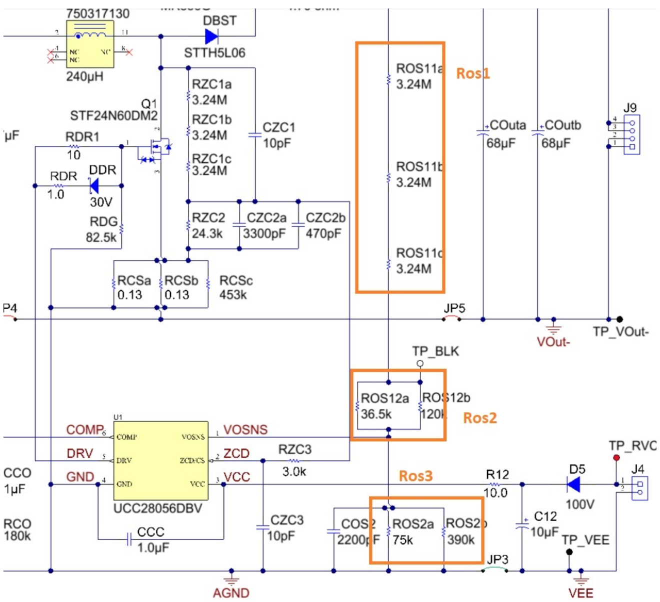

Figure 2. Reference for Output Voltage Sense Circuit

Reducing the OVP1 threshold can decrease this overshoot, provide additional margin, and prevent any component damage related to it. A lower OVP1 threshold allows for lower voltage-rated output components/capacitors, reducing system cost.

Table 3. OVP1 Threshold Variation

FEATURE	UCC28056	UCC28056A	UCC28056B	UCC28056C
OVP1 Threshold	10%	8%	10%	10%
$V_{OSOvp1Rise}$	2.75 V	2.7 V	2.75 V	2.75 V
$V_{OSOvp1Fall}$	2.675 V	2.625 V	2.675 V	2.675 V

Over Voltage Protection OVP2

This is a second level of output voltage protection, which is independent to the OVP1 sensing. The OVP2 protection is triggered when the controller senses the excessive voltage stress across the boost MOSFET. The controller monitors the voltage at the ZCD/CS pin during the discharge period (TDCH). The OVP2 trigger is considered as a long fault and the controller stops switching for 1 sec. You can estimate the output voltage at which the OVP2 triggers using Equation 3:

$$V_{OutOVP2} = V_{OVP2Th} \times K_{ZC} \tag{3}$$

where

- V_{OVP2Th} is the second-level output overvoltage fault threshold typ 1.125 V
- K_{ZC} is the attenuation factor considered as 401 per the UCC28056 EVM design

$$V_{OutOVP2} = 1.125 \times 401 = 451.125V \tag{4}$$

Once the Vout is greater than the VoutOVP2 voltage, the controller enters the fault condition and the one second restart. The resistor divider placed on the ZCD/CS pin is used to sense output voltage during inductance demagnetization time and is also used to sense converter-rectified input voltage. Based on the voltage on the ZCD/CS pin, the IC decides whether or not to switch depending on if the voltage is higher or lower than the internal Brown-in threshold. In some cases, if the customer wants to select the quiet low Brown-in threshold, it is not possible to set Brown-in and OVP2 at the desired level since they depend on the same resistor divider. The UCC28056A has the OVP2 fault disabled for applications where this fault is undesirable.