

# Why is high UVLO important for safe IGBT and SiC MOSFET power switch operation?



## Introduction

Silicon Carbide (SiC) MOSFET and Si IGBT switching power devices are primarily used in high-power applications due to their high blocking voltage rating (>650 V) and current handling capabilities. When the power devices are efficiently driven, both the switching and conduction losses are minimized. Under voltage lockout (UVLO) is implemented in gate drivers to monitor the gate voltage and prevent it from dropping below a specified threshold. The UVLO rating is an important consideration in high-power applications such as EV traction inverters, solar inverters and on-board chargers that use SiC MOSFETs or IGBTs versus Si MOSFETs. These devices have differing voltage drive requirements, so the UVLO thresholds must also be different. This application note discusses why UVLO is important for safe and efficient power switch operation. It also describes why different UVLO levels are required for Si MOSFETs versus SiC MOSFETs and IGBTs and how the gate driver architecture affects this setting.

## Si MOSFET vs. SiC MOSFET UVLO

Under voltage lockout (UVLO) is a key feature to ensure the system is protected in case of a bias supply failure. In isolated gate drivers, the voltage supply is provided at both the primary and secondary sides of the IC. The UVLO setting on the secondary side determines the minimum acceptable drive voltage for the power switch. To detect UVLO, the gate voltage,  $V_{GS}$  or  $V_{GE}$ , is compared to a preset reference voltage. Typically, at least 12V is used to fully turn on high-power IGBTs and SiC MOSFETs. The device's operating characteristics can be used to determine the appropriate voltage drive. The typical I-V curves for a Si MOSFET versus a SiC MOSFET are shown in Figure 1. The gate voltage affects the output characteristics of the device. For the Si MOSFET, the output curves remain close together until  $V_{GS}$  drops below a certain point at which they begin to saturate at different levels. When the gate drive voltage is too low, the MOSFET can go into saturation sooner (at a lower current), resulting in high conduction losses because it does not fully turn on ( $V_{DS}$  is still high). For the SiC MOSFET, the output has a much larger dependence on gate voltage as shown by the large margin between the I-V curves. As a result, SiC MOSFETs require a higher drive voltage to keep conduction losses low. Additionally, when the 6V SiC MOSFET curve is compared to the 6V Si MOSFET curve, the SiC has a much flatter response at low  $I_D$  whereas the Si MOSFET output is almost the same at high drive voltage curves. Si IGBTs also are more dependent on

the drive voltage than Si MOSFETs. Thus, Si MOSFETs can tolerate a smaller  $V_{GS}$  while still maintaining lower conduction loss while the SiC MOSFET and Si IGBT performance will suffer much more when gate voltage is lower. Typically Si MOSFETs utilize 15V or lower drive voltage and 8V (or lower) UVLO. On the other hand, SiC MOSFETs and Si IGBTs typically utilize drive voltages 15V or greater, and UVLO of 8V or greater.

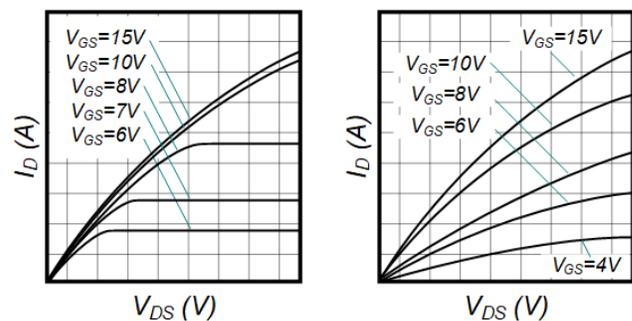


Figure 1. I-V Curves for a Si MOSFET (left) and SiC MOSFET (right).

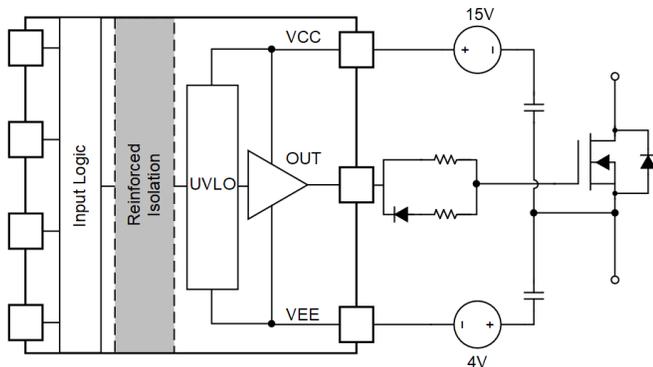
## UVLO Design Considerations

Now that the differences between Si MOSFETs, Si IGBTs and SiC MOSFETs have been reviewed, the UVLO setting and design considerations will now be addressed. The device characteristics are used to determine the optimal UVLO setting for the turn-on voltage to minimize power losses. It's also important to understand how the turn-off voltage level may also affect this setting. In high-power applications the switching losses are higher and Miller induced turn-on can be an issue, so a negative bias is typically used to turn the device off. For SiC MOSFETs this is key to enabling very fast switching and for Si IGBTs it helps to minimize the switching losses due to the current tail at turn off. With a negative bias, the gate driver architecture needs to be considered because of the referencing structure, whether to VEE or COM.

To visualize this difference, the block diagram for a gate driver where the UVLO is referenced to VEE is shown in Figure 2. Consider the case where a SiC MOSFET requires a positive drive voltage of 15V and negative drive of -4V and an 8V UVLO setting is desired. Since the driver UVLO circuit measures VCC with reference to VEE, the minimum positive drive level is much lower than the desired UVLO threshold voltage, as shown in Equation 1.

$$8V + (-4V) = 4V. \quad (1)$$

Referring back to [Figure 1](#), this low UVLO threshold will result in unacceptable performance for a SiC MOSFET. This is detrimental to the system due to high power losses and excessive heating of the device, leading to destruction. Thus, this type of UVLO referencing circuit is being used, the UVLO setting needs to be at least 12V to achieve an 8V UVLO for VCC. Otherwise, if no negative bias is used, like for Si MOSFETs, the UVLO may be set to 8V.

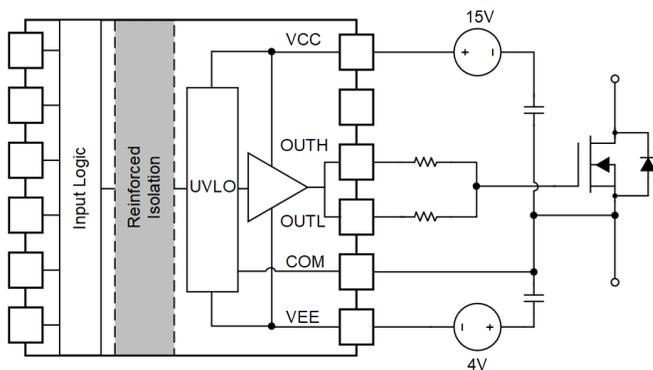


**Figure 2. Isolated driver with UVLO referenced to VEE.**

TI offers many gate drivers which also have the architecture as shown in [Figure 3](#) where VCC and VEE are both referenced to COM. In this case, if the UVLO threshold setting must be 12V, the actual UVLO threshold will be the same as shown in [Equation 2](#) because COM is the new reference point.

$$12\text{ V} + (0\text{ V}) = 12\text{ V.} \quad (2)$$

Now, the UVLO threshold is actually what the gate driver datasheet specifies and is not dependent on the negative voltage rail. This architecture, which is used in the [UCC217xx](#) family of devices, includes the benefit of monitoring both VCC and VEE. VCC is monitored to prevent excessive losses and ensure the device fully turns on while VEE is monitored to ensure the device remains off and has low switching losses.



**Figure 3. Isolated driver with UVLO referenced to COM**

## Summary

High UVLO is required for SiC MOSFETs and IGBTs in high power applications due to the device characteristics and high power system. The efficient switching of these devices is critical to prevent destruction or reduced lifetime. Knowing the differences between Si MOSFETs, SiC MOSFETs and Si IGBTs is critical to determine the best UVLO setting. Si MOSFETs can tolerate a lower gate voltage while the same setting may be unsafe for SiC MOSFETs and IGBTs. Additionally, the gate driver architecture needs to be considered to find the actual UVLO due to negative bias voltages. Thus, while 8V or lower UVLO is acceptable for Si MOSFETs, SiC MOSFETs and IGBTs typically require 10V or higher UVLO. TI offers isolated gate drivers with UVLO ranging from 5V-12V, and the option for UVLO detection of the positive voltage rail only. External circuitry may be added to reduce the UVLO setting, if required, for some applications. Proper UVLO ensures the best performance with regards to losses and reduced heating.

For more information on TI's, visit [www.ti.com/sic](http://www.ti.com/sic) or visit the product folders listed in the table below [Table 1](#). For related documents on SiC MOSFET and IGBT protection and technology, see [Table 2](#).

**Table 1. Alternative Device Recommendations**

DEVICE	OPTIMIZED PARAMETERS	PERFORMANCE TRADE-OFF
<a href="#">UCC217xx</a>	Single-output, 12V UVLO $\pm 10$ -A drive strength, and integrated isolated sensor	UVLO for both VCC and VEE available and high drive strength
<a href="#">ISO5851/2s</a>	Single-output driver with 12-V UVLO, >100-V/ns CMTI	High voltage UVLO and isolation technology
<a href="#">UCC21530</a>	Dual-output driver with 12-V UVLO, 3.3-mm channel spacing	High voltage UVLO and maximized isolation between dual driver outputs

**Table 2. Adjacent Tech Notes**

<a href="#">Understanding the short circuit protection for Silicon Carbide MOSFETs</a>	Read more about short-circuit protection methods for IGBTs and SiC MOSFET
<a href="#">Silicon carbide gate drivers - a disruptive technology in power electronics</a>	See for more information on Silicon Carbide (SiC) gate driver technology
<a href="#">Impact of an isolated gate driver</a>	Learn more about TI's outstanding high-voltage isolation technology in gate drivers

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