

bq33100 Super Capacitor Manager - Top 13 Design Considerations

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ABSTRACT

The bq33100 Super Capacitor Manager is a fully integrated, single-chip solution that provides a rich array of features for managing, charge control, monitoring, and protection, for either 2, 3, 4, or 5 series super capacitors with individual monitoring and balancing. Or, up to 9 series capacitors may be managed with only the stack voltage being measured.

This paper discusses the top 13 most important design considerations for applying the bq33100 Super Capacitor Manager IC: 1) What are the benefits and differences between Normal mode and Stack mode? 2) What configurations need attention based on use of Normal mode or Stack Mode? 3) How are the balancing components calculated? 4) Is there a need for device calibration? 5) How are the charge voltage settings determined and configured? 6) What other basic configuration parameters are needed? 7) How to size the learning load? 8) What are some alternate circuits for the learning load? 9) What are some guidelines for circuit board layout? 10) What happens if power goes off while learning is occurring? 11) What is the difference between commands 0x23, 0x24 and 0x25? 12) When does the CL bit clear? 13) Frequently asked questions.

1 What are the benefits and differences between Normal mode and Stack mode?

The bq33100 operates in one of two basic modes – Normal mode, or Stack mode. The STACK bit in the Operation Cfg Register determines the mode. In Normal mode, the voltage across each capacitor in a stack of 2 to 5 series caps is continuously monitored, and optionally balanced. In Stack mode, up to 9 caps may be stacked in series, but only the top of the stack voltage is monitored and no cell balancing is possible.

1.1 Capacitor Balancing

The series cell balancing feature of the bq33100 only operates when the device is in Normal mode. Otherwise, cell balancing is disabled. While cell balancing is critical for stacked super capacitors, there are various ways to implement it. For example, a string of resistors or resistors and opamps will sometimes be provided as part of a super capacitor “pack”. Or, a super capacitor charger with a balancing feature may be used. In this case, the balancing feature of the bq33100 may be disabled and BOM count correspondingly reduced. There are two ways to disable the balancing: First, is to setup the device for Stack mode by setting the STACK bit in the **DF:Configuration:Registers:Operation Cfg** Register. Second, is to stay in Normal mode, but simply disable cell balancing by not implementing the balancing hardware in your design. In this case if you don’t want to see the cell balance (CB) flag in the Operation Status register, set **DF:Charge Control:Capacitance Balancing Cfg:CB Threshold** to some impossible value such as 5000 mV.

Which mode should you use? It depends on whether or not you have access to the middle nodes of the capacitor stack. A super capacitor pack may, or may not, provide this access. If the middle nodes are available, then they may be connected to the bq33100 pins, thereby enabling the safety feature that monitors cell imbalance.

For super capacitor stacks of 6S to 9S, the Stack mode must be used, and cell balancing must be implemented as a function independent of the bq33100.

1.2 Stack Mode Connections

When using stack mode, care must be taken to insure that the IC pins 3(VC1), 4(VC2), 5(VC3), 6(VC4), and 7(SRP) are terminated correctly. *You must insure that the differential voltage between any two of the adjacent signals does not exceed 8 V.* This can be implemented with a set of two or more high-value resistors, depending on the maximum stack voltage in the application.

For example, if a 9S stack is to be used, with maximum voltage of 24 V, you can arrange a string of four 1-M Ω resistors with high side connected to pin 3(VC1) and bottom to ground. The 18-V tap would connect to pin 4(VC2) along with a 0.1- μ F capacitor to ground. Similarly, the 12-V tap would connect to pin 5(VC3) and the 6-V tap to pin 6(VC4) – each with a 0.1- μ F cap to ground.

The top of the cap stack is measured by pin 3(VC1) using a 1K series resistor and 0.1- μ F cap to ground from pin 3. The low side of the cap stack should be referenced to the analog ground on pin 19 of the bq33100. In stack mode, VC5 and VC5BAL pins are not used and should be connected to Vss.

2 What configurations need attention based on use of Normal mode or Stack Mode?

2.1 Stack Mode

This is the simple case. You simply set the STACK flag in the **DF:Configuration:Registers:Operation Cfg** register and you can then ignore the configuration parameters for cell imbalance, cell balancing, and cell voltage measurement calibration.

2.2 Normal Mode

The default values will be satisfactory in most cases, but you may want to review the four settings in the Safety section for cell imbalance, abbreviated as CIM. In the Charge Control section, you can review the three parameters associated with Capacitance Cell Balancing. In the Calibration section, there is actually a calibration gain (k) factor for each individual cell. While these can be ignored in many cases, it is possible to populate them with an average value that improves the factory calibration. In rare cases it may be helpful to calibrate each device individually for absolute maximum accuracy. Again, this is not recommended unless it is desired to have near perfect calibration for voltage balancing and ESR measurement. Since capacitance measurement is based on dV rather than absolute value, perfect calibration is of little importance.

To enable the use of these calibration factors, the override code of 9669 must be placed in the k-factor override flag parameter.

3 How are the balancing components calculated?

When using a fixed string of resistors, Super Capacitor manufacturers will typically specify the balancing current to be ten times the rated leakage current of the capacitors. However, when balancing is controlled by an intelligent firmware algorithm we find that significantly higher currents are useful for keeping tighter control of the voltages.

There is a simple general-rule formula that works well – use one milliAmp of bypass current per Farad. For example, at 2.1 V/cell, 100- Ω resistors will provide 21 mA for 20-F caps. Or, 5.6- Ω resistors will provide 375 mA for 350-F capacitors. Note that the balancing current is only applied as needed, and only at a max duty cycle of 40%.

The external p-channel balancing FETs should be the low voltage type, with Vgs(th) under 1 V. For low current applications, the dual si1023x is appropriate. For higher currents, the CDS23201W10 is a good choice.

4 Is there a need for device calibration?

Generally, the answer is no. Factory calibration of the internal reference and individual gain factors for each cell (except for cell 1 in a 5S configuration) will generally mean that no calibration will be required during the production process. If factory calibration errors are not suitable, it is next recommended to use an averaging approach where ten units are individually calibrated perfectly, then the average of the 10 resulting calibration constants is used for all production units. Let's address each calibration section separately.

4.1 Voltage Calibration

In Stack Mode, there is no cell balancing and the overall stack voltage calibration from the factory should be accurate to within a few millivolts over the range of interest. It should be noted that both ESR and capacitance measurements are relatively immune from calibration errors, since they are based on dV, not absolute voltage.

In Normal Mode, the accuracy of cell balancing is important but the default factory calibration should suffice. There is only one concern – the accuracy of the bottom cell (cell 1) when using a 5S configuration. The voltage measurement of cell 1 is handled differently in this case and relies on a precision external 3:1 voltage divider (see the EVM or datasheet reference schematic). Insure that these resistors are implemented as 1% or better with decent temperature coefficient. Then, calibration of this cell can also be a “don’t care” or averaging as previously described may be used.

4.2 Current Calibration

Current measurement accuracy is important since it is a fundamental quantity in the measurement of both capacitance and ESR. There are two basic error components to consider – A/D converter voltage reference and sense resistor accuracy. The offset for the current measurement is automatically measured and subtracted by the firmware routine.

The A/D converter voltage reference is factory trimmed, so nothing to worry about here. That leaves the actual value of the sense resistor as the only concern. We recommend the use of a sense resistor with 1% tolerance and 75 ppm/°C thermal coefficient. In that case, and assuming proper “Kelvin” layout, the current measurement accuracy should be well within normal requirements. Of course, it is possible to calibrate every unit, or use an average value as described in the first paragraph of this section.

4.3 Temperature Calibration

As long as a suitable 10-kΩ thermistor is used, temperature accuracy should be within ±3°C with only the factory calibration. Since temperature measurement is not critical in this application, it is expected that the need for specific temperature calibration will be rare. If better accuracy is desired, it is recommended that the user first consider the averaging approach as previously discussed before committing to individual calibration of each unit.

5 How are the charge voltage settings determined and configured?

The bq33100 controls a charge circuit in four discreet steps. The lowest voltage is the normal, also known as *nominal* voltage that will be used over most of the supercapacitor lifetime. The highest voltage is the level used for ESR and capacitance learning. The two in the middle are used to squeeze additional life out of a dying capacitor bank toward the end of its life.

Perhaps the most important consideration is to set the nominal voltage at a level recommended by the supercapacitor manufacturer for achieving the lifetime you will require. Generally, this is around 2.1 V per cell. It is recommended to set **DF:Charge Control:Charge Cfg:Chg Voltage**, **DF:System Data:Data:Design Voltage**, and **DF:Monitoring:Charging Voltage:V Chg Nominal** to 2.1 V × number of series cells.

The next consideration is the learning level. This should be configured as high as practical, given the maximum rating of the capacitor bank, and the accuracy of the charging circuit. Generally, this should be set to 2.5 V × number of series cells. There are actually two independent parameters representing this level – **DF:Monitoring:Charging Voltage:V Chg Max** and **DF:Monitoring:Charging Voltage:V Learn Max**. It is recommended to set both of them to the same voltage.

The two middle levels should be scaled to lie equally between these two extremes. For example, in the bq33100 EVM the default configuration is for 5S stack with voltage settings as follows:

DF:Charge Control:Charge Cfg:Chg Voltage = 10500 mV
DF:Monitoring:Charging Voltage:V Chg Nominal = 10500 mV
DF:Monitoring:Charging Voltage:V Chg A = 11000 mV
DF:Monitoring:Charging Voltage:V Chg B = 11800 mV
DF:Monitoring:Charging Voltage:V Chg Max = 12400 mV
DF:Monitoring:Charging Voltage:V Learn Max = 12400 mV

If you are interested in how the bq33100 decides whether or not to bump up the charging voltage as the capacitor stack nears end-of-life, here is the basic algorithm:

1. Calculate required energy in watt-seconds (Joules) based on Min Power and Required Time in seconds. These are specified in the monitoring section of the dataflash.

$$J = \text{Min Power} \times \text{Required Time}$$

2. Calculate the stack charge voltage (Max Voltage) required to provide the above energy based on the newly completed capacitance measurement. Min Voltage is specified in the monitoring section of the dataflash. C units are in Farads.

$$\text{Max Voltage} = \text{SQRT} [\text{Min Voltage}^2 + (2 \times J / C)]$$

3. Calculate effect of latest measured ESR on voltage drop.

$$\text{Vesr} = \text{Min Power} / \text{Max Voltage} \times \text{ESR}$$

4. Add the calculated ESR drop to the existing charge voltage to obtain the new charge voltage.

$$\text{New Charge Voltage} = \text{Max Voltage} + \text{Vesr}$$

5. Bump up the charge voltage as needed

6 What other basic configuration parameters are needed?

While it is recommended to review all of the configurable parameters, the great majority of them should be suitable as is. After setting the basic mode in section 1 and charge voltages in section 5, the important remaining parameters are found on the System Data, Configuration, and Monitoring tabs of the EVSW Data Flash screen.

6.1 System Data

To minimize confusion during evaluation, it is recommended to set the three capacitance parameters to the expected value of the total stack capacitance. For example, if you are using a 5S2P stack composed of 10 F capacitors, the total capacitance would be calculated as $2 \times 10 / 5 = 4$ F. Therefore:

DF:System Data:Data:Design Capacitance = 4 F

DF:System Data:Data:Init 1st Capacitance = 4 F

DF:System Data:Data:Capacitance = 4 F

In a similar way, calculate the expected ESR of the total stack. For example:

DF:System Data:Data:Design ESR = 400 mΩ

DF:System Data:Data:Initial ESR = 400 mΩ

DF:System Data:Data:ESR = 400 mΩ

6.2 Configuration

In addition to selecting the basic mode as described in section 1, it is important to configure the bq33100 for the number of series capacitor blocks if Normal mode is to be used. Use the CC0, CC1, and CC2 bits in **DF:Configuration:Registers:Operation Cfg**. The binary value in this three bit field will be set to one less than the number of series capacitor blocks. Be sure to review the meaning of each configuration bit in the bq33100 data sheet.

6.3 Monitoring

Finally, three very important parameters are located in the monitoring section of the data flash. These are:

DF:Monitoring:System Requirements:Min Power

DF:Monitoring:System Requirements:Required Time

DF:Monitoring:System Requirements:Min Voltage

Combined, these represent the energy that must be available in the supercapacitor bank at all times to insure a valid backup or other emergency operation of your system. Note that the units for Min Power are not in watts, but rather in tenths of watts.

7 How to size the learning load?

The bq33100 EVM provides a constant current capacitance/ESR learning load of approximately 500 mA. Certainly there are applications where this value is too large, and others where this level of learning current is too small. The exact value is not critical, but here are some guidelines.

First, understand the learning process by carefully reviewing the graphic, formulas, and description in the datasheet. When the learning load is turned on, the immediate voltage drop is basically an ohm's law function of the ESR and the load. The subsequent linear ramp down of voltage due to the constant current will be evaluated to measure capacitance as $c = dt \times I / dv$. A smaller load allows for a longer capacitance measurement as the capacitor is discharged from its max value to a voltage level where it can still maintain normal service of the system being protected. The longer ramp will allow more voltage samples to be taken, and therefore increase the accuracy of both the time and voltage measurements. We recommend that the learning load allow for a measurement of at least one second. For example, if the nominal capacitance is 2.5 F and minimum allowable voltage reduction (for a nearly deteriorated cap) is 300 mV, then calculated current for a 1-second ramp ($I = c \times dv / dt$) is $2.5 \text{ F} \times 0.3 \text{ V} / 1 \text{ s} = 0.75 \text{ A}$. Again, a lighter load will improve accuracy somewhat in this case.

The tradeoff is with the accuracy of the ESR measurement. Unfortunately, accuracy here is improved with a stronger load which provides a larger initial drop in voltage. It is recommended that the learning current be high enough to provide at least a 25-mV drop. For example, if the nominal ESR is 100 mΩ, then load current should be at least $0.025 \text{ V} / 100 \text{ m}\Omega = 0.25 \text{ A}$. For the 2.5 F capacitor stack with 100-mΩ ESR, an ideal learning load would be around 0.5 A.

8 What are some alternate circuits for the learning load?

The learning load circuit on the EVM reference schematic uses a bipolar transistor to implement a constant current load. The base is directly connected to the 2.7-V LDO output on pin 20, and the current magnitude is set by the emitter resistor. Because the transistor will become hot during the learning cycle, a collector resistor is used to drop some of the voltage and relieve the power dissipation problem. As mentioned in the schematic note, this collector resistor should be removed for low voltage applications.

An important consideration is the beta of the bipolar transistor, since the 2.7-V LDO output is only capable of sourcing 25 mA. For higher current applications, a good choice is a Darlington connection of two transistors or a packaged hi-gain device such as TIP120.

One way to achieve a more stable current source is to use an external LDO. Because of the error amplifier inside the LDO, the base-emitter junction temperature drift of the simpler circuit is eliminated for a slight increase in BOM cost. In that case, just substitute an appropriate LDO for the bipolar transistor in the circuit, placing its input pin in place of the collector and its output pin in place of the emitter. The ground connection of the LDO will connect to the drain of the FET switch on the bottom of the string. This forces a constant voltage across the resistor.

9 What are some guidelines for circuit board layout?

There are a few considerations for board layout of the bq33100. Please refer to the EVM schematic and layout ([SLUU466](#)).

- Note that the ground reference for the IC is at the bottom of the stack of super capacitors, not the system ground. The current is measured by the sense resistor between these two "grounds". Because the voltage of the lowest capacitor in the stack is sensed with respect to pin 19, there should be a separate dedicated trace running from pin 19 to the point on the board where the 1N connection to the stack is made.
- Place the differential filter network associated with the sense resistor's Kelvin sense lines less than one inch from the IC. Maintain a symmetrical pattern with these traces and components as demonstrated on the evaluation module layout.
- Place the 1.0-μF bypass capacitor for REG27 (pin 20) as close as practical to the IC.
- If large current transients are expected during a backup operation, insure that any high current traces are routed away from the bq33100 and that they don't run in close parallel proximity to lines associated with pins of the IC.

10 What happens if power goes off while learning is occurring?

If the system power goes off while learning is occurring and the capacitor takes over powering the application for the specified time frame, the capacitance and ESR learned will be erroneous. The device may even learn a negative ESR value as a result. The workaround for this situation is for the host to reissue the learn command once system power is restored so the gauge can relearn the ESR and capacitance.

11 What is the difference between commands 0x23, 0x24, and 0x25?

0x24 copies the value in *Design Capacitance* to **both** *Capacitance* and *Init 1st Capacitance*. Also, it copies the value in *Design ESR* to **both** *ESR* and *Initial ESR*.

0x23 measures the capacitance and ESR and **only** changes the values in *Capacitance* and *ESR*. It does not affect the initial values.

0x25 measures the capacitance and ESR and changes *Capacitance*, *ESR*, *Init 1st Capacitance*, and *Initial ESR* to the measured values.

12 When does the CL bit clear?

Once the learn command is sent or learning starts due to the learn frequency time programmed in the dataflash elapsing, the *[CL]* bit in operation status register gets set. The *[CL]* bit only clears if the super cap stack *[voltage]* is less than the sum of the *[charging voltage]* and the **taper voltage**. The taper voltage **must** be set to a value lower than the overvoltage **OV threshold**. If the **OV threshold** is greater than the **taper voltage**, once the *[CL]* bit clears, the *[OV]* bit in the safety status register will be set indicating an overvoltage condition. The *[OV]* bit is set if the capacitor stack voltage is greater than the sum of the *[charging voltage]* and the **OV threshold**.

13 Frequently Asked Questions

Q: What is the purpose of D4 in the EVM reference schematic?

A: Without D4, if the super capacitor is discharged, the base-collector junction in Q7 will forward bias and overload the 2.7-V LDO in the bq33100. D4 blocks this unwanted current path.

Q: Explain the “Cap Start Time” parameter in the monitoring section of dataflash

A: Take a look at figure 1 in the bq33100 data sheet ([SLUS987](#)). Cap Start Time is the time between points A and C. This delay insures that we will be well into the linear region before initiating data acquisition of the line from points C to D. There is generally no reason to change the default value.

Q: Explain how the FC flag works.

A: The Fully Charged (FC) flag, which is required for capacitance learning, can be set by one of two different methods. The default method is to set the flag upon primary charge termination. Rules for this are in the data sheet. In this case, the **DF:Charge Control:Full Charge Cfg:FC Set % = -1**. Alternatively, this data flash parameter can be set to a specific state of charge, and crossing that threshold will then set the flag. The flag is cleared when *RelativeStateOfCharge* is less than the value programmed in **DF:Charge Control:Full Charge Cfg:FC Clear %**.

Q: Do I have to have the SMBus / I2C communication available in my system in order to use the bq33100?

A: No. As a minimum, the host system can simply monitor the fault pin for an indication that maintenance is required.

Q: Why does the bq33100 not have a discharge FET?

A: A discharge FET in the circuit is redundant because the capacitors should be able to immediately provide power to the application if the system power gets cut off. The ability to be able to discharge supercapacitors to 0 V, unlike batteries, eliminates the need to protect the capacitors from discharging further once they reach a particular voltage level. Having a discharge FET in the discharge path will introduce issues as the discharge FET driver would be turned off once the cap voltage reaches the shutdown voltage of the chip, thus cut off supply to the application.

Q: How is the relative state of charge (RSOC) calculated?

A: The charge stored in a capacitor is the product of the capacitance and voltage. The bq33100 calculates the RSOC according to the following formula:

$$\frac{\text{voltage} - \text{minimum voltage}}{\text{charging voltage} - \text{minimum voltage}} \times 100\% \quad (1)$$

Where voltage is the super cap stack voltage, charging voltage is the voltage level specified by the gauge for charging the caps and minimum voltage is the value specified in data flash. Notice the absence of the capacitance as its presence in the numerator and denominator cancels out.

Q: Can the learning be set to occur more frequently for test purposes?

A: Yes, setting the learn frequency register to a value of 250 in unsealed mode causes the learning to occur every 10 minutes.

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