THE NEW UC3879 PHASE-SHIFTED PWM CONTROLLER SIMPLIFIES THE DESIGN OF ZERO VOLTAGE TRANSITION FULL-BRIDGE CONVERTERS

by Laszlo Balogh

INTRODUCTION

This Application Note will introduce the UC3879 integrated circuit and compare its performance to its predecessors, the UC3875/6/7/8 controller family. These integrated circuits provide all necessary control, decoding, protection and drive functions to successfully manage the operation of the full-bridge converter with phase-shifted control. This integrated solution greatly simplifies the design procedure and offers significant savings in development time and printed circuit board real-estate for the designer.

Using the conventional full-bridge topology with phase-shifted control technique has already demonstrated its superiority in medium to high power, DC-to-DC power conversion. This control method provides well controlled dv/dt values and zero-voltage switching of all primary side semiconductors in the power stage over nearly all operating conditions. Several publications [1-8] discussed the details of operation including equivalent circuits for the resonant transitions for both legs of the bridge converter, conditions for zero-voltage switching and describing further improvement possibilities. The major benefits offered by this approach are a simpler power stage than its hard switched counterpart, utilizing circuit parasitics instead of being penalized by them, improved efficiency and lower EMI level. These significant advantages are realized with a slightly more complex control algorithm.

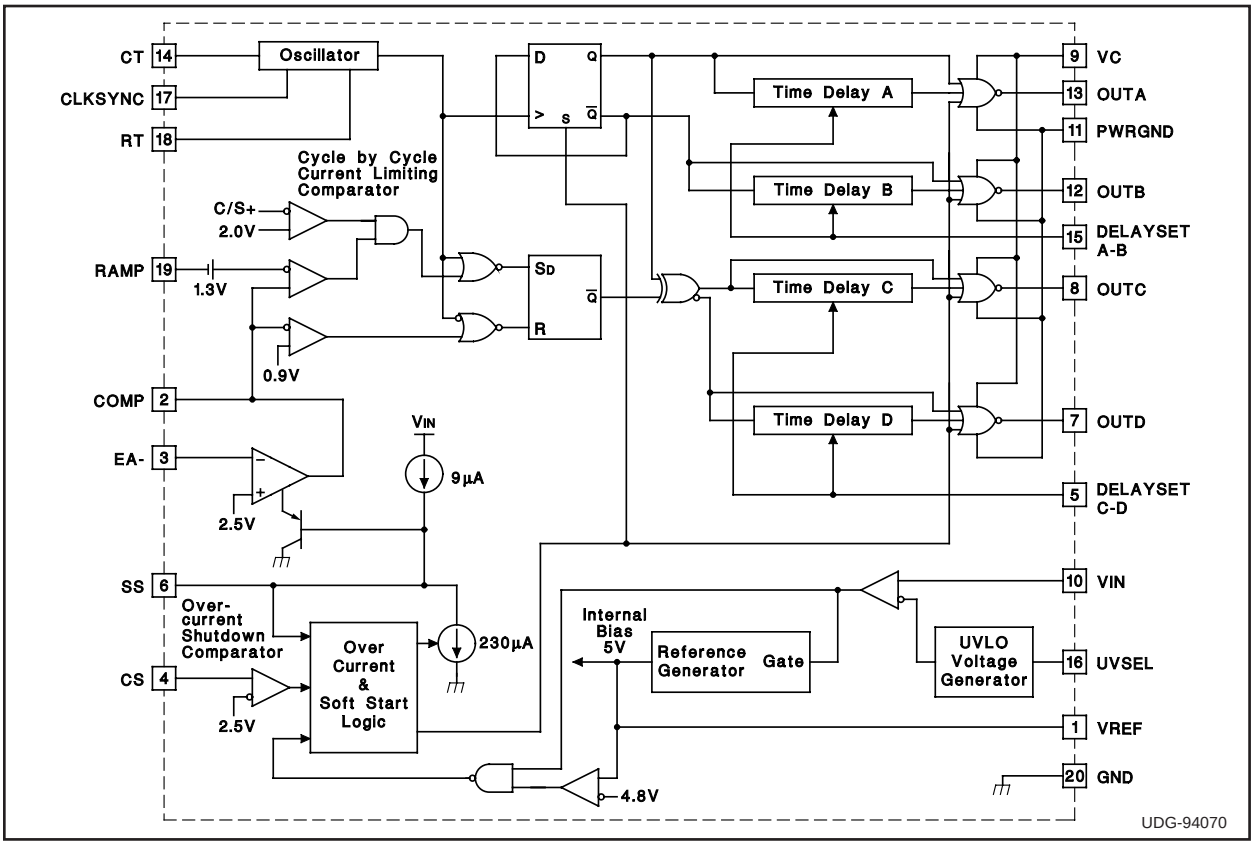

Figure 1. UC3879 Block Diagram

UNITRODE UC3879 PHASE-SHIFT PWM CONTROL IC - BLOCK DIAGRAM

The UC3879 is an improved version of the previously introduced UC3875 controller family. The internal architecture of the IC is shown in Figure 1.

The undervoltage lockout level of the UC3879 is user selectable by the UVSEL pin. Two predefined thresholds are available. If the UVSEL pin is floating, the chip starts running when the supply voltage exceeds 15.25V on the VIN pin. In case the UVSEL pin is externally connected to the VIN pin, operation starts at 10.75V. Independent of the selected start up option, the UC3879 goes to an undervoltage lockout mode when the input voltage falls below approximately 9.25V. The threshold levels reflect the two most commonly used auxiliary power generation methods; bootstrap or off-line.

The operating frequency of the synchronizable oscillator is programmed by two external components. The resistor from the RT pin to ground defines the charge current of the timing capacitor while the discharge current is internally fixed at 10mA. This way, the duty-cycle (D_{OSC}) of the oscillator, which corresponds to the duty ratio of the signal appearing on the CLKSYNC output of the IC, can be set accurately based on the relationship:

$$RT = \frac{2.5V}{0.01A \cdot D_{OSC}}$$

The minimum recommended pulse width for reliable operation is around 250nsec and for all practical applications it should not exceed 500nsec. Hence, D_{OSC} shall be determined based on the clock frequency as:

$$D_{OSC} = (250nsec...500nsec) \cdot f_{CLOCK}$$

The timing capacitor, connected between the CT pin and ground, in combination with the already defined RT value determines the clock frequency (f_{CLOCK}) by the following formula:

$$CT = \frac{(1 - D_{OSC})}{1.08 \cdot RT \cdot f_{CLOCK}}$$

In practice, the selection of proper capacitance values are much more difficult than those of the resistors. Therefore, one might first select the appropriate capacitor value to fulfill the requirement based on the following simple table:

Frequency Range	Capacitance
f_{CLOCK} < 30kHz	2.2nF
30kHz < f_{CLOCK} < 100kHz	680pF
100kHz < f_{CLOCK}	220pF

After choosing the value of the timing capacitor, the required resistance can be calculated as:

$$RT \cong \frac{0.47 + 0.07 \cdot \sqrt{47.17 - 5 \cdot 10^4 \cdot CT \cdot f_{CLOCK}}}{CT \cdot f_{CLOCK}}$$

Figure 2 shows the solution of the timing equations for the most commonly used frequency range. It offers a quick guide to estimate the required resistor value.

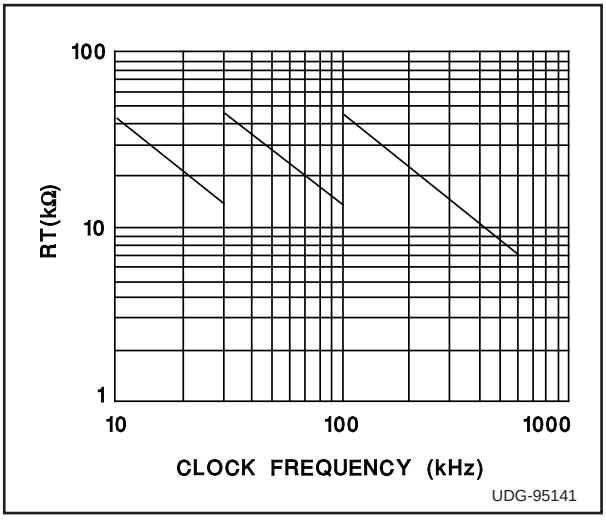

Figure 2. Timing Resistor (RT) vs. Oscillator Frequency

During free-running operation the capacitor voltage changes between nearly 0V and 2.9V linearly. Typical operating waveforms for free-running and synchronized operation are demonstrated in Figure 3.

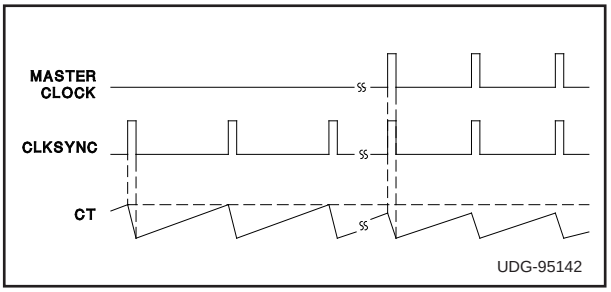

Figure 3. Oscillator Waveforms
a) Free-running; b) Synchronized Operation

Synchronization can be attained by driving the CLKSYNC pin from another UC3879 or by external circuitry as shown in Figure 4.

In both cases, all ICs will synchronize to the IC or external clock signal with the highest free-running frequency. The resistors R1 to Rn may be needed to properly terminate the synchronization bus and to keep the sync pulse narrow due to capacitance loading the line.

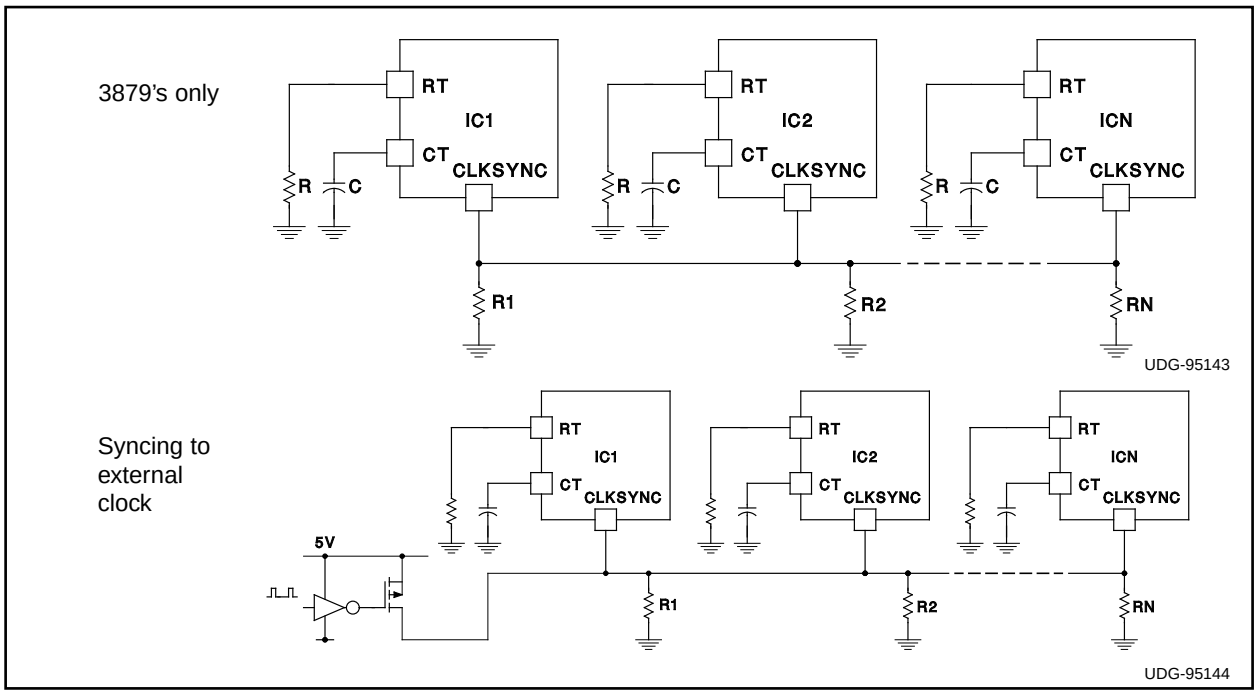

Figure 4. Typical Synchronization Schemes

An additional benefit of using local timing components for each individual oscillator is that it allows the synchronizing connections among the ICs to be broken without any local loss of functionality.

Output regulation is achieved using the 10MHz gain bandwidth on-board error amplifier. The noninverting input of the error amplifier is internally connected to a 2.5V reference. The inverting input (E/A–) and the output of the amplifier (E/A OUT) are accessible for feedback and compensation purposes. The output of the error amplifier is utilized to command the high speed PWM circuit. This signal is compared to the RAMP input of the IC having a usable input voltage range from zero to 2.9V.

Soft-start is accomplished with a capacitor from the soft-start pin (SS) to ground. During the soft-start period, the soft-start output of the error amplifier is clamped to the capacitor voltage which is gradually increased from zero to about 4.8V. It corresponds to pulse width, phase shift or peak current limiting

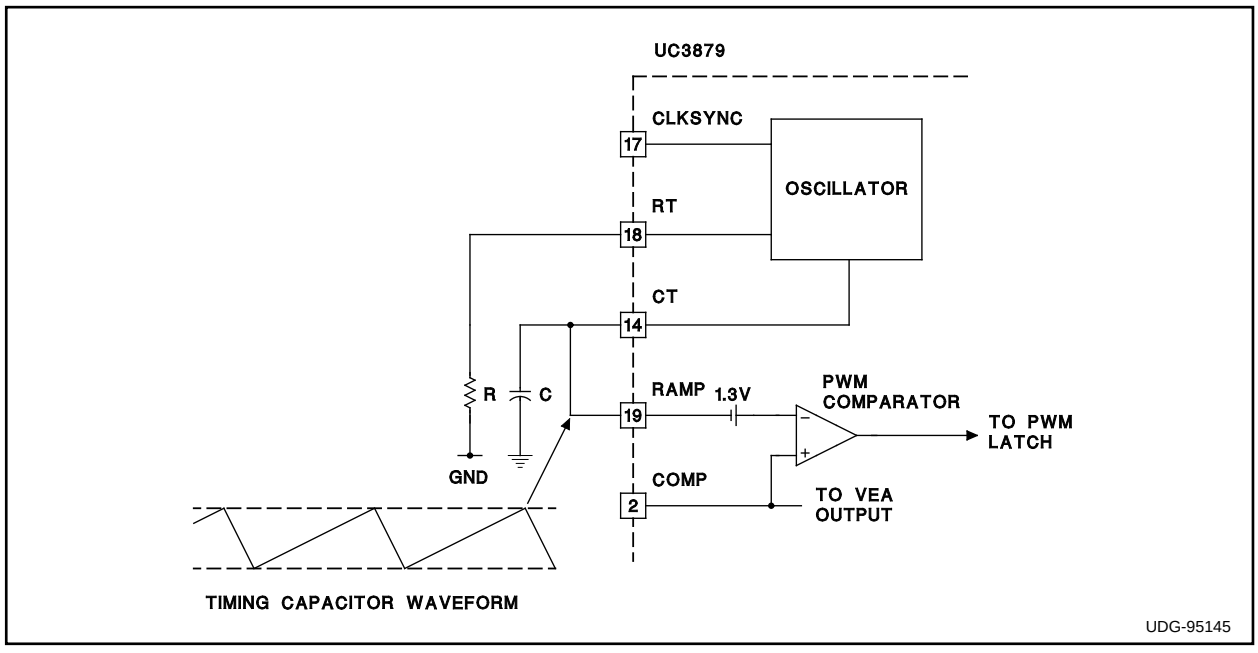

Figure 5. UC3879 with Voltage Mode Control

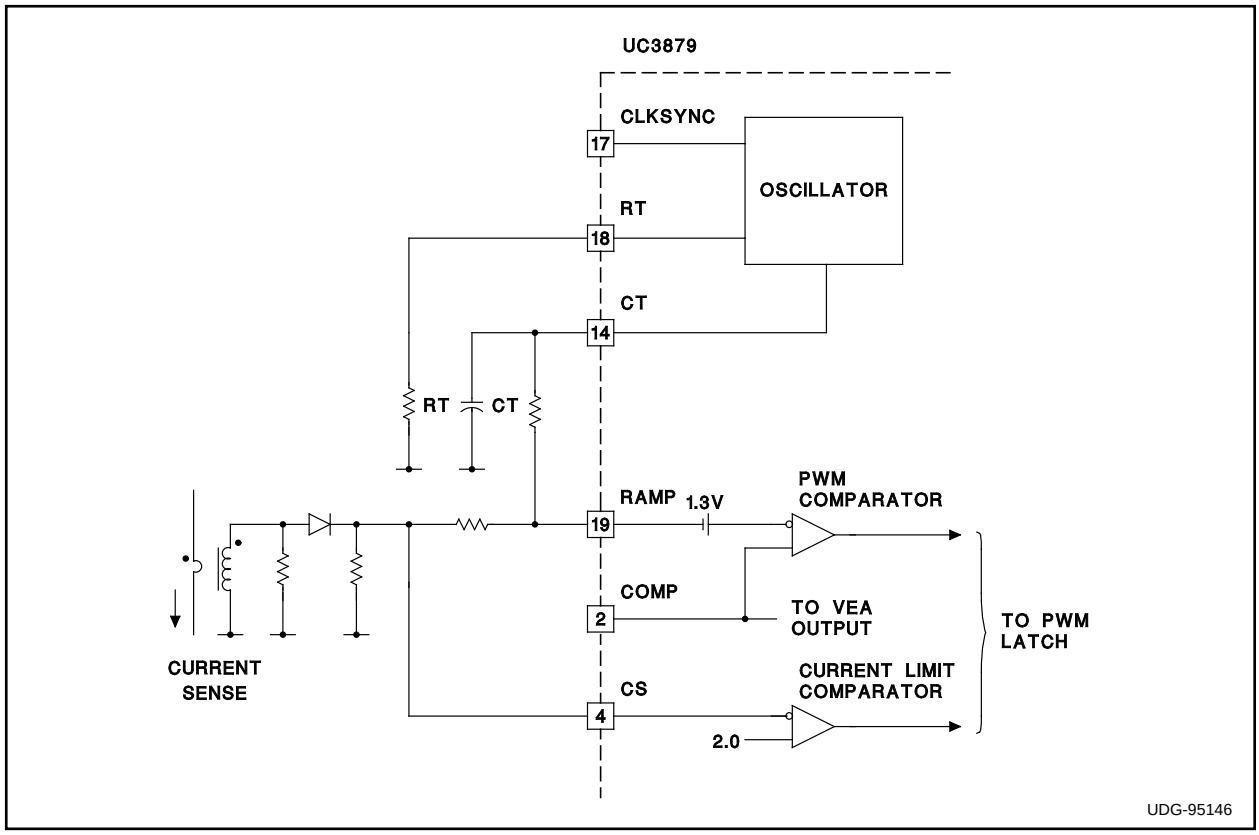

Figure 6. UC3879 with Peak Current Mode Control

depending on the exact implementation.

The UC3879 is equally suited for conventional voltage mode control or for peak current mode control. When used in voltage mode, the CT signal is directly fed to the RAMP terminal as indicated in Figure 5.

In current mode operation, the RAMP signal is the sum of the current sense signal and the slope compensation, derived from the voltage across the timing capacitor as it is shown in Figure 6.

Fault protection is established by two independent current limiting circuits which accept a 0V to 2.5V amplitude maximum current sense signal on their CS input pin. They provide cycle-by-cycle and shutdown type current limit protection in both voltage or

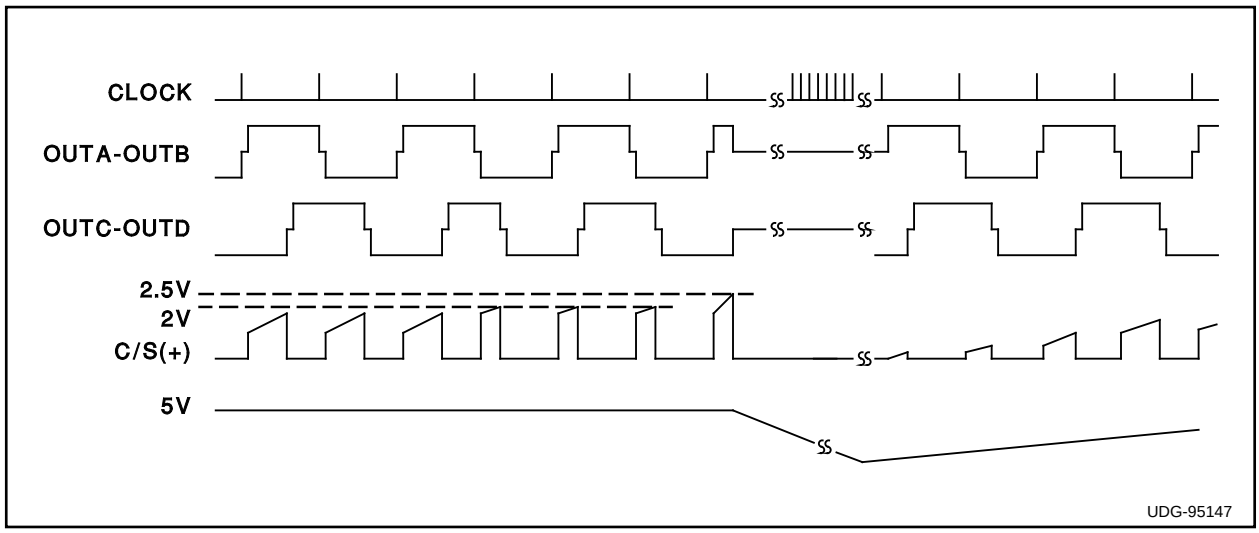

Figure 7. Operation of the Current Limiting Circuits (typical waveforms)

current mode operation. The characteristic waveforms are presented in Figure 7.

The fault protection circuits are inactive until the instantaneous voltage on the CS pin remains below the first threshold of 2V. When the signal on the CS pin exceeds 2V the existing output pulse is terminated. This first level of overload protection provides an effective defense mechanism to protect the primary side semiconductors against excessive current stress and to establish a rough input power limitation for the converter based on cycle-by-cycle current limit action.

At more severe overload conditions, this protection method is not adequate. For these cases, the UC3879 offers a second level of security. When the current sense signal on the CS pin would exceed, even momentarily, the 2.5V maximum value, the IC will initiate a full soft-start cycle to prevent catastrophic failure. If the load conditions do not change, hiccup mode will be established to reduce component stresses and to limit average power dissipation to a fail safe level.

The four totem pole OUTputs of the UC3879 can each deliver 100mA peak drive current. These outputs are intended to drive external gate drive circuits. This enhances the robustness of the overall design. To further reduce the noise transmitted back to the analog circuitry, the output section features its own collector power supply (VC) and ground (PGND) connections. Local decoupling capacitors and series impedance to the auxiliary supply improves performance even more.

The steady state timing relations for the four outputs are shown in Figure 8.

Delays between the output drive commands to facilitate Zero Voltage Switching operation are programmed at the DELAYSET inputs. Delay time is determined by the current flowing from the delay set pin to ground through a resistor, R_{delay}. Timing accuracy will improve by using a current sink connected to the delay set pins in place of the resistors. The delay time can be calculated by the following equations:

$$t_{delay} = \frac{249.6 \cdot 10^{-12}}{I_{delay}} \text{ [sec.]}$$

where

$$I_{delay} = \frac{V_{delayset}}{R_{delay}};$$

$V_{delayset}$ = delay set pin voltage (2.4V typ.);

R_{delay} = resistor value from delay set pin to GND.

One unique feature of the UC3879 is the ability to separately program the A-B output delays differently from the C-D outputs. This capability accommodates the different energy levels available for the resonant transitions of the leading and trailing legs of the bridge circuit [7-9]. Inability to optimize each of these durations will generally result in loosing zero voltage switching of the full-bridge converter switches under some operating conditions.

The optimum delay time, on the cycle-by-cycle basis, is the function of the actual current flowing in the primary winding of the transformer. This current

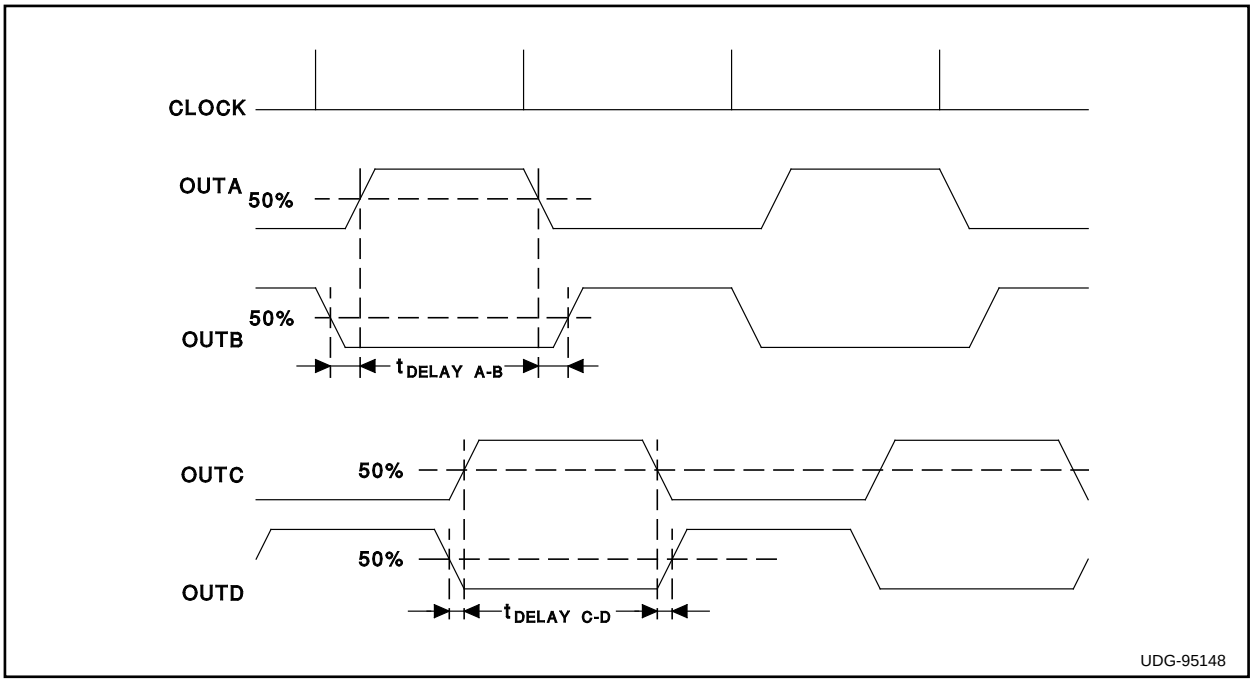

Figure 8. Output Timing Diagram for Steady State Operation

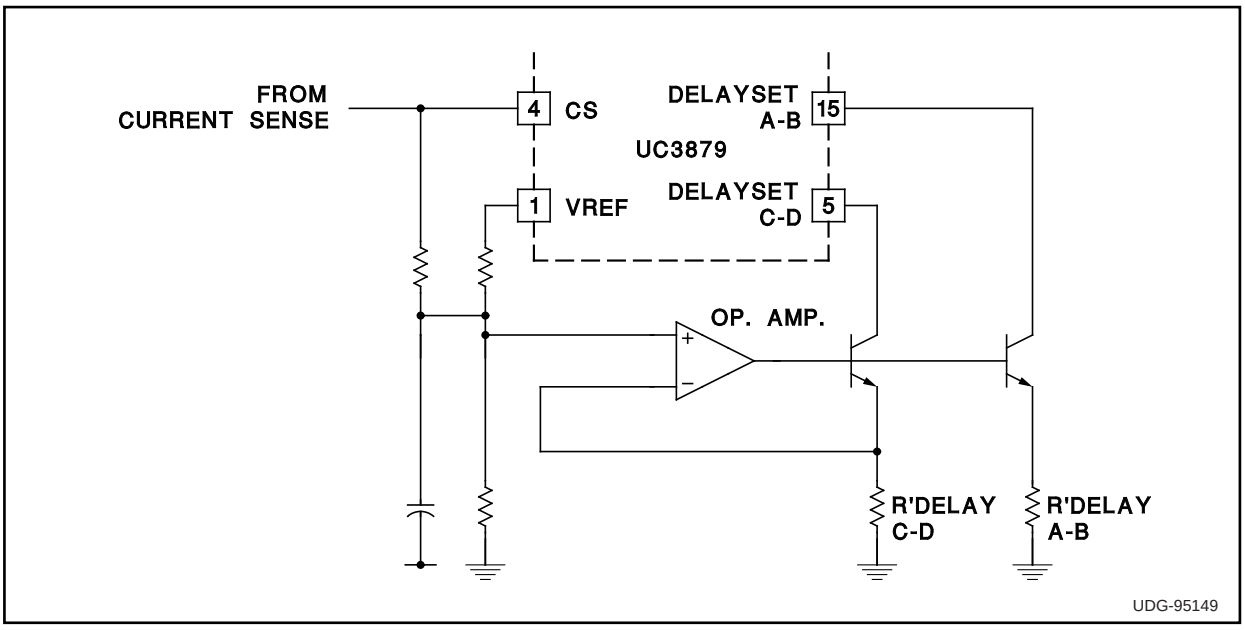

Figure 9. Adaptive Control of Delay Times

value can easily change by a factor of 10 to even 100 depending on load conditions. This causes a large variation in the required delay time, thus adaptive programming of delays might be desirable for certain applications.

Figure 9 introduces a simple external circuit to achieve variable delay times based on the momentary value of the sensed current.

The resistor network connected to the positive input of the operational amplifier determines the ratio of the minimum and the maximum delay times. The actual values of $t_{delayA-B}$ and $t_{delayC-D}$ can be scaled by the resistors between the emitters of the respective transistors and ground.

As these delays can be realized in several ways along the external gate drive circuits, setting zero delay is also offered by simply connecting the delay set inputs to the IC's 5.0V reference.

The precision, short circuit protected 5.0V bandgap reference is available for external functions as well.

UC3879 VS. UC3875/6/7/8

Although the UC3879 retained the operating principle and the basic architecture of the UC3875, it is still important to draw attention to the enhanced and added features of the new IC. The differences between the two controllers are summarized in Table 1. Their consequences for the circuit design will also be highlighted.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit utilizes a logic input (UVSEL) to select between the two available turn-on voltages (15.25V/10.75V). The advantage of this solution is that it can configure the undervoltage lockout threshold without external components. The UC3879 provides the same undervoltage lockout

Features	UC3875/6/7/8	UC3879
Undervoltage Lockout	Fixed at 15.25V/10.75V	Selectable
Supply Current	45mA typ.	27mA typ.
Oscillator Section	up to 2MHz operation	up to 600kHz operation
Error Amplifier	noninverting input accessible	noninverting input tied to 2.5V
Cycle-by-cycle Current Limiting	not available	implemented
Time Delay Circuits	60ns minimum delay	0 delay available
Output Drivers	4 x 2A totem-pole	4 x 100mA totem-pole

Table 1. Comparison of Unitrode's Phase-Shifted PWM Control ICs

levels that were offered by multiple part numbers in the UC3875/6/7/8 family.

SUPPLY CURRENT

The supply current demand (I_{IN}) of the UC3879 has been significantly reduced. While the startup current stayed the same, approximately 150µA, the operating supply current of the circuit decreased from 45mA to about 27mA. The gain was achieved by reducing internal bias currents. As a result, the maximum operating frequency has been lowered and the gate drive philosophy is revised. The UC3879 expects a high current gate drive device connected to its outputs opposed to the direct drive capability of the UC3875 family.

OSCILLATOR SECTION

The UC3879 features a completely redesigned oscillator circuit offering better noise immunity, temperature stability, and linearity. The charge current of the timing capacitor is constant, producing a linear, positive slope on the timing capacitor during the conduction period. The voltage level is tailored to provide ramp signal for voltage mode control directly. Likewise, slope compensation can be effortlessly accomplished using the voltage of the timing capacitor in case of peak current mode control. The operating frequency is programmed by the combination of RT and CT, which are connected to their separate pins.

ERROR AMPLIFIER

Both integrated circuits make use of a 10MHz gain bandwidth amplifier to regulate the output voltage. The noninverting input of the UC3879 error amplifier is internally wired to a 2.5V reference opposed to the UC3875 family where the reference is to be provided externally.

In constant output voltage applications, the UC3879 will save those components related to generating the reference for the feedback amplifier. Conversely, it will require more components and more elaborate solution if the programming of the output voltage, thus the reference, is required. Systems with isolation between the primary and secondary side controllers will not experience any difference in the design since the error amplifier of the control IC is usually configured as a voltage follower processing the error signal transmitted from the secondary side of the converter.

CYCLE-BY-CYCLE CURRENT LIMITING

This new feature is implemented only in the UC3879 controller. It provides exact, cycle-by-cycle current protection for the primary side switches during over-load conditions. The fast comparator utilized for cycle-by-cycle current limiting will terminate the active interval in every switching period when the current sense signal exceeds the internally set 2V reference value. This first level of overload protection is suitable to limit the maximum power to be handled by the power stage and will not result in a hiccup type of operation.

DELAY CIRCUITS

As previously described, the time between turning off one switch and turning on the other in the same leg of the bridge has a profound effect on circuit performance. Note that the programmed delay times should accommodate any delays introduced by the high current gate circuits and transformer.

Allowing zero delay between the outputs of the UC3879 provides greater freedom to the designer to implement those delays as desired. Possible other points to program the necessary delays are the inputs of the high current gate drivers or the secondary sides of the gate drive transformers. All these solutions have their pros and cons, and require careful considerations in sight of the actual application.

OUTPUT DRIVERS

The output totem pole drivers of both controllers have identical structures. They feature their own power rail connections and they are kept active low during undervoltage lockout. However, output current ratings are remarkably different. With its 2A peak current capability, the UC3875 family is prepared for direct drive of the gates or gate drive transformers of the most commonly used power switches. Yet, with the continuously increasing die sizes, separate driver chips can be advantageous to eliminate undesired power dissipation and noise generation from the sensitive analog control sections. In this regard, the UC3879 is designed to work with external high current gate drive circuits. Its fast outputs, with 100mA peak current capability, are especially appropriate to drive the TTL or MOSFET input stages of those devices.

Undervoltage Lockout		Delay Times		**UC3879**	UVSEL pin		DELAYSET pins	
Turn-ON	Turn-OFF	$\tau_D > 0$	$\tau_D = 0$	Old Part #	Float	$\rightarrow V_{CC}$	$\rightarrow V_{REF}$	R_{SET}
10.75V	9.25V	X		**UC3875**		X		X
15.25V	9.25V	X		**UC3876**	X			X
10.75V	9.25V		X	**UC3877**		X	X	
15.25V	9.25V		X	**UC3878**	X		X	

Table 2. Providing UC3875/6/7/8 functionality through the setup options of the UC3879 control IC.

UC3879 DESIGN FLEXIBILITY

Besides the several improved features and added functions, the UC3879 offers the greatest degree of design flexibility with the minimum number of external components. Table 2 shows the different setup possibilities to achieve the same functionality offered by four different part numbers in the UC3875 family.

SUMMARY

As demonstrated, the UC3875/6/7/8 and the UC3879 integrated circuits are dedicated to eliminate most of the difficulties associated with implementing the numerous auxiliary functions and the tedious control algorithm of the full bridge converters with phase-shifted control. The single chip solution with its carefully optimized signal levels and minimum number of external components provide the fast track in the controller design for one of today's most promising power conversion techniques.

REFERENCES

[1] R.A. Fisher, K.D.T. Ngo, and M.H. Kuo, "A 500 kHz, 250 W dc-dc converter with multiple outputs controlled by phase-shifted PWM and magnetic amplifiers", Proc. High Frequency Power Conversion Conference, pp. 100-110.

[2] L.H. Mweene, C.A. Wright and M.S. Schlecht, "A 1 kW, 500 kHz front-end converter for distributed power supply system", Proc. APEC '89, pp 423-432.

[3] D.B. Dalal, "A 500 kHz multi-output converter with zero voltage switching", Proc. APEC '90, pp. 265-274.

[4] J.A. Sabate, V. Vlatkovic, R.B. Ridley, F.C. Lee and B.H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switching PWM converter", Proc. APEC '90, pp. 275-284.

[5] R. Redl, L. Balogh and N.O. Sokal, "A novel soft-switching full-bridge dc/dc converter: analysis, design considerations, and experimental results at 1.5 kW, 100 kHz", Proc. PESC '90, pp. 162-172.

[6] W.M. Andreycak, "Phase-shifted, zero voltage-transition design considerations and the UC3875 PWM controller", Application Note U-136, Unitrode Product & Applications Handbook 1993-94, pp. 9.393-9.406.

[7] W.M. Andreycak, "Designing a phase shifted zero voltage transition (ZVT) power converter", Topic 3, Unitrode Power Supply Design Seminar SEM-900.

[8] R. Redl, L. Balogh and D.W. Edwards, "Optimum ZVS full-bridge dc/dc converter with PWM phase-shift control: analysis, design considerations, and experimental results", Proc. APEC '94, pp. 159-165.

[9] R. Redl, L. Balogh and D.W. Edwards, "Switch transitions in the soft-switching full-bridge PWM phase-shift dc/dc converter: analysis and improvements", Proc. INTELEC '93, pp. 350-357.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.