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APPLICATION NOTE

New Integrated Circuit Produces Robust, Noise Immune System For Brushless DC Motors

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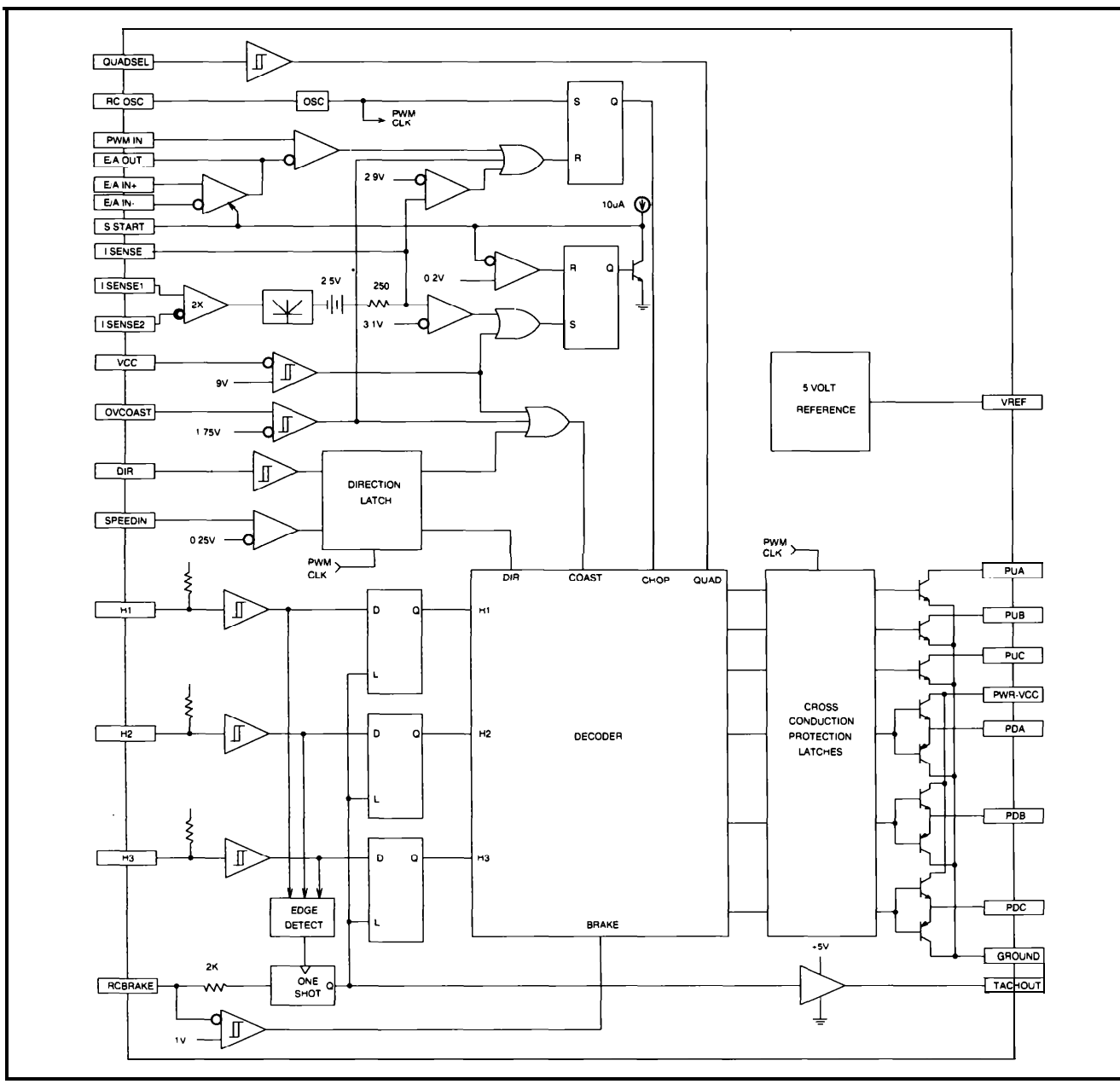
Abstract

A new integrated circuit for brushless DC motor control is presented that implements many new techniques to enhance reliability and reduce the detrimental effects of noise. In addition to safety features and noise rejection circuitry, the new circuit contains a complete pulse-width modulator (PWM), a practical tachometer, a precision voltage reference, a high-speed current-sense amplifier, and high-voltage, high power, output stages.

Various applications of the IC are discussed in detail, including using the PWM for fixed frequency and fixed off-time control, driving power MOSFETs, driving bipolar power transistors, and sensing winding current. The IC is shown in applications that allow braking and direction reversal without damage to the motor or the power semiconductors.

BLOCK DIAGRAM OF THE UC3625



The Problem

Conventional brush motors have proven reliable and versatile. They remain popular partly because the pressures to improve haven't been high, and partly because nothing better has been available that is practical. Brushless DC motors (BDCMs) can pack the same horsepower into smaller, lighter boxes. They can also accelerate faster due to inherently lighter rotor construction. Without the friction and arcing of brushes, they are acoustically quieter. As they have permanent magnet rotors, they are faster to manufacture. Permanent magnet rotors also dissipate very little power, so BDCMs have far less heat dissipation problems.

One thing that has held the motor industry back has been the availability of economical control electronics. Recent price trends in power MOSFETs and monolithic motor controllers have reduced these limits. The final hurdle to broad acceptance is assurance of reliability. Brush motors proved their reliability not through design, but instead through over a hundred years of development of rugged brushes and slip rings.

Two problems with BDCMs today are performance and reliability in the presence of noise. Noise here can refer to externally generated electromagnetic noise, internally generated chopping noise, or inappropriate commands from the operator of the system.

The UC3625 specifically addresses the need for an economical, robust BDCM controller by specifically addressing these failure modes and also by implementing many functions and features desirable in high performance motor systems. The following table outlines some of the important features of the UC3625:

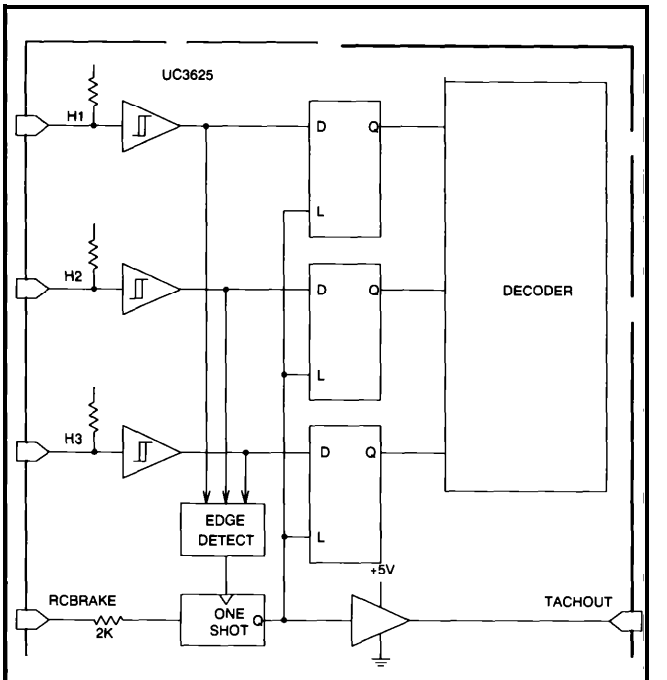
- Push-Pull Low-Side Drivers
- Versatile High-Side Drivers
- Complete PWM
- Two or Four-Quadrant Chopping
- Tachometer
- Soft Start
- Undervoltage Protection
- Overvoltage Protection
- Active Safe Braking
- Differential Current Amp
- Hysteresis on all inputs
- Direction latch
- Cross Conduction prevention

Unique Features For Noise

All logic inputs to the UC3625 have hysteresis and /or latches for maximum noise rejection. The position sensor inputs specifically contain 0.8 volts of hysteresis, yet still meet TTL input thresholds. These inputs also contain pull-up resistors allowing them to directly interface to open-collector sensors.

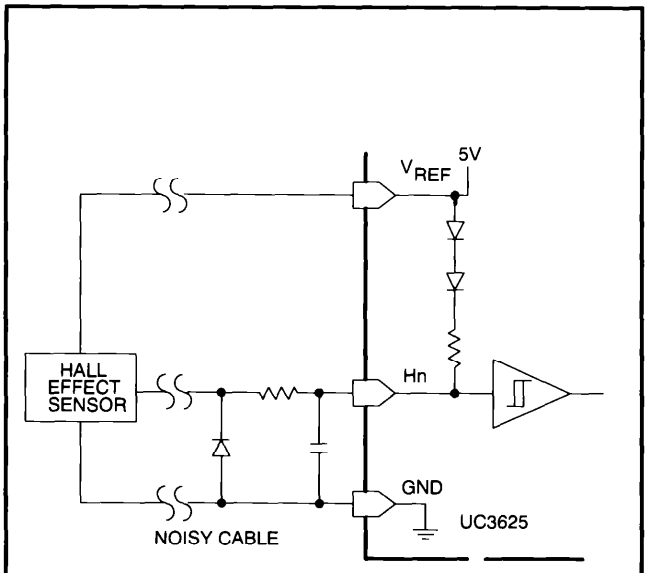
Position sensor inputs are latched immediately following commutation, and remain latched through the on-time of the tachometer monostable (one-shot). This prevents commutation noise from reaching the decoder, latching out the largest noise spike in the motor system. Although this sets a maximum motor speed, correct choice of pulse width guarantees operation up to the maximum speed of the motor while still affording excellent noise rejection.

The one-shot pulse also drives a low saturation-voltage driver connected to TACH OUT. The average value of the voltage on TACH OUT is directly proportional to motor speed, so that the pulse generator doubles as a simple tachometer.



Tachometer Doubles As Input Noise Gate

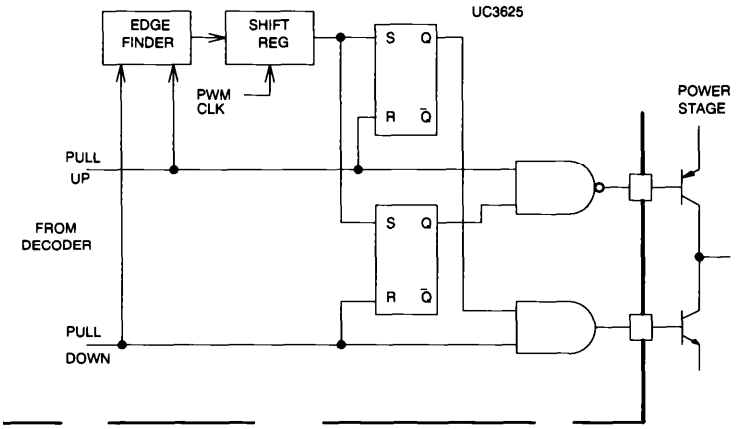
Even with input latches, external noise filtering is often valuable. Chopping noise lends itself to analog low-pass filtering because of its dominant high-frequency components. As high-frequency noise energy can be very strong, zener clamping ahead of the filter can be very effective.



Suggested External Non-Linear Filter For PWM Noise

Cross-Conduction Prevention

To further assure noise immunity, the UC3625 contains latches and a shift register to guarantee that all power stages turn off and remain off for a minimum time before changing states. In addition to preventing noise-induced cross conduction, this prevents cross conduction due to slow power stages.



Logic That Prevents Cross Conduction

The delay time is only inserted when an output is commanded from high to low or vice versa. During normal three phase commutation, outputs are turned off (opened) for a full cycle before changing states, so this delay will not impede normal operation. The only times that this delay will be inserted are during noise spikes, direction reversal, and braking.

Pulse-Width Modulation System

Motors perform better with higher operating voltages because for a given value of inductance, higher voltages can change winding current faster. A necessary adjunct to higher supply voltages is current control, either by linear amplifiers of pulse-width modulation (PWM). The UC3625 uses fixed frequency PWM for chopping.

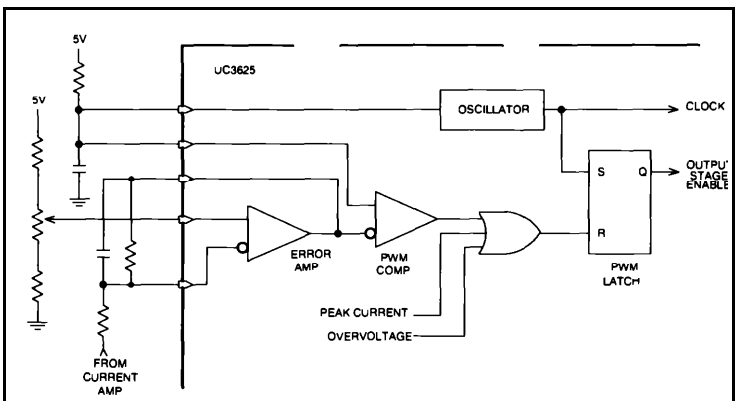
At the heart of the PWM is a sawtooth oscillator. The oscillator is programmed up to 500kHz with one resistor to the reference and one capacitor to the ground. This oscillator is used to enable the PWM latch every cycle, and also to clock the protection shift registers.

Another fundamental part of the PWM is the PWM latch. The output of this latch enables the power stages. The latch is set once per cycle by the oscillator, and cleared by either the PWM comparator, a peak current signal generated in current-sense circuitry, or by a fault signal from the OV/COAST input. This latch is reset dominant, meaning that a steady reset signal from any of three sources completely inhibits the power stages.

The other elements in the PWM are the PWM comparator and the error amplifier. The PWM comparator is an NPN-input comparator dedicated to comparing the output of the error amplifier to some other signal such as a command voltage, ramp, or sensed signal. The error amplifier is a PNP-input op-amp compensated for unity-gain operation, who's inputs can operate linearly down to ground.

The PWM can be configured into any number of different loops that regulate winding current (torque is nearly proportional to winding current), regulate speed, or regulate some other parameter. The PWM is internally configured for peak current control as well, although this is not intended to be the principle feedback loop.

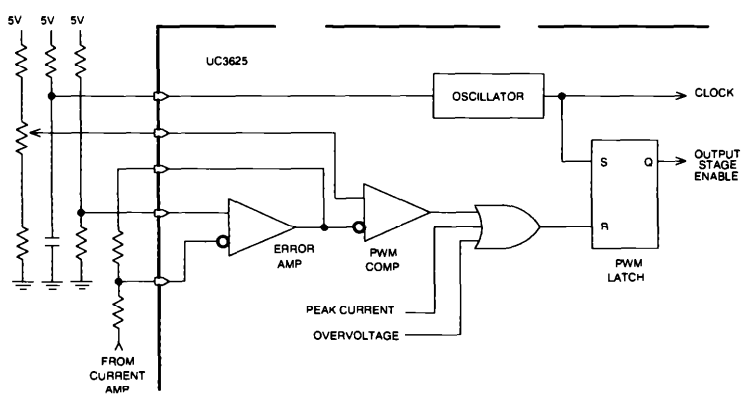
The approach above compares winding current to a DC voltage with the PWM comparator, and pulse-by-pulse regulates winding current. This is similar to "current mode" in PWM power-supply systems, and offers the advantage of removing the pole caused by load inductance from the feedback loop.



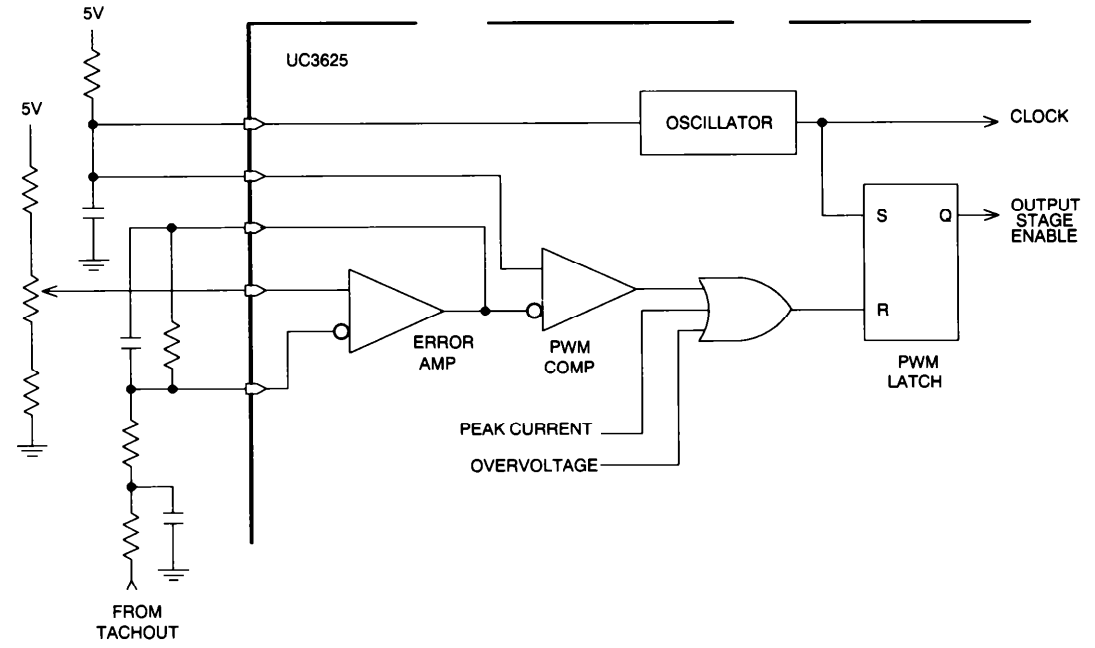
PWM Configured For Average Current Feedback

The PWM can also be configured to use the error amplifier to amplify the difference between the winding current and a desired current, and to use the PWM comparator to compare the error amp output to the oscillator ramp. This current loop operates on average, rather than peak current.

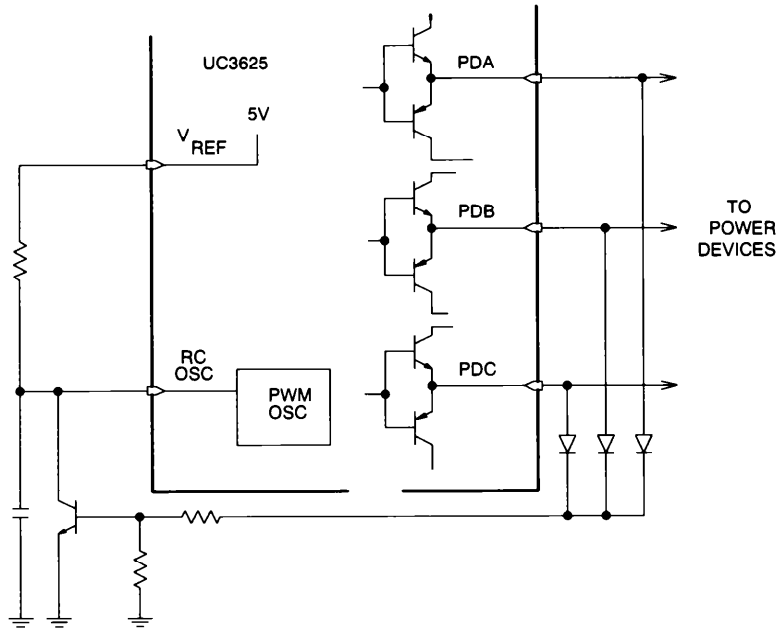
If the PWM comparator is used to compare the oscillator ramp to a DC voltage, then the load duty cycle is directly proportional to the applied DC voltage, as is the average load voltage. This "voltage mode" loop comes close to controlling speed because speed is nearly proportional to average winding voltage. If an overall speed feedback loop is required to regulate speed, this "voltage mode" topology can serve as a local feedback loop to make the system transfer function more linear, and the error amplifier can be used as the overall loop amplifier.



UC3625 PWM Block Diagram Configured For Pulse-By-Pulse Current Control



Voltage Mode Speed Control



Circuit for Fixed Off-Time PWM Using the UC3625

The advantages of each topology must be weighed considering complexity, overall stability, and sensitivity to load. In cases where current feedback seems nearly impossible to compensate, some compromise between current feedback and voltage feedback is dictated.

The PWM is also configurable to fixed off-time PWM rather than fixed frequency PWM by adding a few external components that couple the output off signal back into the oscillator.

Fixed off-time control is sometimes desirable because it uses one of the easiest feedback loops to compensate. Its main drawback is that the modulation frequency varies with load and speed. This means that for some loads chopping noise can become audible (below 20kHz). This also allows variation in the dead time inserted to prevent output stage cross conduction.

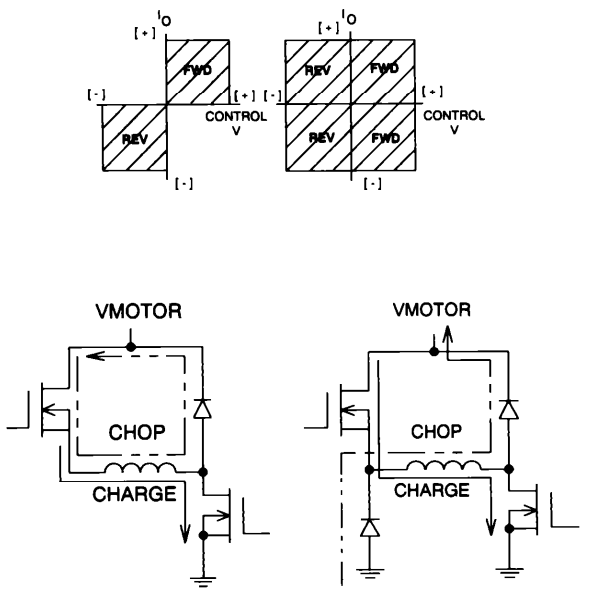
Different Chopping Techniques

Chopping capitalizes on the inductance of the load to maintain load current when the driving voltage is removed. The driving voltage is normally supplied through power switches, and diodes normally conduct across the load when the switches are opened.

Two different methods are common for chopping. The more efficient method chops one low-side power switch while one high-side switch is on. This is referred to as a two-quadrant PWM.

Two-quadrant PWM normally operates with a low duty cycle, as winding current is charged principally by the supply voltage, yet winding inductance is discharged by the voltage drop in the diode circuit (see figure below). Motor back EMF reduces the effective supply voltage and increases the effective diode voltage drop, so the duty cycle tends to increase with speed.

The main advantage of two-quadrant chopping is efficiency. Its main drawback is that it can't quickly decrease winding current. This can be very troublesome in position feedback systems.



Two-Quadrant vs. Four-Quadrant Chopping

In contrast, four-quadrant PWM systems chop both switches, and circulate load current through two diodes backwards into the supply.

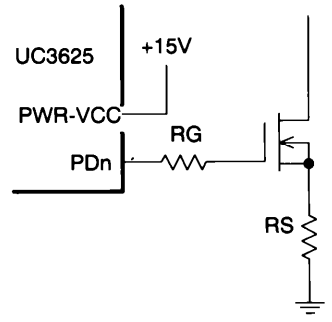
Again ignoring back EMF, four-quadrant chopping produces a nearly symmetrical current waveform, as current rises due to the supply voltage impressed on the load inductance, and decays due to reverse supply and load inductance. With four-quadrant chopping, a motor can decelerate as quickly as it can accelerate.

To program the UC3625 for one approach or the other, apply a logic signal to the QUAD SEL input. QUAD SEL can also be changed during operation to tailor performance to specific requirements.

Power Drivers

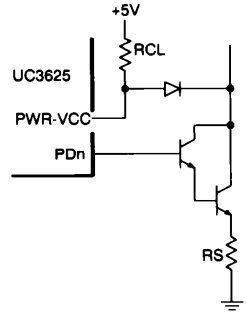
The overwhelmingly dominant power output device in new designs is the N-Channel Enhancement-Mode Power MOSFET. Bipolar power transistors and power darlingtons still have advantages in very high-voltage systems, but these advantages are being continuously eroded by developments in MOSFET structures and merged bipolar MOSFET devices. The UC3625 is able to drive both power MOSFETs and bipolar transistors.

The low-side drivers in the UC3625 are totem-poles capable of greater than 250mA peak gate or base current, but the package and the die are not constructed for continuous power dissipation greater than 1 watt, which imposes an upper limit on the available current for bipolar device drive.



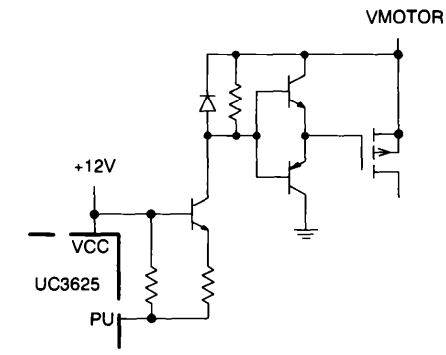
Driving Low-Side MOSFETs with the UC3625

The Power Vcc pin is separated from signal Vcc so that high gate current peaks can be isolated from signal Vcc, and also so that Power Vcc can be tailored to the power device. For fastest switching of power bipolar devices, the Power Vcc pin can be limited and clamped, as shown in this example.

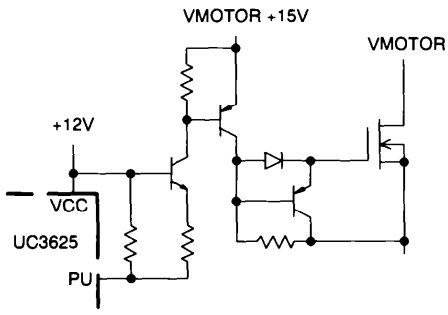


Driving Low-Side Darlingtons with the UC3625

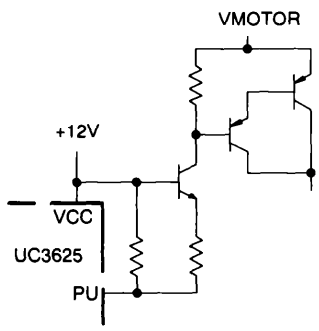
Driving high-side devices with the UC3625 requires level shifting if the motor supply is greater than 50V. The UC3625 high-side outputs are open collector NPN transistors which pull low to turn on high-side MOSFETs or bipolar transistors.



Driving High-Side P-MOSFETs



Driving High-Side N-MOSFETs



Driving High-Side PNP Darlingtons with the UC3625

Although capable of 50mA current sinking, the open collector outputs are normally operated with lower currents to minimize the power supplied by the high-voltage supply.

As a high-side switch, P-channel power MOSFETs are far easier to drive than N-Channel power MOSFETs because the gate of P-channel MOSFETS need not be pulled above the positive supply to obtain low voltage drop. Unfortunately, P-channel power MOSFETs are more expensive and less available than N-channel devices, so the added supply in the N-channel design is often justified.

Current Sense

The UC3625 contains a high-speed gain-of-two differential amplifier dedicated to current sensing. This amplifier can be connected directly across a low-value current-sense resistor or between two different current-sense resistors. Since the amplifier common mode range allows operation one volt below ground, the amplifier has excellent common-mode noise rejection.

The current-sense amplifier also embodies an ideal diode that performs absolute value and level shifting of the input, giving a transfer function of:

$$Vo = 2.5 + 2\ ABS\ (Vi_2 - Vi_1)$$

If the low-side power devices and the lower catch diodes are returned to the same current-sense resistor, and the UC3625 is chopping in four-quadrant mode, then the winding current always flows through the current-sense resistor. The voltage on the current-sense resistor flips polarity every time the PWM chops, but the absolute value current-sense amplifier rectifies this, giving a smoother representation of continuous winding current, and requiring less filtering.

Some filtering of the current-sense signal is always required, however, and the output of the current-sense amplifier is the best place to filter. The amplifier is stable with all capacitive loads, and has approximately 250 ohms output impedance.

Filtering at the input of the current-sense amplifier is also valuable to remove spikes that are faster than the amplifier can track. However, to insure that the absolute value circuit continuously tracks current, use only a minimal amount of input filtering.

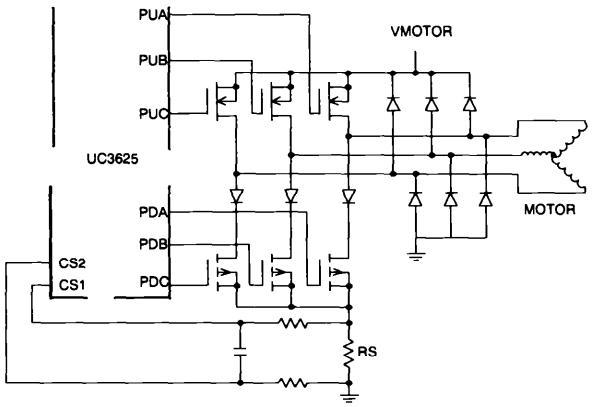
The output of the current amplifier drives two comparators through the filtering resistor: the peak current comparator and the overcurrent comparator. The peak current comparator resets the PWM latch whenever the current-sense voltage exceeds approximately 200mV. The overcurrent comparator initiates soft start if the current-sense voltage exceeds approximately 300mV.

The peak current comparator can be used to limit maximum peak winding current while a larger feedback loop limits winding current to control some other parameter, such as speed or position. The overcurrent comparator then functions as a fail-safe device that commands SOFT START if the peak current loop loses control, as might happen if a power device becomes shorted.

Is it Brake...or Break?

The UC3625 contains provisions for braking by way of a multifunction pin called “RC / BRAKE”. This pin also serves as the timing pin for the internal tachometer, pulsing between 1.67V and 3.33V every time the position sensors commutate. To command BRAKE, pull RC/BRAKE low with an open collector gate or switch. The tachometer then stops pulsing and all three low-side drivers turn on.

Normal PWM configurations do not allow braking current to be modulated because the braking current does not normally flow through the sense resistor. The motor control circuit below includes three added diodes that, during BRAKE and all other circumstances causes winding current to flow through the sense resistor. Using this circuit, the UC3625 stops a motor as fast as the peak limit current setting allows and protects the output power devices and the motor.



Circuit For Safe Braking Series diodes guarantee that braking current will flow in the current-sense resistor

Direction Reversal is Worse

As with braking, direction reversal can also force excessive current into power devices if not checked. Direction reversal forces two of the three driver channels to go from high to low or low to high directly. With the UC3625, cross conduction is completely prevented, but high winding current is dependent upon the application. The higher the speed, the higher back EMF, and the higher the potential peak current.

The approach mentioned for braking also limits peak winding current during direction reversal. In addition, the direction latch and shift register in the UC3625 can be configured to prevent direction reversal until motor speed drops to a safe level. This latch also commands COAST whenever a direction reversal is commanded and motor speed is too high.

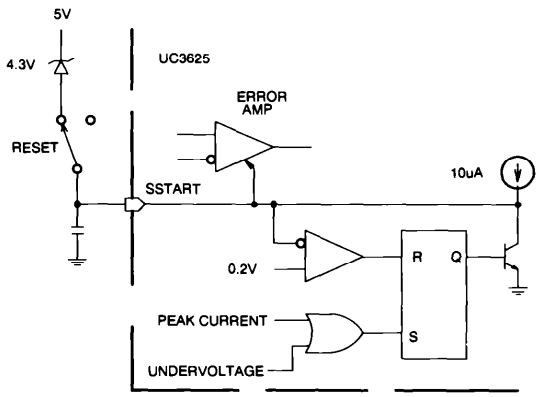
The easiest way to configure this protection is using the internal tachometer to drive “SPEED IN” through a low-pass RC filter. The “SPEED IN” threshold is set to prevent reversal whenever input voltage exceeds approximately 250mV.

Other Protection Features

To prevent confusion or insufficient drive to power MOSFETs, the UC3625 contains a comparator to lock off all six outputs until the Vcc input exceeds 9V, called under-voltage lock-out. The UC3625 also contains an uncommitted comparator that inhibits the outputs and clears the PWM latch whenever its input exceeds 1.75V. This can be used with a voltage divider for an over-voltage inhibit, or can be directly driven from TTL or CMOS for a logic controlled COAST input.

To prevent very high power supply current spikes and to limit average current during faults, the UC3625 contains latched soft start. The latch is set by low power-supply voltage or overcurrent fault, and is only cleared when the setting condition goes away and the soft start input discharges to below approximately 200mV.

Normally, the UC3625 is configured with a capacitor from soft start to ground, which is charged by the soft start 10uA current source. The UC3625 can also be configured to latch soft start until cleared by connecting a 4.3 volt zener and a normally closed switch from Vref to soft start. The switch then functions as a reset switch.



Manual Fault Reset Circuit Uses Zener Diode to Latch Faults

Voltage Reference

Finally, the UC3625 contains a precision voltage reference trimmed to 5V +/- 2%. This reference powers most of the internal circuitry for supply rejection and is available on the “Vref” pin for driving other circuitry such as Hall-effect position sensors and bias circuits. Operation of the voltage reference is guaranteed with loads up to 30mA, and the reference is also short circuit current limited to approximately 100mA.

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