UNITRODE

U-509 Using the bq2007 Enhanced Features for Fast Charge

Introduction

This application note describes the correct setup of the bq2007 features and gives design examples for a NiCd or NiMH switch-mode and gated current source fast-charger applications.

The bq2007 is targeted for applications requiring fast-charging and charge status monitoring at minimal cost. It provides sophisticated full-charge detection techniques such as PVD (peak voltage detection) and -ΔV (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd).

The bq2007 offers flexibility by providing a wide variety of charge status monitoring and charge state display formats. The internal charge status monitor can be configured to support up to a seven-segment bargraph or a single-digit display. The bargraph display indicates seven monotonic steps, whereas the single digit counts in ten steps of 10% increments. The output can direct-drive either LCD or LED interface levels.

The bq2007 indicates charge state status with an audio alarm output option and two dedicated output pins with programmable display options. The $DSEL_{1–2}$ inputs can select one of the three display modes for the $LED_{1–2}$ outputs.

Background

A significant advantage of the bq2007 over other fast-charge solutions is the flexibility to select PVD or -ΔV as the primary decisions for fast-charge termination. PVD is the recommended termination method for NiMH batteries, while -ΔV is recommended for NiCd batteries. -ΔV or PVD detection in the bq2007 may be temporarily disabled during periods when the charge current fluctuates. -ΔV or PVD may be permanently disabled without affecting other bq2007 charge-termination functions.

The bq2007 provides battery protection by trickle-charge conditioning of a battery that is below the low-voltage threshold (V_{EDV}). The battery voltage (V_{CELL}) is compared to the low-voltage threshold (V_{EDV}) and charge will be inhibited if $V_{CELL} < V_{EDV}$. The condition trickle current and fault time-out are a percentage of the fast charge rate and maximum time-out (MTO).

To ensure safety for the battery and system, fast charging also terminates based on a high-temperature cutoff threshold (TCO), a safety time-out, and a maximum cell voltage threshold (MCV). To avoid possible premature fast-charge termination when charging batteries after long periods of storage, the bq2007 disables PVD, and -ΔV detection during a short "hold-off" period at the start of fast charge. During the hold-off period when fast charge is selected, the bq2007 charges at the topoff rate to prevent excessive overcharging of a fully charged battery. This hold-off period is configured as described in the bq2007 data sheet.

The bq2007 may be configured to have two or three charge stages. In a two-stage configuration, the fast-charge stage controlled by the bq2007 is preceded and followed by a pulse trickle charge at a rate controlled by bq2007 input pins FAST, TM, and VSEL. In a three-stage configuration, the fast charge is followed by a "top-off" charge stage where the battery is charged at $\frac{1}{8}$ of the fast charge rate. This allows the battery to be quickly and safely brought to a full charge state. Following top-off, pulse trickle is used to compensate for self-discharge while the battery is idle. The trickle rate is $\frac{1}{64}$ for PVD and $\frac{1}{32}$ when -ΔV is enabled.

Charger Circuit Examples

Two detailed applications follow this section. One provides direct control of a switch-mode regulator, and the other provides control of an external current source.

The switching-mode constant-current regulator is used on the DV2007S1 development system. The board layout and schematic is described in the layout guidelines section.

Gating Current

Figure 1 shows an example of external gated current source. With SNS connected to V_{SS}, the bq2007 enables charge current to the battery by taking MOD high at the start of charging and maintaining this state until charging is terminated. In this example, R7, R19, R15, and Q1 and Q2 form the switching circuit. When MOD goes high, Q2 switches on—turning on Q1. When MOD goes low, the base current in Q1 is turned off and the charging path is switched off.

The current-handling capability of this circuit is limited by the product of the current gains of the transistors and by the 5mA drive capability of the MOD pin.

This limitation may be removed by replacing the PNP at Q1 with a pFET. See Table 1 for suggested transistors.

Table 1. Suggested Transistors (Q1)

Q1	Type	Package	Maximum Current	Maximum Voltage
IRFR9010	pFET	DPAK	5.3	-50
IRFR9022	pFET	DPAK	9.0	-50
IRFR9020	pFET	DPAK	9.9	-50
IRFD9014	pFET	HEXDIP	1.1	-60
IRFD9024	pFET	HEXDIP	1.6	-60
IRF9Z10	pFET	TO-220	4.7	-50
IRF9Z22	pFET	TO-220	8.9	-50
IRF9Z20	pFET	TO-220	9.7	-50
IRF9Z32	pFET	TO-220	15	-50
BD136	PNP	TO-225	1.5	-60
MJE171	PNP	TO-225	3.0	-60
TIP42A	PNP	TO-220	6.0	-60

Note: For very high currents, two parallel pFETs or an nFET with a high-side driver circuit may be suitable.

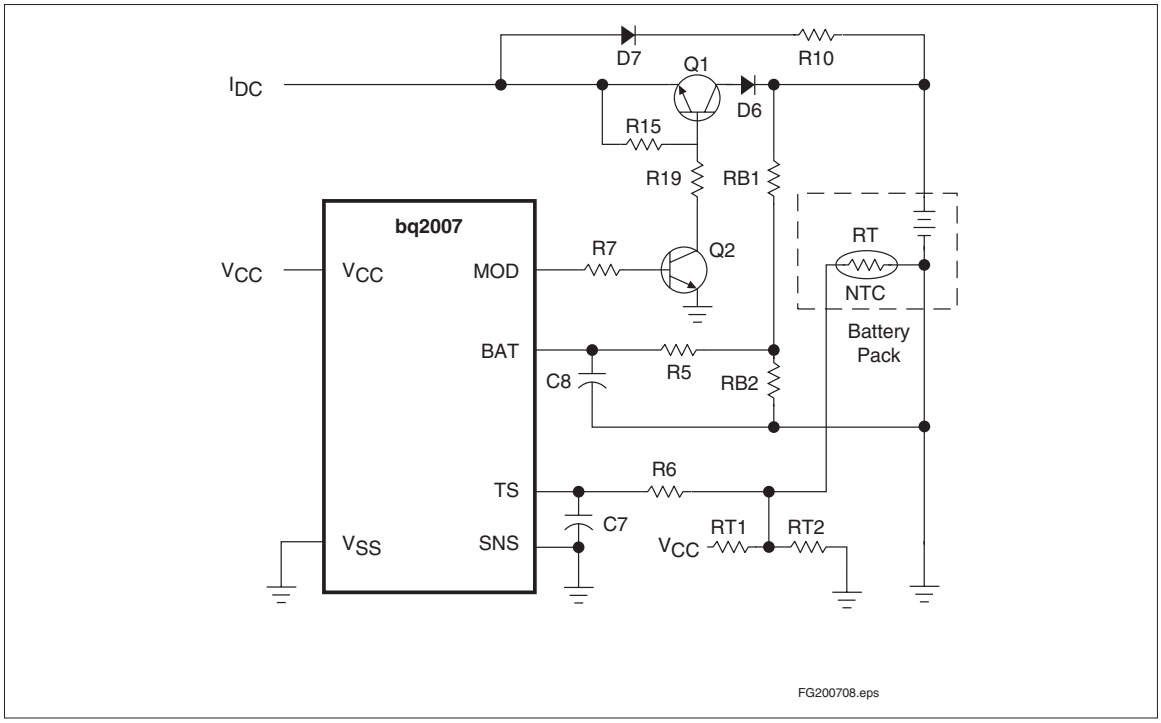

Figure 1. Gated External Source (Bipolar Switch Option)

Using the bq2007 Enhanced Features for Fast Charge

Charge Action Control

The bq2007 charge action is controlled by input pins $\overline{DCMD}$, VSEL, FAST, and TM. When charge action is initiated, the bq2007 enters the charge-pending state, checks for acceptable battery voltage and temperature, and performs any required discharge-before-charge operations. $\overline{DCMD}$ controls the discharge-before-charge function, and VSEL, FAST, and TM select the charger configuration. See Tables 4 and 5 of the bq2007 data sheet.

Charge Status Indication

Table 2 summarizes the bq2007 charge status display. The charge status indicators include the DIS output, which can be used to indicate the discharge state, the audio ALARM output, which indicates charge completion and fault conditions, and the dedicated status outputs, LED_1 and LED_2.

Outputs $LED_{1–2}$ have three display modes that are selected at initialization by the input pins $DSEL_1$ and $DSEL_2$. The $DSEL_1$ and $DSEL_2$ input pins, when pulled down to V_{SS}, are intended for implementation of a simple two-LED system, where LED_2 indicates the precharge status (i.e., charge pending and discharge) and LED_1 indicates the charge status (i.e., charging and completion). $DSEL_1$ pulled up to V_{CC} and $DSEL_2$ pulled down to V_{SS} mode is for implementation of a single tri-color LED such that discharge, charging, and completion each have a unique color. $DSEL_1$ pulled down to V_{SS} and $DSEL_2$ pulled up to V_{CC} mode allows for fault status information.

Audio Alarm Selection

The alarm output waveform is a 3.5KHz square wave signal that allows a direct connection to drive standard piezoelectric alarm elements. Piezoelectric alarm elements are designed for a maximum sound output at a specific frequency and drive voltage. The alarm element must be selected for a maximum sound output at a frequency of 3.5kHz with a 5V peak-to-peak drive signal. The PCB mount element can be connected directly to the bq2007 alarm output with a 20K isolation resistor. The design of a molded resonant cavity should follow the manufacturers recommended procedures to assure maximum sound output. Manufactures also provide several boost circuits that can be used to increase the drive voltage for increased sound output levels.

Table 2. bq2007 Charge Status Display Summary

Mode	Charge Action State	LED_1	LED_2	DIS	ALARM
$DSEL_1$ = L $DSEL_2$ = L (Mode 1)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	1	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = H $DSEL_2$ = L (Mode 2)	Battery absent	0	0	0	0
	Discharge in progress, pending	1	1	1	0
	Charging	1	0	0	0
	Charge complete	0	1	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = L $DSEL_2$ = H (Mode 3)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	Flashing	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	1	0	High tone

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

Selecting the BAT Divider for Charge Monitoring

The voltage based state of charge monitoring is enabled when charging packs with a fixed number of cells by pulling the multi-cell pack select input MULTI to V_{SS}. When MULT = 0, internal voltage thresholds are compared with the BAT pin input voltage for both charge and discharge capacity status indications. When discharge-before-charge is initiated, the state-of-charge monitor indicates the discharge condition as monotonic decreasing steps from the charged condition. The voltage charge status monitoring circuit is shown in Fig. 2. The circuit changes its voltage threshold reference divider for charge or discharge monitoring when the discharge signal is zero or one, respectively. The voltage thresholds are a fixed ratio of the V_{CC} supply voltage and are specified in the bq2007 data sheet in the section entitled "DC Thresholds." The voltage thresholds were selected based on typical NiCad and NiMH battery characteristics for a typical charge rate of 1C and a typical discharge rate of 1 Amp.

To optimize the charge status monitoring for a range of fixed-cell packs (i.e. MULTI = 1), the BAT divider should be calculated such that the highest fixed cell pack will be centered at the EDV threshold. For example, to charge packs that range from 4 to 6 fixed cells, select the BAT divider MULTI = 0. The BAT divider should be determined by BAT divider equation 2 for values shown in Table 4. To further optimize, you can fit the battery characteristics to the end points of the EDV and MCV thresholds. This will center the battery voltage charge characteristics in the center of the bq2007 charge monitoring thresholds. This is possible since the full charge detection methods (PVD, -DV) are not dependent on absolute voltage value. When adjusting the battery divider, the maximum cutoff voltage (V_{MCV}) must not be exceeded.

Charge Status Monitoring

The bq2007 charge status monitor may display the battery voltage or charge safety timer as a percentage of the full-charged condition. These options are selected with the MULT input pin.

When MULT is pulled down to V_{SS}, the battery charge status is displayed as a percentage of the battery voltage, and the single-cell battery voltage at the BAT pin is compared with internal charge voltage reference thresholds. When V_{BAT} is greater than the internal thresholds of V_{20}, V_{40}, V_{60}, or V_{80}, the respective 20%, 40%, 60%, or 80% display outputs are activated. The battery voltage directly indicates 20% charge increments, while the 10% charge

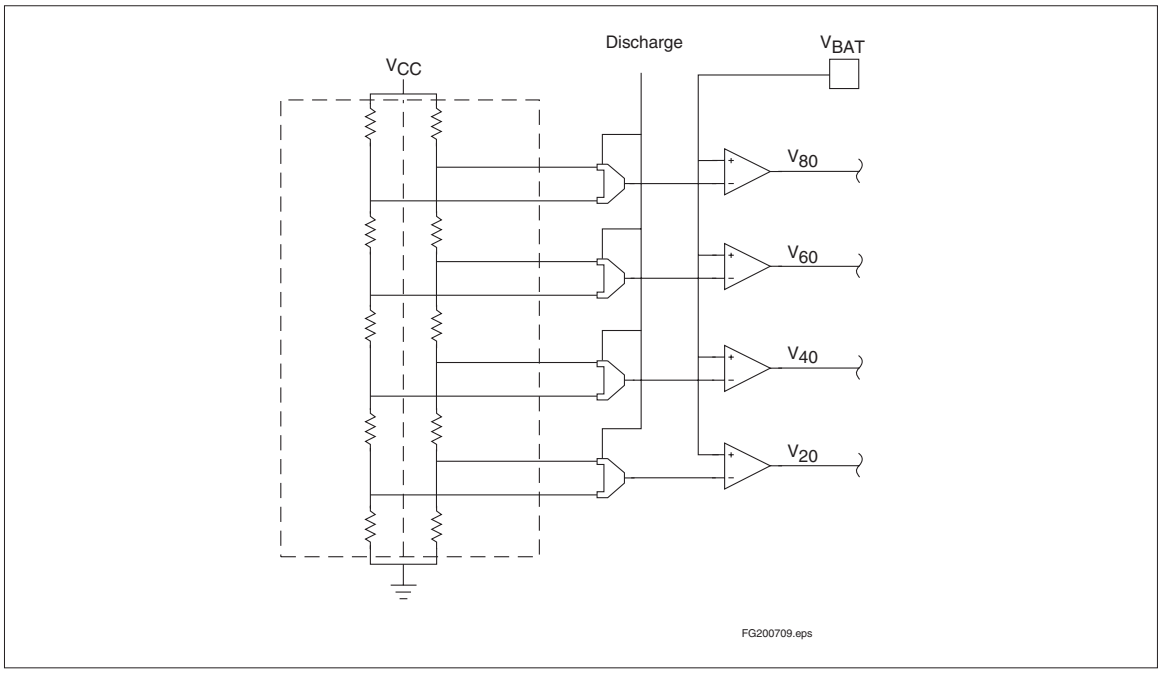

Figure 2. Voltage Charge Status Monitoring Circuit

increments use a timer that is a function of the charge safety timer.

When MULT is pulled down to V_{SS} and when V_{BAT} exceeds V_{20} during charging, the 20% charge indication is activated and the timer begins counting for a period equal to $\frac{1}{64}$ to $\frac{1}{32}$ of the charge safety time-out period. When the timer count is completed, the 30% charge indication is activated. Should V_{BAT} exceed V_{40} prior to the timer count completion, the charge status monitor activates the 30% and 40% indications. This technique is used for all the odd percentage charge indications to assure a monotonic charge status display.

When MULT is pulled up to V_{CC}, the bq2007 charge status monitor directly displays $\frac{1}{32}$ of the charge safety timer as a percentage of full charge. This method is recommended over the voltage-based method when charging multi-cell packs where the battery terminal voltages can vary greatly between packs. This method offers an accurate charge status indication when the battery is fully discharged.

During discharge with MULT pulled down to V_{SS}, the charge status monitor indicates the percentage of the battery voltage by comparing V_{BAT} to the internal discharge voltage reference thresholds. In BCD format, the discharge thresholds V80, V60, V40, and V20 correspond to a battery charge state indication of 90%, 70%, 50%, and 30%, respectively. In bargraph format, the same discharge thresholds correspond to a battery charge state indication of 90%, 60%, 40%, and 30%, respectively. Differences in the battery charge state indications are due to the finer granularity of the BCD versus the bargraph format.

During discharge and when MULT is pulled up to V_{CC}, the state-of-charge monitor segment format displays the discharge condition, letter "d," whereas the bargraph format has no indication.

The charge status display is blanked during the charge pending state and when the battery pack is removed.

Charge Status Display Modes

The bq2007 charge status monitor can be displayed in two modes summarized in Table 3. The display modes are a seven-segment monotonic bargraph or a seven-segment single-digit format. When QDSEL is pulled down to V_{SS}, pins $SEG_{A–G}$ drive the decoded seven segments of a single segment digit display, and when QDSEL is pulled up to V_{CC}, pins $SEG_{A–G}$ drive the seven segments of a bargraph display.

In the bargraph display mode, outputs $SEG_{A–G}$ allow options for a three-segment to seven-segment bargraph display. The three-segment charge status display uses outputs SEG_B, SEG_D, and SEG_F for 30%, 60%, and 90% charge indications, respectively. The four-segment charge status display uses outputs SEG_A, SEG_C, SEG_D, and SEG_E for 20%, 40%, 60%, and 80% indications, respectively. The seven-segment charge status monitor uses all segments.

The segment display mode drives pins $SEG_{A–G}$ with the decoded seven-segment single-digit information. The display indicates in 10% increments from a segment zero count at charge initiation to a segment nine count indicating 90% charge capacity. Charge completion is indicated by the letter "F," a fault condition by the letter "E," and the discharge condition by the letter "d." See Table 3.

Display Driver Modes

The bq2007 is designed to interface with LCD or LED type displays. The LED signal levels are driven when the MSEL input is pulled to V_{CC} at initialization. The output pin COM is the common anode connection for LED $SEG_{A–G}$.

The LCD interface mode is enabled when the MSEL input pin is pulled to V_{SS} at initialization. An internal oscillator generates all the timing signals required for the LCD interface. The output pin COM is the common connection for static direct-driving of the LCD display backplate and is driven with an AC signal at the frame period. When enabled, each of the $SEG_{A–G}$ pins is driven with the correct-phase AC signal to activate the LCD segment. In segment mode, output pins $SEG_{A–G}$ interface to LED or LCD segments.

Discharge Before Charge

It may be desirable in the application to allow the user to occasionally discharge the battery to a known voltage level prior to charge. The reason for this may either be to remedy a voltage-depression effect found in some NiCd batteries or to determine the battery's charge capacity.

Figure 3 illustrates the implementation of this function. Discharge-before-charge is initiated on a positive strobe signal on DCMD.

Note: This function takes precedence over a charge action and commences immediately when conditions warrant, forcing DIS to a high state until the voltage sensed on BAT falls below $V_{CC}/5$. Charging begins as soon as conditions allow.

Care should be taken not to overheat the battery during this process; excessive temperature is not a condition that terminates discharge.

Configuring the BAT Input

The bq2007 uses the battery voltage sense input on the BAT pin to control discharge-before-charge, qualify charge initiation, terminate charge at an absolute limit, facilitate peak voltage detect (PVD) and negative delta voltage (-ΔV) detection, and detect a battery replacement.

V_{BAT} may be derived from a simple resistive network across the battery. As shown in Figure 1, resistors RB1 and RB2 are chosen to divide the battery voltage down to the optimal detection range. When MULT is pulled up to V_{CC}, battery voltage is sensed at the BAT pin by a resistive voltage divider that divides the terminal voltage between 0.262 ∗ V_{CC} (V_{EDV}) and 0.8 ∗ V_{CC} (V_{MCV}). The bq2007 charges multi-cell battery packs from a minimum of N cells, to a maximum of 1.5 ∗ N cells. The battery voltage divider is set to the minimum cell battery pack (N) by the BAT pin voltage divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{1.33}\right) - 1 \qquad \text{Equation 1}$$

When MULT is pulled down to V_{SS}, tighter charge voltage limits and voltage-based charge status display are selected. This is recommended for charging packs with a fixed number of cells where the battery voltage divider range is between 0.4 ∗ V_{CC} (V_{EDV}) and 0.8 ∗ V_{CC} (V_{MCV}). The bq2007 charges fixed-cell battery packs of N cells. The battery voltage divider is set by the divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{2}\right) - 1 \qquad \text{Equation 2}$$

Although virtually any value may be chosen for RB1 and RB2 due to the high input impedance of the BAT pin, the values selected must not be so low as to appreciably drain the battery nor so large as to degrade the circuit's noise performance. Constraining the source resistance as seen from BAT between 20KΩ and 1MΩ is acceptable over the bq2007 operating range. Total impedance between the battery terminal and VSS should typically be about 300KΩ to 1MΩ . See Table 4.

Note: Because V_{SNS} may be positive in bq2007 switching regulation applications, the actual internal comparison

Table 3. bq2007 Charge Status Display Summary

Mode	Display Indication	SEG_A	SEG_B	SEG_C	SEG_D	SEG_E	SEG_F	SEG_G
QDSEL = H	20% charge	1	0	0	0	0	0	0
	30% charge	1	1	0	0	0	0	0
	40% charge	1	1	1	0	0	0	0
	60% charge	1	1	1	1	0	0	0
	80% charge	1	1	1	1	1	0	0
	90% charge	1	1	1	1	1	1	0
	Charge complete	1	1	1	1	1	1	1
QDSEL = L	0% charge—digit 0	1	1	1	1	1	1	0
	10% charge—digit 1	0	1	1	0	0	0	0
	20% charge—digit 2	1	1	0	1	1	0	1
	30% charge—digit 3	1	1	1	1	0	0	1
	40% charge—digit 4	0	1	1	0	0	1	1
	50% charge—digit 5	1	0	1	1	0	1	1
	60% charge—digit 6	1	0	1	1	1	1	1
	70% charge—digit 7	1	1	1	0	0	1	0
	80% charge—digit 8	1	1	1	1	1	1	1
	90% charge—digit 9	1	1	1	1	0	1	1
	Charge complete—letter F	1	0	0	0	1	1	1
	Fault condition—letter E	1	0	0	1	1	1	1
	Discharge—letter d	0	1	1	1	1	0	1

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

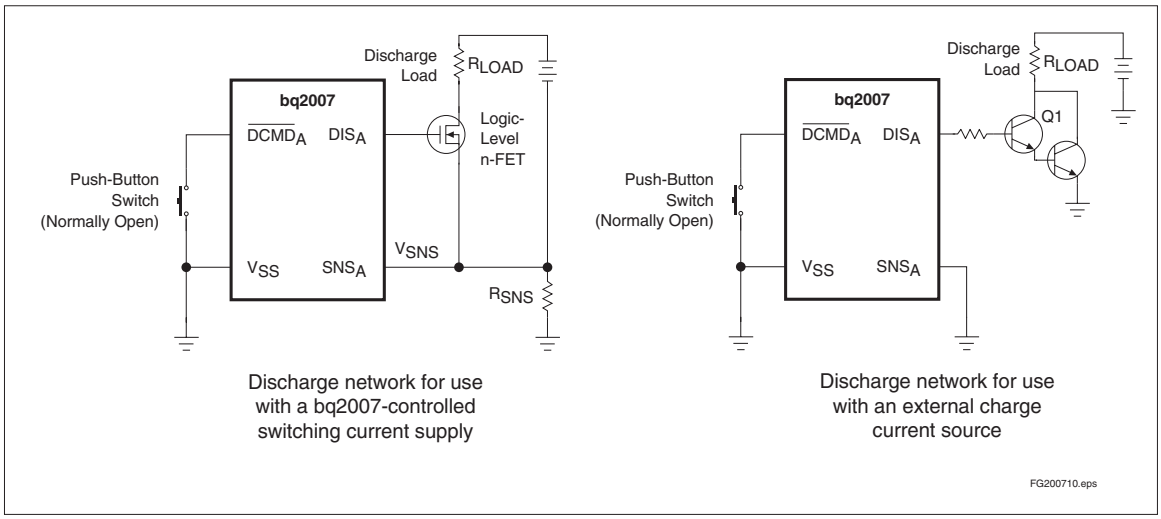

Figure 3. Battery Conditioning Network

Table 4. Suggested RB1 and RB2 Values for NiCd and NiMH Cells

Number of Cells (V_{BAT} Divisor)	RB1(KΩ)	RB2(KΩ)
4	150	165
5	150	110
6	150	80.6
8	150	53.6
10	150	40.2

Note: MULTI = 0; RB1/RB2 = (N/2) - 1.

uses $V_{BAT} - V_{SNS}$, or V_{CELL}. This internal value V_{CELL} maintains a representative voltage independent of any current through R_{SNS}.

Temperature Sensing and the TCO Pin

The bq2007 uses the temperature sense input on the TS pin to qualify charge initiation and termination. A negative temperature coefficient (NTC) thermistor referenced to SNS and placed in close proximity to the battery may be used as a temperature-to-voltage transducer as shown in Figure 1. This example shows a simple linearization network constituted by RT1 and RT2 in conjunction with the thermistor, RT.

Temperature-decision thresholds are defined as LTF (low-temperature fault) and TCO (temperature cutoff). Charge action initiation is inhibited if the temperature is not within the LTF-to-TCO range. In this case, the charge pending state is active on the charge status display (see Table 2), and charging does not initiate until the battery temperature returns to this range.

Once initiated, charging terminates if the temperature is either less than LTF or greater than TCO. The bq2007 interprets the reference points V_{LTF} and V_{TCO} as V_{SS}-referenced voltages, with V_{LTF} fixed at ½ V_{CC} and V_{TCO} equal to the voltage presented on the TCO pin. See Figure 4. Note that since the voltage on pin TS decreases as temperature increases, V_{TCO} should always be less than ½ V_{CC}. The resistive dividers may be used to generate the desired V_{TCO}.

VCC Supply

The V_{CC} supply provides both power and voltage reference to the bq2007. This reference directly affects BAT voltage and internal time-base voltage measurements.

The time-base is trimmed during manufacturing to within 5 percent of the typical value with V_{CC} = 5V. The oscillator varies directly with V_{CC}. If, for example, a 5% regulator supplies V_{CC}, the time-base could be in error by as much as 10%.

Charge State Actions

Once the required discharge is completed and temperature and voltage prequalifications are met, the charge state is initiated. The charge state is configured by the VSEL, FAST, and TM input pins. The FAST input selects between Fast and Standard charge rates. The Standard

Table 5. bq2007 Charge Action Control Summary

FAST Input State	TM Input State	Time-out Period (min)	MOD Duty Cycle	Hold-off period (sec)	Trickle Rep Rate -ΔV /32	Trickle Rep Rate PVD /64
V_{SS}	Float	640 (/8)	25%	2400	219Hz	109Hz
V_{SS}	V_{SS}	320 (/4)	25%	1200	109Hz	55Hz
V_{SS}	V_{CC}	160 (/2)	25%	600	55Hz	27Hz
V_{CC}	Float	160 (/2)	100%	600	219Hz	109Hz
V_{CC}	V_{SS}	80 (C)	100%	300	109Hz	55Hz
V_{CC}	V_{CC}	40 (2C)	100%	150	55Hz	27Hz

charge rate is ¼ of the Fast charge rate, which is accomplished by disabling the regulator for a period of 286µs of every 1144µs (25% duty cycle). In addition to throttling back the charge current, time-out and hold-off safety time are increased accordingly.

The VSEL input selects the voltage termination method. The termination mode sets the top-off state and trickle charge current rates. The TM input selects the Fast charge rate, the Standard rate, and the corresponding charge times. Once charging begins at the Fast or Standard rate, it continues until terminated by any of the following conditions:

- Negative delta voltage (-ΔV)

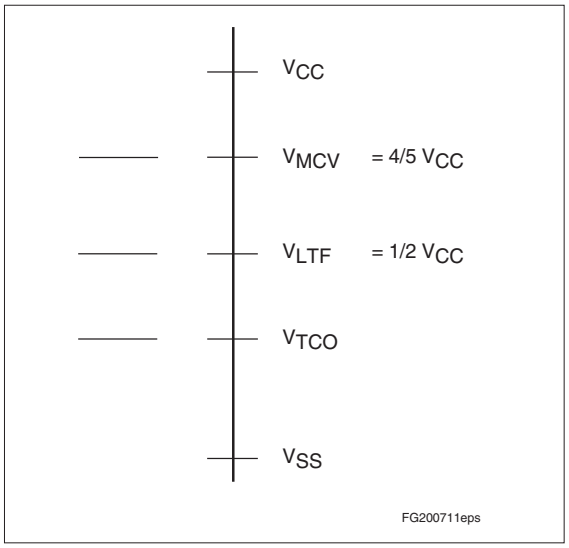

Figure 4. Temperature Reference Points

- Peak voltage detect (PVD)
- Maximum temperature cutoff (TCO)
- Maximum time-out (MTO)
- Maximum cutoff voltage (MCV)

Voltage Termination Hold-off

To prevent early termination due to an initial false peak battery voltage, the -ΔV and PVD terminations are disabled during a short "hold-off" period at the start of charge. During the hold-off period when fast charge is selected (FAST = 1), the bq2007 will top off charge to prevent excessive overcharging of a fully charged battery. Once past the initial charge hold-off time, the termination is enabled. TCO and MCV terminations are not affected by the hold-off time.

-ΔV or PVD Termination

Table 6 summarizes the two modes for full-charge voltage termination detection. When VSEL = V_{SS}, negative delta voltage detection occurs when the voltage seen on the BAT pin falls 12mV (typical) below the maximum sampled value. VSEL = V_{CC} selects peak voltage detect termination and the top-off charge state. When charging a battery pack with a fixed number of cells, the -ΔV and PVD termination thresholds are -6mV and 0 to -3mV per cell, respectively. The valid battery voltage range on V_{BAT} for -ΔV or PVD termination is from $0.262 * V_{CC}$ to $0.8 * V_{CC}$.

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Top-Off Charge

The top-off charge option allows for the self-discharge replacement trickle current to be very low, but still provides for filling up the last fraction of capacity after the fast-charge phase has terminated. Top-off occurs at $\frac{1}{8}$ of the fast charge rate to prevent excess heat generation, and terminates after a period equal to the safety time-out. It also terminates if TCO or MCV is detected.

Top-off is not recommended in applications where a battery charge is re-initiated with extremely high frequency (many times per day); for example, when the unit is returned to the charge cradle after each short period of use.

Pulse trickle is used to compensate for self-discharge while the battery is idle and to condition a depleted low-voltage battery to a valid voltage prior to high-current charging. The battery is pulse trickle charged when Fast, Standard, or top-off charge is not active. This results in a trickle rate of $\frac{1}{64}$ for PVD and $\frac{1}{32}$ when -ΔV is enabled.

Table 6. VSEL Configuration

VSEL	Detection Method	Top-Off	Pulse Trickle Rate
V_{SS}	-ΔV	Disabled	$\frac{1}{32}$
V_{CC}	PVD	Enabled	$\frac{1}{64}$

Charge Inhibit

Fast charge, top-off, and pulse trickle may be inhibited by using the $\overline{INH}$ input pin. When low, the bq2007 suspends all charge activity, drives all outputs to high impedance, and assumes a low-power operational state. When $\overline{INH}$ returns high, a fast-charge cycle is qualified and begins as soon as conditions allow.

Power Supply Selection

The DC supply voltage, V_{DC}, must satisfy two requirements:

1. To support the bq2007 V_{CC} supply, V_{DC} must be adequate to provide for 5V regulation after the losses in the regulator and across D1 ($V_{DC} \geq 7.7V$ using the 78L05).
2. To support the charge operation, V_{DC} > (number of cells * MCV_{MAX}) + V_{LOSS} in the charging path. (MCV_{MAX} is the maximum cell voltage threshold with the maximum bq2007 V_{CC}.)

Polarity Reversal Protection

If the DC input has any risk of being accidentally connected with power (+) and ground (–) reversed, then the system input should include either a protection diode to protect against circuit damage or a diode bridge to provide both protection and operation. This also increases minimum input voltage for charger operation by approximately 1V to 2V.

Layout Guidelines

PCB layout to minimize the impact of system noise on the bq2007 is important when the bq2007 is used as a switching modulator, with a separate nearby switching regulator, or close to any other significant noise source.

1. Avoid mixing signal and power grounds by using a single-point ground technique incorporating both a small signal ground path and a power ground path.
2. The charging path components and associated traces should be kept relatively isolated from the bq2007 and its supporting components.
3. 0.1µF and 10µF decoupling capacitors should be placed close together and very close to the V_{CC} pin.
4. 0.1µF capacitors and resistors forming R-C filters connected to pins BAT, TS, TCO, and MCV should be as close as possible to their associated pins.
5. Because the bq2007 uses V_{CC} for its reference, additional loading on V_{CC} is not recommended.
6. Diode D1 (1N4148) is recommended for rectification and filtering.
7. If the DCMD input is electronically controlled, care should be taken to prevent noise-induced false transitions.
8. For bq2007-modulated switching applications:
   - A 2KΩ resistor is required between the MOD pin and the transistor.
   - A 1000pF capacitor/1KΩ resistor R-C filter should be as close as possible to the SNS pin.
   - The 0.1µF capacitors for BAT and TS should be routed directly to SNS and not to ground.

Figures 6, 7, and 8 show an example layout of the DV2007S1 Development Board. Figure 9 is a schematic of the board. Table 7 contains the parts list for the board. A comparable layout is recommended.

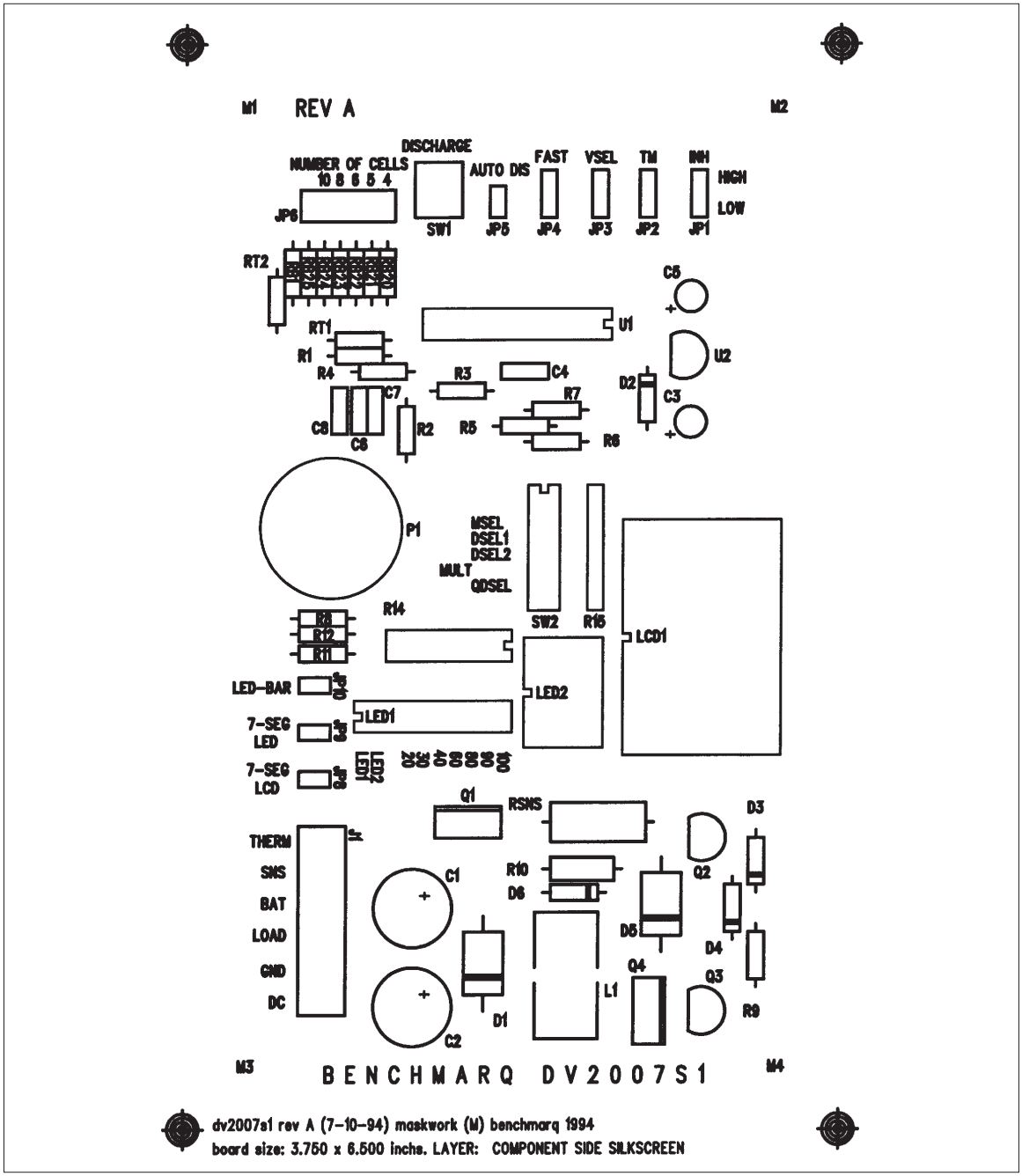

Figure 6. DV2007S1 Development Board Layout Component Placement

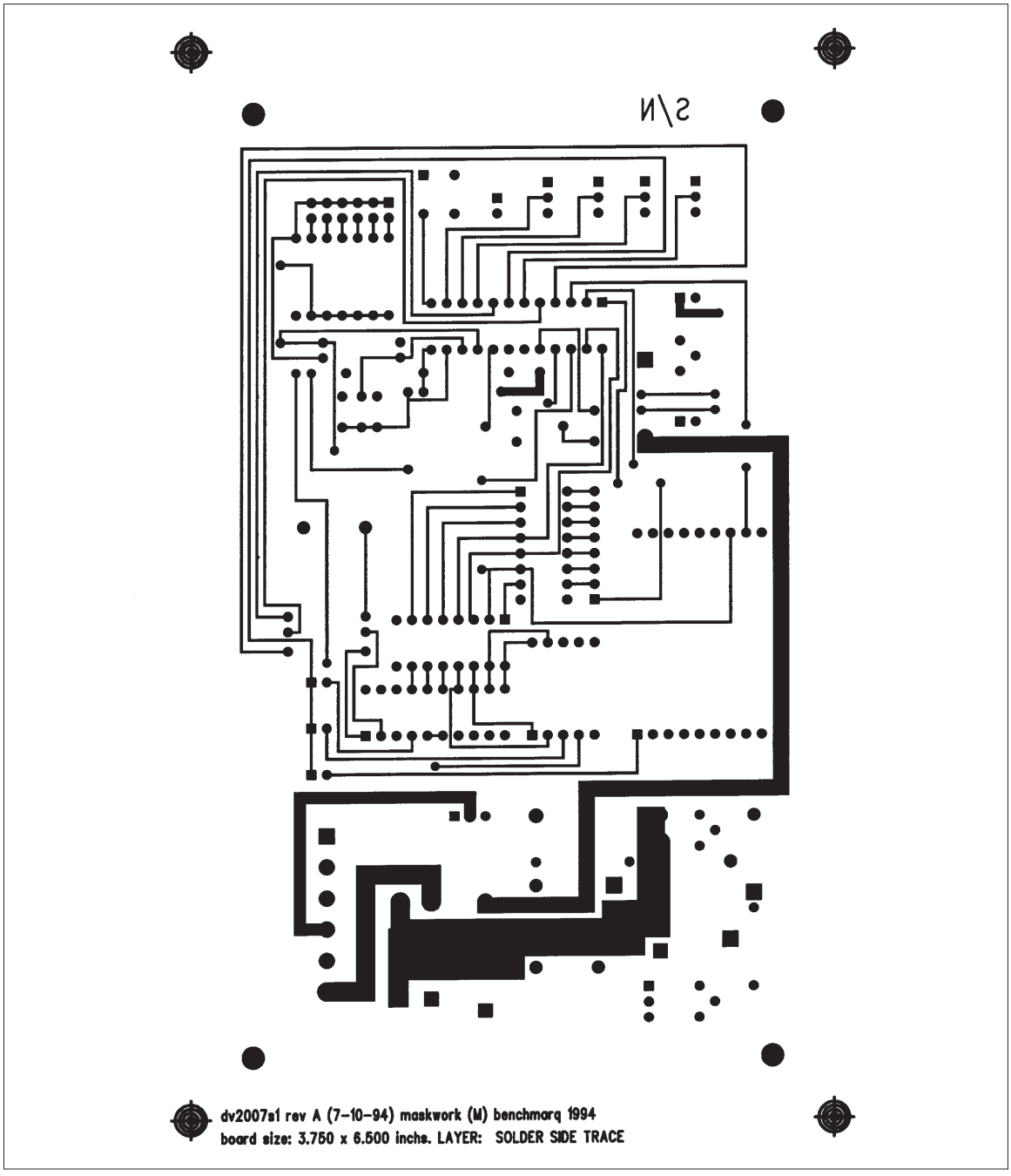

Figure 7. DV2007S1 Development Board Layout

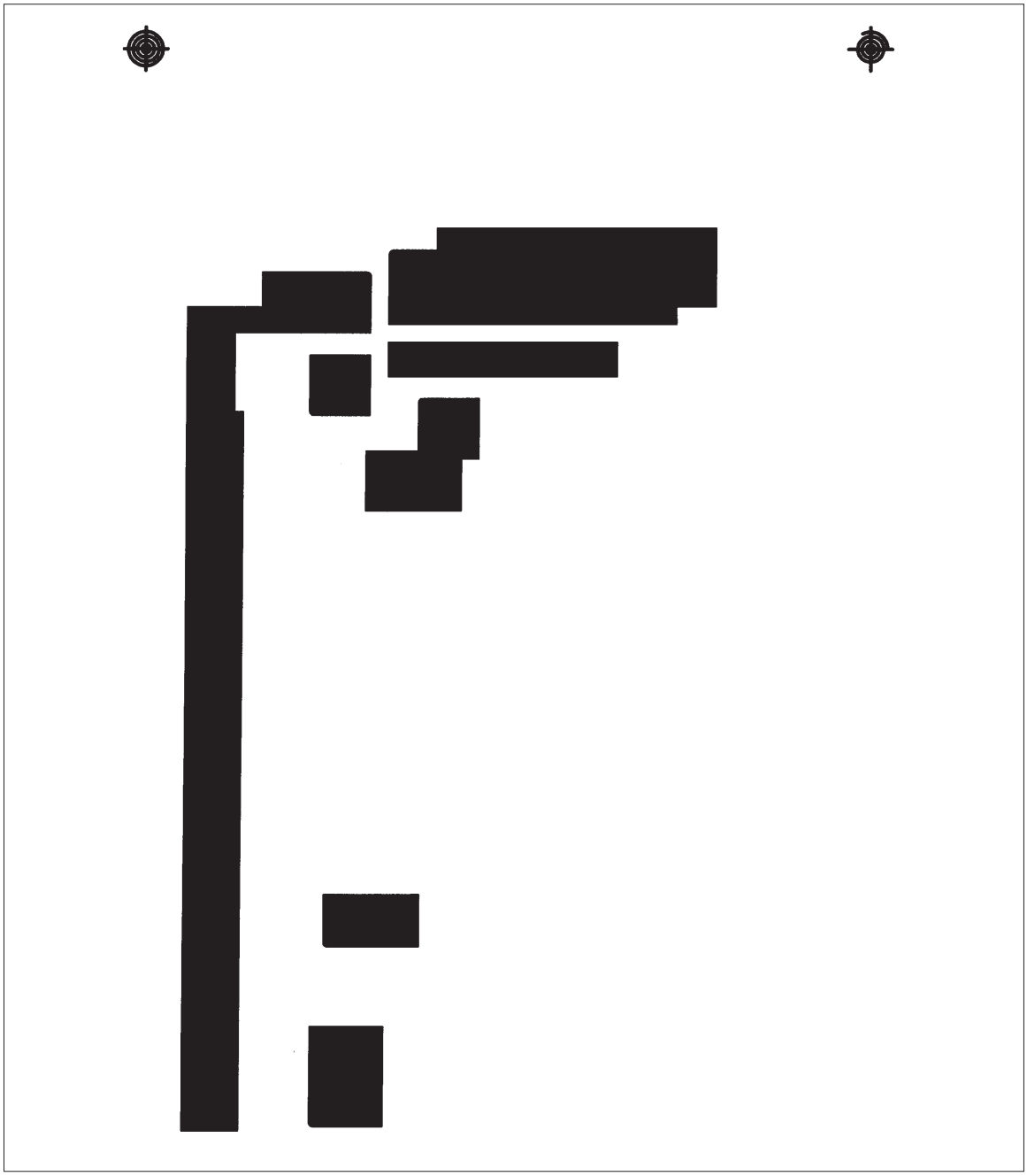

Figure 8. DV2007S1 Development Board Layout

Table 7. DV2007S1 Development Board Parts List

Component Name	Component Description
C2, C1– Optional	1000µF
C5, C3	100µF
C4, C6, C7	0.1µF
C8	1nF
D1	1N5400
D4, D2	1N4148
D3	1N751A
D5	1N5821
D6	1N4001
JP1, JP2, JP3, JP4	HEADER 3
JP5, JP8, JP9, JP10	HEADER 2
J1	CON6
LCD1	7-SEG LED
LED1	LED BAR
LED2	7-SEG LCD
L1	100µH
P1	BUZZER
Q1	MTP3055EL
Q2	2N7000
Q3	2N3904
Q4	MTP23P06E
R14	Resistor 8pack
RB1	150K
RB2X	User Selected
RSNS	0.2
RT1	20K
RT2	Open
R1	300K
R6, R7	100K
R2, R5, R10	2K
R3	82K
R4	20K
R8	20K
R9	6.8K
R12, R11	510
SR	SIP8
SW1	SW pushbutton
SW2	SW DIP-8
U1	bq2007
U2	78L05

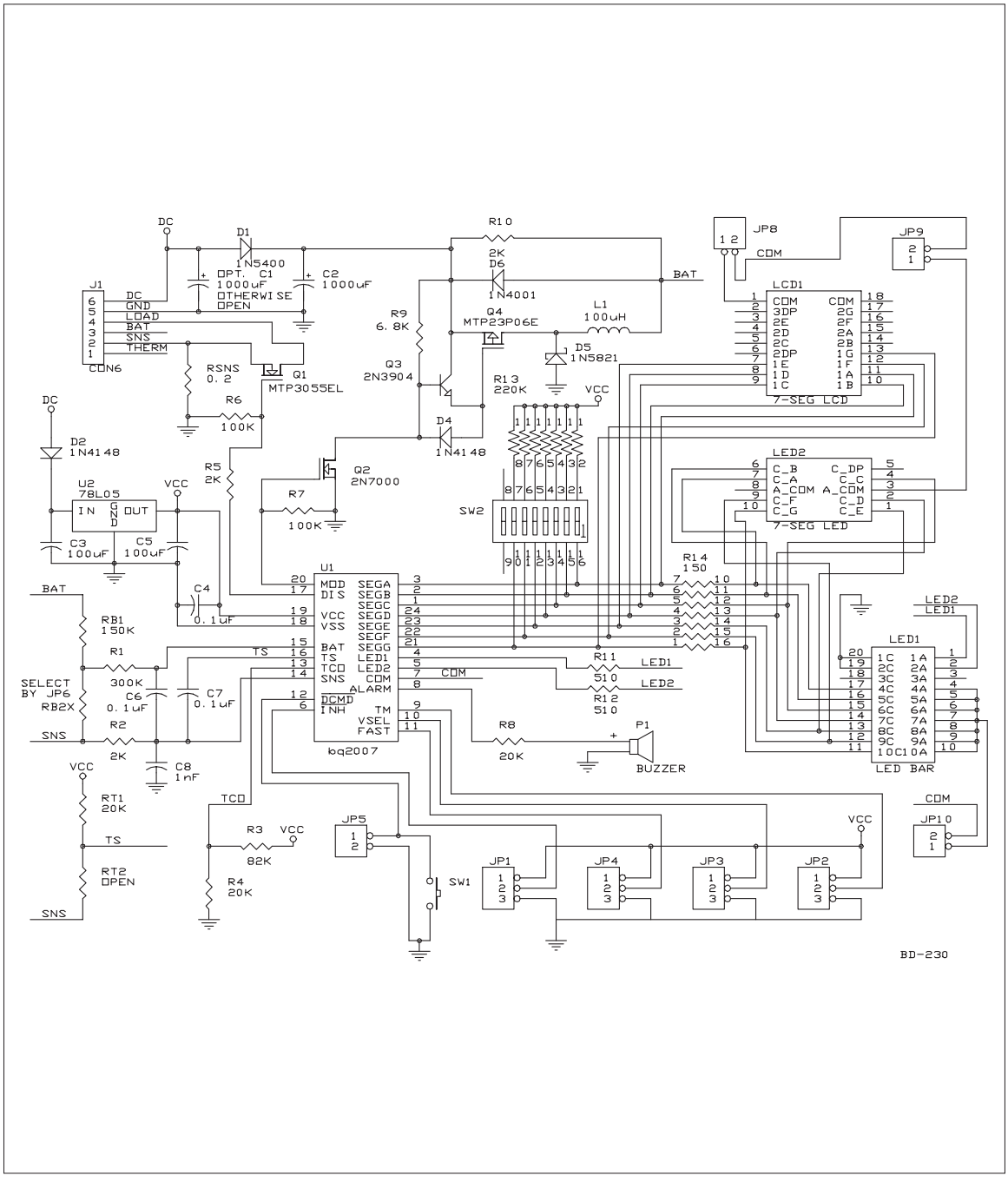

Figure 9. DV2007S1 Development Board Schematic

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