# 16-Bit 8-Channel PLC Analog Input Module With High-Voltage (±150 V) Common-Mode Support

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Supporting high-voltage common mode in programmable logic controller (PLC) analog input modules is achieved using different techniques. Using a difference amplifier at the input offers a very wide common-mode range and differential to single-ended conversion with a typical bipolar supply like ±15 V.

This article explores the performance of analog input modules when an integrated difference amplifier is used to add high-voltage common mode (HVCM) support.

The ADS868x family of ADCs are ideal candidates for PLC analog input module applications with high-speed sampling up to 500 ksps, integrated multiplexer, and an input buffer that accepts a standard ±10-V voltage input. Adding the INA148 difference amplifier to the ADC input as in Figure 2 extends the common-mode voltage range to ±200 V without degrading differential input performance.

Any mismatch of resistor dividers around the difference amplifier would result in degraded common-mode rejection. The INA148 device overcomes this issue by integrating high-precision trimmed resistors.

To validate performance of that proposed solution, a high-voltage analog front-end (AFE) prototype board is developed as Figure 1 shows. The prototype board has eight HVCM channels, power stage, and is designed to connect directly to the ADS8688A EVM board.

Figure 1 shows an onboard power circuit supporting a 24-V non-isolated supply. Other supply options like an isolated 24-V supply might be added through daughterboard connectors. The step-down converter, TPS560430, converts the wide input voltage level to 5.3-V intermediate voltage. The split-rail converter, TPS65130, produces the dual ±15-V outputs to power the eight-channel high-voltage buffers. The LDO TLV760 and LP2985 provide respectively, the 3.3-V DVDD and 5-V AVDD required for the ADS8688AEVM.

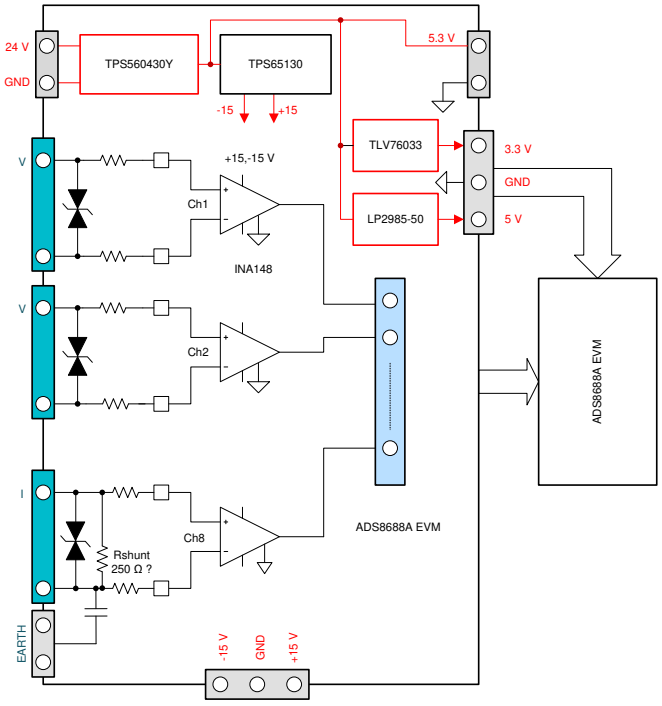


**Figure 1. Eight-Channel HVCM Front-End Board**

As Figure 2 shows, the interface circuit includes a flat-clamp surge-protection device TVS3301, followed by a couple of high-voltage (160 V) TVS diodes to protect against common-mode surge events.

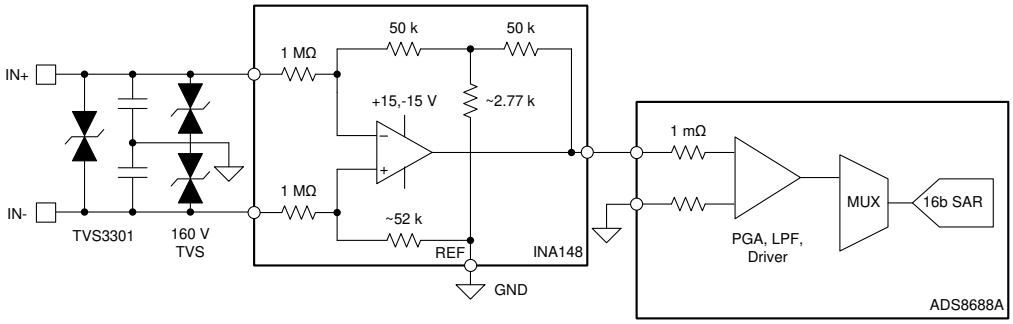


**Figure 2. High-Voltage Common-Mode Block Diagram**

## Test Setup

A prototype board of the described circuit was built and put under test using various test setups.

Offset voltage and total front-end noise is tested as Figure 3 shows. In this test, zero volt input is provided to each channel. Histogram analysis, mean and standard deviation captured by the ADS8688AEVM software are used to estimate the offset and total output noise of each channel.

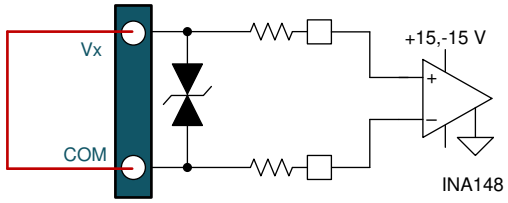


**Figure 3. Offset Voltage and Total Front-End Noise Test**

Common-mode rejection is tested as Figure 4 shows. Zero volt input is provided to each channel, in addition to this a common-mode voltage of ±20-V, 1-kHz sine wave is injected to both positive and negative inputs.

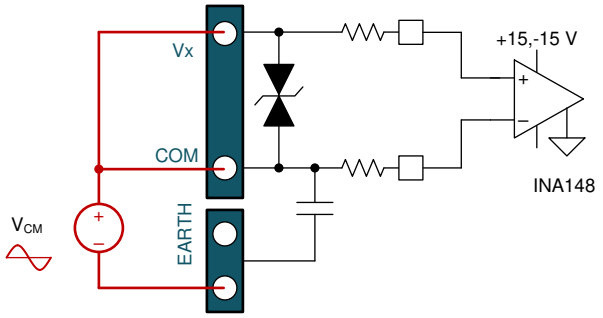


**Figure 4. Common-Mode Rejection Test**

Spectrum analysis and time histogram analysis captured by ADS8688AEVM software can be used to calculate the common-mode rejection after removing the noise calculated in the first test.

## Test Results

Table 1 lists a summary of the test results.

The test results show that, compared to the ADS8688AEVM alone, an EVM with an AFE board attached achieves pretty high common-mode voltage support with minor effect on the performance.

Throughout the tests, the ADS8688A sampling rate was set to a maximum of 500 kSPS, that is, conversion time per channel is 2 µs and scan time for all 8 channels is 16 µs.

**Table 1. Performance Test Results**

| Parameter | ADS8688AEVM | AFE + ADS868AEVM |
|---|---|---|
| Number of channels | 8 | 8 |
| Resolution | 16 bits | 16 bits |
| Conversion time per channel | 2 µs | 2 µs |
| Input Impedance | Not applicable | 2 MΩ (Differential)<br>1 MΩ (Common) |
| Differential Input Voltage Range | Not supported | ±10.24 V |
| Common Input Voltage Range | ±10.24 V | ±150 V |
| Offset Error | ±1 mV | –1.6 to 1.7 mV |
| Offset Error with Common Mode | Not applicable | –1.8 to 2.2 mV ($V_{CM}$ = ±10 V)<br>–1.6 to 2.4 mV ($V_{CM}$ = ±20 V) |
| Gain Error | ±0.05 %FSR | –0.04 to 0.06 %FSR |
| Gain Error with Common Mode | Not applicable | –0.05 to 0.06 %FSR ($V_{CM}$ = ±10 V) |
| SNR | 92.5 dB | 90 dB |
| SNR with Common Mode | Not applicable | 90 dB ($V_{CM}$ = ±10 V) |
| Small Signal Bandwidth | 15 kHz | 13.1 kHz |
| Settling Time (1-V step to 0.01%) | 750 µs | 2.2 ms |
| Common Mode Rejection | Not applicable | 80.6 dB (86 dB for INA148) |
| Cross Talk | 110 dB | < 86 dB |
| 3rd Harmonic Distortion (20 $V_{PP}$ at 1 kHz) | –110 dB | < –89 dB |

Table 1 shows that adding common-mode voltage has little effect on offset error and on gain error. *Total Output Noise RMS* with common-mode change increases just 0.2 dB. The *3rd Harmonic Distortion* with AFE stays in low level –89 dB.

To summarize, adding INA148 at the ADC input increases the CMVR to ±150 V with 80.6 dB CMRR, decreases the differential input impedance to 2 MΩ, decreases the SNR by 2.5 dB, and has minor effect on other relevant parameters even in presence of non-zero common mode. This represents a reliable and simple solution to add HVCM support to typical PLC analog input modules.

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