Application Report
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TUSB4020BI Schematic Checklist

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ABSTRACT

This application report for TUSB4020BI, a USB hub device that provides one upstream port and two USB2.0 High speed downstream ports in compliance with the Universal Serial Bus (USB) specification. TUSB4020BI is implemented with a digital state machine requiring no firmware programming. This device has the ability to be configured via pin strap, I2C, and SMBus communication. This schematic checklist provides a brief explanation of each device pin and the recommended configuration of the device pin for default operation. Use this information to check the connectivity for each TUSB4020BI on a system schematic.

This document is intended to aid design at the system level for general applications but should not be the only resource used. In addition to this list, customers are advised to use the information in the TUSB4020BI datasheet, TUSB4020BPHPEVM User's Guide and associated documents to gain a full understanding of device functionality.

NOTE: TUSB4020BI has many configurations; this schematic checklist will cover a USB Hub that is configured with no external EEPROM with downstream power switching and overcurrent reporting.

Trademarks

1 TUSB4020BI Schematic Checklist

Table 1. Schematic Checklist

Pin Name	Pin Number(s)	Pin Description	Recommendation	Additional Pin Considerations
Power Pins				
VDD33	7, 13, 23, 25, 33, 37, 40, 48	3.3 V Positive Power Supply	0.1 uF decoupling capacitors on each VDD33 pin to GND. One 10 uF bulk capacitor from VDD33 to GND.	VDD33 and VDD should have a ramp time of 0.2 ms to 100 ms. VDD33 and VDD have ramp order only when using a passive reset.
VDD	1, 12, 18, 30, 34, 45	1.1 V Positive Power Supply	0.1 uF decoupling capacitors on each VDD pin to GND. One 10 uF bulk capacitor from VDD to GND.	
GND	PAD	Ground	Connected to PCB Ground.	Ensure thermal pad has ample solder for stable connection to ground.
I2C/SMBUS Pins				
SCL / SMBCLK	2	EEPROM Serial Clock	Leave Unconnected. If EEPROM is used, connect a 2-kΩ pull-up resistor to VDD33 and to SCL pin of external EEPROM.	The external interface is enabled when both the SCL/SMBCLK and SDA/SMBDAT terminals are pulled up to 3.3 V at the deassertion of reset. When used, EEPROM overwrites all the pin configurations.
SDA / SMBAT	3	EEPROM Serial Data.	Leave Unconnected. If EEPROM is used, connect a 2-kΩ pull-up resistor to VDD33 and to SDA pin of external EEPROM.	

Table 1. Schematic Checklist (continued)

Pin Name	Pin Number(s)	Pin Description	Recommendation	Additional Pin Considerations
Configuration and Miscellaneous Pins				
SMBUSz	22	I2C or SMBUS mode Select Pin .	Connect a 4.7-kΩ pull-up resistor to VDD33 or leave NC to use internal pull-up resistor for no EEPROM implementation. This indicates TUSB4020BI is I2C Master and will read the external EEPROM for configuration settings.	These settings are configured during reset. Do not tie directly to supply but instead pull-up or pull-down using external resistor. Values read from EERPROM override pin values seen during reset.
PWRCTL_POL	21	Power control polarity. Controls behavior of PWRCTL pins.	Connect a 4.7-kΩ pull-down resistor to GND or leave NC to use internal pull-up resistor. This indicates active high polarity for the PWRCTL pins on the downstream ports.	
GANGED / SMBA2 / HS_UP	35	Ganged Operation Enable / SMBus address bit 2 / Upstream Port High-Speed Status Indicator	Connect a 4.7-kΩ pull-down resistor to GND or leave NC to use internal pull-down resistor indicating individual power control supported when power switching is enabled. If SMBUSz = 0, SMBUS slave address is '1000 10yz' in combination with the y equal to the FullPWRMGMTz / SMBA1 pin and z equal to the read/write bit, when GRSTz is deasserted.	These settings are configured during reset and after reset this pin becomes an output and indicates high-speed USB connection status of the upstream port (Output active when enabled via device registers). Values read from EERPROM override pin values seen during reset.
FullPWRMGMTz / SMBA1	36	Full Power Management Enable / SMBus Address bit 1.	Connect a 4.7-kΩ pull-down resistor to GND or leave NC to use internal pull-down resistor indicating power switching is supported by downstream ports. If SMBUSz = 0, SMBUS slave address is '1000 1x0z' in combination with the x equal to the GANGED / SMBA2 / HS_UP pin and z equal to the read / write bit, when GRSTz is deasserted.	These settings are configured during reset. Do not tie directly to supply but instead pull-up or pull-down using external resistor. Values read from EERPROM override pin values seen during reset.
XI	38	Crystal Clock Input.	Connect 24-MHz crystal input. When using a crystal a 1-MΩ feedback resistor is required between XI and XO. This pin may also be driven by an external oscillator.	See TUSB4020BI Datasheet sections 8.3.4, 8.3.5, 8.3.6 for more information.
XO	39	Crystal Clock Output	Connect 24-MHz crystal output. When using a crystal a 1-MΩ feedback resistor is required between XI and XO. If XI is driven by an external oscillator this pin may be left unconnected.	
GRSTz	11	Device Active Low Reset.	For passive reset, connect 1uF capacitor and VDD must be stable before VDD33. For active reset, VDD33 must be stable before the VDD11 supply and meet the 3ms power-up delay. Counting from both power supplies being stable to the de-assertion of GRSTz.	See TUSB4020BI datasheet section 7.6 and 8.3.7 for more information on reset.
TEST	10	TEST mode enable.	Connect a 4.7-kΩ pull-down resistor to GND.	
RSVD	16, 17, 19, 20, 28, 29, 31, 32, 43, 44, 46, 47	Reserved Pin.	Leave Floating.	
Upstream Facing Port				
USB_DP_UP	26	Upstream or Root Differential Pair for USB High Speed Communication.	Connect DM0 and DP0 to D- and D+, respectively, to USB host or upstream facing USB Connector.	
USB_DM_UP	27			
USB_R1	24	Precision resistor reference.	Connect 9.53-kΩ ±1% resistor between USB_R1 and GND.	
USB_VBUS	9	USB upstream port power monitor, Vbus Detection.	Connect resistor divider using a 90.9-kΩ ±1% pull-up resistor to Vbus and a 10-kΩ ±1% pull-down resistor to GND.	Resistor divider values may change with Vbus to keep voltage seen by USB_VBUS inside 0V to 1.155 V range. (See TUSB4020BI Datasheet section 7.3 Recommended Operating Conditions)

Table 1. Schematic Checklist (continued)

Pin Name	Pin Number(s)	Pin Description	Recommendation	Additional Pin Considerations
Downstream Facing Port [2:1]				
USB_DP_DN[2:1]	14, 41	Downstream Differential Pair for USB High Speed Port.	Connect DM[2:1] and DP[2:1] to D- and D+, respectively, to downstream facing USB connector.	If downstream port is unused, leave unconnected. No additional termination needed.
USB_DM_DN[2:1]	15, 42			If downstream port is unused, leave unconnected. No additional termination needed.
OVRCUR[2:1]z	5, 8	Indicates overcurrent event on downstream Port [4:1].	Connect to overcurrent indicator on power switch for downstream port [2:1] to allow overcurrent reporting to USB host.	If downstream port is unused, pull pin high with 4.7-kΩ pull up resistor to VD33. Overcurrentreporting required for USB-IF Compliance.
PWRCTL[2:1] /BATEN[2:1]	4, 6	Port 1 power control signals.	Connect to power switch EN pin to allow USB host control of downstream port power and protection in overcurrent event.	If downstream port is unused, leave unconnected.
Notes: Routing through ESD or common mode choke before receptacle is allowed and recommended. ESD protection should be placed as close as possible to the USB connectors. Common mode chokes should be placed between the USB hub and the ESD protection. Verify the pinout of the USB connectors. Verify pin-out of TUSB4020BI matches TUSB4020BI Datasheet. Always refer to the TUSB4020BI Datasheet of this device for complete descriptions of each pin. For USB compliant applications overcurrent events on downstream ports must be reported to the USB host.				

2 References

- TUSB4020BI Two-Port USB 3.0 Hub, Datasheet
- TUSB4020BPHPEVM Evaluation Module

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