Application Report
SLLA301C–August 2010–Revised February 2011

TUSB9260 Implementation Guide

Lee Myers — *Computer Connectivity Solutions*

ABSTRACT

This document is provided to assist platform designers in implementing the TUSB9260 USB 3.0 to Serial ATA Bridge Controller. Detailed information can be found in the TUSB9260 Data Manual (SLLS962). This document provides board design recommendations for the various device features when designing in the TUSB9260.

This document is intended for developers familiar with high-speed PCB design and layout. Knowledge of the USB 3.0 and SATA specifications and protocol is required as well. The following layout recommendations should not be considered the sole method of implementation, but rather as a guide. The preferences of the individual developer, requirements of the design, number of components in the circuit, as well as many other factors will influence each individual layout.

Contents

List of Figures

List of Tables

1 TUSB9260 Typical System Implementation

Figure 1 represents a typical implementation of the TUSB9260 USB 3.0 to Serial ATA Bridge. The device serves as a bridge between a downstream USB 3.0 host port and a SATA device such as a hard disk drive. A crystal or oscillator supplies the required clock source. A SPI Flash device contains the firmware that is loaded into the TUSB9260 after the de-assertion of RESET. Push buttons or any other desired logic can be connected to the TUSB9260 GPIO terminals. The TUSB9260 can also output a pulse width modulated signal that can be used to drive an activity LED.

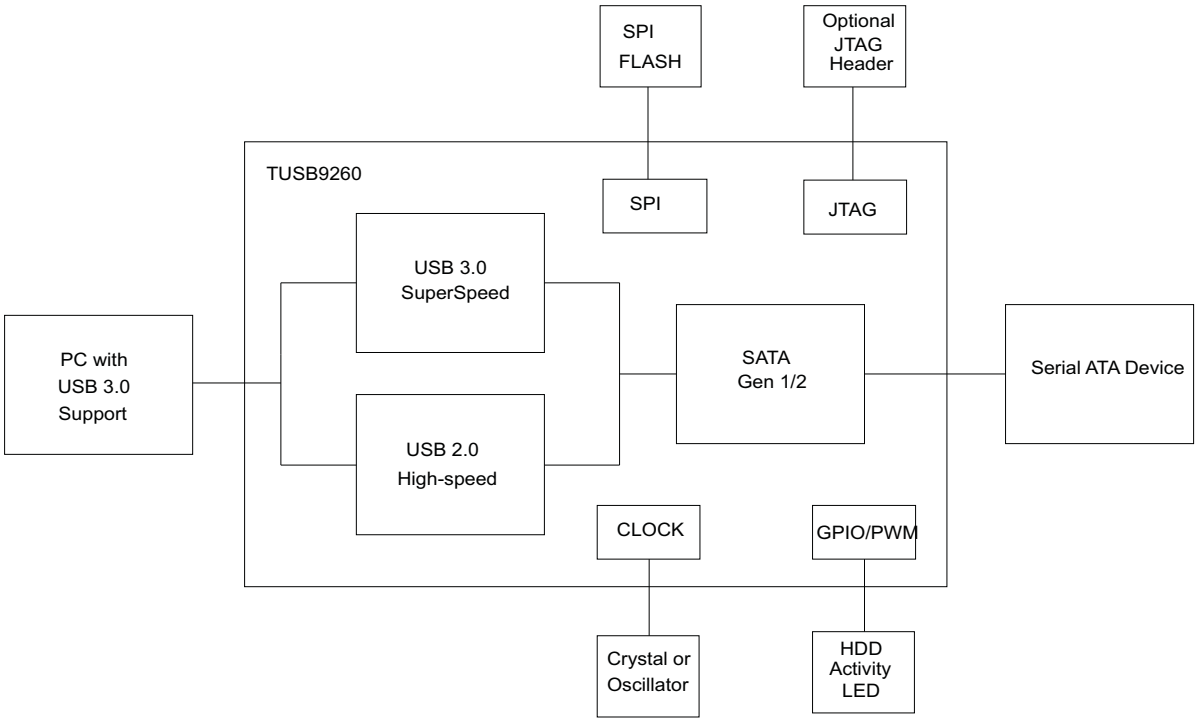


Figure 1. Typical System Implementation

2 Power Considerations

2.1 1.1-V and 3.3-V Digital Supplies

The TUSB9260 requires 1.1-V and 3.3-V digital power source.

The 1.1-V terminals are named VDD11. These terminals supply power to the digital core. The 1.1- V core allows for a significant reduction in both power consumption and logic switching noise.

The 3.3-V terminals are named VDD33 and supply power to most of the input and output cells.

Both VDD11 and VDD33 supplies must have 0.1-µF bypass capacitors to VSS (ground) to ensure proper operation. One capacitor per power terminal is sufficient and should be placed as close to the terminal as possible to minimize trace length. Smaller value capacitors like 0.01-µF are also recommended on the digital supply terminals.

When placing and connecting all bypass capacitors, high-speed board design rules must be followed.

2.2 1.1-V, 1.8-V and 3.3-V Analog Supplies

A Pi filter is recommended on all analog power terminals to minimize circuit noise. These filters can be combined on a per-rail basis for a total of three (VDDA11/VDDA11_USB2) + (VDDA18/VDDR18) + (VDDA33).

Analog power terminals must have a 1-µF and a 10-µF bypass capacitor connected to VSSA (ground) to ensure proper operation. Place the capacitor as close as possible to the associated terminal to minimize trace length. Smaller value capacitors such as 0.1-µF and 0.01-µF are also recommended on the analog supply terminals.

2.3 Ground Terminals

VSS, VSSA, VSS18, and VSS33 can be connected together to form one ground plane. This technique allows for creating a large image plane for the signal layer directly adjacent to the ground plane.

2.4 Capacitor Selection Recommendations

When selecting bypass capacitors for the TUSB9260 device, X7R-type capacitors are recommended. The frequency versus impedance curves, quality, stability, and low-cost of these capacitors make them a logical choice for most computer systems.

The selection of bulk capacitors with low-ESR specifications is recommended to minimize low-frequency power supply noise. Today, the best low-ESR bulk capacitors are radial leaded aluminum electrolytic capacitors. These capacitors typically have ESR specifications that are less than 0.01 Ω at 100 kHz. Also, several manufacturers sell “D” size surface mount specialty polymer solid aluminum electrolytic capacitors with ESR specifications slightly higher than 0.01 Ω at 100 kHz. Both of these bulk capacitor options significantly reduce low-frequency power supply noise and ripple.

2.5 Power-Up/Down Sequencing

All TUSB9260 analog and digital power terminals must be controlled during the power-up and power-down sequence to ensure that absolute power terminal ratings are not exceeded as doing so can result in damage to the device.

No particular power-up or power-down sequencing of the power rails is required.

For additional power requirements, please refer to the TUSB9260 Data Manual (SLLS962).

2.6 External Voltage Regulator Recommendation

Since the TUSB9260 requires three voltage supplies (1.1-V, 1.8-V, and 3.3-V) a multi-channel voltage regulator is recommended. The TPS650061 or TPS65024x are good choices. The TPS650061 utilizes a DCDC converter and two LDO regulators in a single package. The DCDC converter can supply 1-A nominal current while the two LDO's can supply 300-mA nominal current. Since the 1.1-V supply can consume upwards of 340-mA of current the DCDC converter is ideal for supplying the 1.1-V current while the two LDO's can be used to supply 1.8-V and 3.3- V current. Likewise the TPS65024x utilizes three DCDC converters and three LDO's. Both devices also have a built in supervisor circuit that can be connected to GRST# on the TUSB9260.

2.7 TUSB9260 Power Consumption

Nominal power ratings for the TUSB9260 are shown in Table 1. Measurements were taken at nominal voltage while transferring data via USB3 to a SSD drive.

Table 1. TUSB9260 Nominal Power Consumption by Voltage Rail (Approximate)

VOLTAGE RAIL	CURRENT	POWER
3.3 V	6 mA	19.8 mW
1.8 V	58 mA	104.4 mW
1.1 V	319 mA	350.9 mW
Total	383 mA	475.1 mW

2.8 USB VBUS

Power can be supplied via a USB cable on the terminal VBUS. VBUS is a 5-V source that is connected to the USB_VBUS terminal on the TUSB9260 via a voltage divider. Connect a 90.9-kΩ, 1% resistor from the cable VBUS connector to the USB_VBUS terminal on the TUSB9260 and a 10-kΩ, 1% resistor from USB_VBUS to ground.

2.8.1 Limiting Inrush Current on VBUS

To prevent inrush current the TI TPS2560/61 is recommended. Inrush current can occur on VBUS when a function is plugged into the network. For example the bulk capacitance used to supply power to the SATA device can be quite large, causing inrush current when the USB cable is connected. The TPS2560/61 power-distribution switches are intended for applications where heavy capacitive loads are likely to be encountered. The TPS2560/61 has two controllable outputs that can be controlled via the TUSB9260 GPIO terminals. In the example implementation the TUSB9260 is used to switch power on or off to the SATA device by controlling the EN2 terminal on the TPS2561.

3 USB Connection

There are three sets of differential pairs for connecting the USB port; one set for High-Speed and two sets for SuperSpeed.

3.1 High-Speed Differential Routing

The high-speed differential pair (USB_DM and USB_DP) is connected to a USB type B connector. The differential pair traces should be routed with 90-Ω, ±15% differential impedance. The high-speed signal pair should be trace length matched. Maximum trace length mismatch between High-Speed USB signal pairs should be no greater than 150 mils. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. No termination or coupling caps are required. If a common mode choke is required then place the choke as close as possible to the USB connector signal pins. Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke).

In order to minimize cross-talk on the USB2/3 differential signal pairs, it is recommended that the spacing between the two interfaces be five times the width of the trace (5W rule). For instance, if the SS USB TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs and the DP/DM differential pair.

If this 5W rule cannot be implemented, then the space between the TX/RX differential pairs and DP/DM differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

3.2 SuperSpeed Differential Routing

SuperSpeed consists of two differential routing pairs, a transmit pair (USB_SSTXM and USB_SSTXP) and a receive pair (USB_SSRXM and USB_SSRXP). Each differential pair's traces should be routed with 90-Ω, ±15% differential impedance. The high-speed signal pair should be trace length matched. Maximum trace length mismatch between SuperSpeed USB signal pairs should be no greater than 2.5 mils. The transmit differential pair does not have to be the same length as the receive differential pair. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. The transmitter differential pair requires 0.1-µF coupling caps for proper operation. The package/case size of these caps should be no bigger than 0402. C-packs are not allowed. The caps should be placed symmetrically as close as possible to the USB connector signal pins. If a common mode choke is required then place the choke as close as possible to the USB connector signal pins (closer than the transmitter caps). Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke and transmitter caps).

It is permissible to swap the plus and minus on either or both of the SuperSpeed differential pairs. This may be necessary to prevent the differential traces from crossing over one another. However it is not permissible to swap the transmitter differential pair with receive differential pair.

In order to minimize cross-talk on the SS USB differential signal pairs, it is recommended that the spacing between the TX and RX signal pairs be five times the width of the trace (5W rule). For instance, if the SS USB TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs.

If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

4 SATA Connection

The TUSB9260 supports one 3G SATA port operating at 1.5 GHz or 3 GHz depending on the maximum speed of the attached device.

4.1 SATA Differential Routing

The SATA traces (SATA_TXP and SATA_TXM) should be routed with 100-Ω, ±15% differential impedance. Maximum trace length mismatch between SATA signal pairs should be no greater than 2.5 mils. Transmit differential pair does not have to be the same length as receive differential pair. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. Each SATA trace requires a coupling capacitor be placed inline. The package/case size of these caps should be no bigger than 0402. C-packs are not allowed. The caps should be placed symmetrically as close as possible to the SATA connector signal pins.

It is permissible to swap the plus and minus on the SATA differential pair. This may be necessary to prevent the differential traces from crossing over one another. However it is not permissible to swap the transmitter diff pair with the receive diff pair.

In order to minimize cross-talk on the SATA differential signal pairs, it is recommended that the spacing between the TX and RX signal pairs for each interface be five times the width of the trace (5W rule). For instance, if the SATA TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs.

If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

5 ESD Protection

The TUSB9260 provides ESD protection on all signal and power pins up to 2000 V using the human body model and 500 V using the charged device model. If more protection is required, the TI TPD2EUB30 can be used as this device meets or exceeds IEC61000-4-2 (Level 4) requirements. This device can be used on any of the differential pairs of the TUSB9260. Place the device as close as possible to the signal pins of the connector. Refer to the datasheet for more information regarding this device.

6 GPIO Terminals

The TUSB9260 supports a minimum of 12 GPIOs. Some GPIO terminals have dual functionality depending on how they are configured.

6.1 GPIO[7:0]

GPIO terminals 7 through 0 can be used for general purpose use such as connecting activity LEDs, used as push-button input, or connected to various signals from other devices. Each GPIO terminal has internal pull-down resistors. If a GPIO terminal is not used it should be left unconnected.

6.2 GPIO[8/UART_RX:9/UART_TX]

GPIO terminals 8 and 9 are dual function terminals. They can be used as general purpose input/output terminals like GPIO[7:0] or they can be configured as an UART interface. Both terminals have internal pull-up resistors, so they can be left unconnected if not used.

6.3 GPIO[10/SPI_CS2:11/SPI_CS1]

GPIO terminals 10 and 11 are dual function terminals. They can be used as general purpose input/output terminals like GPIO[7:0] or they can be configured as SPI chip select terminals for additional peripherals such as an LCD driver. Both terminals have internal pull-up resistors, so they should be left unconnected if not used.

7 PWM Terminals

The TUSB9260 has two pulse width modulated (PWM) terminals. These terminals are always outputs. They should be left unconnected if not used.

8 JTAG Interface

The TUSB9260 supports JTAG for board level test and debug support. Typically these terminals are left unconnected or routed to a header to plug in an external JTAG controller. Table 2 shows the JTAG terminal names and internal resistor connection. The JTAG interface should be left unconnected if JTAG support is not required.

Table 2. Internal JTAG Resistor Termination

NAME	PULL-UP OR PULL-DOWN	DESCRIPTION
JTAG_TCK	Pull-down	JTAG test clock
JTAG_TDI	Pull-up	JTAG test data in
JTAG_TDO	Pull-down	JTAG test data out
JTAG_TMS	Pull-up	JTAG test mode select
JTAG_RSTZ	Pull-down	JTAG reset

9 External Reference Clock

The TUSB9260 requires an external reference clock. This clock can be derived from an existing clock, crystal, or oscillator. The TUSB9260 supports one clock frequency as shown in Table 3. FREQSEL[1:0] terminals can be connected directly to ground or tied to VDD33.

Table 3. External Reference Clock Selection

FREQSEL[1:0]	INPUT FREQUENCY (MHz)
00b	Reserved
01b	Reserved
10b	Reserved
11b	40

9.1 Crystal Selection

Select a fundamental mode crystal with load capacitance of 12 pF – 24 pF and PPM rating of ±100 PPM or better. Connect the crystal between the XI and XO terminals with a 1-MΩ shunt resistor as shown in Figure 2. Place the crystal near the XI and XO terminals. Try to keep the XI and XO traces to a minimum length with few or no vias as shown in Figure 3.

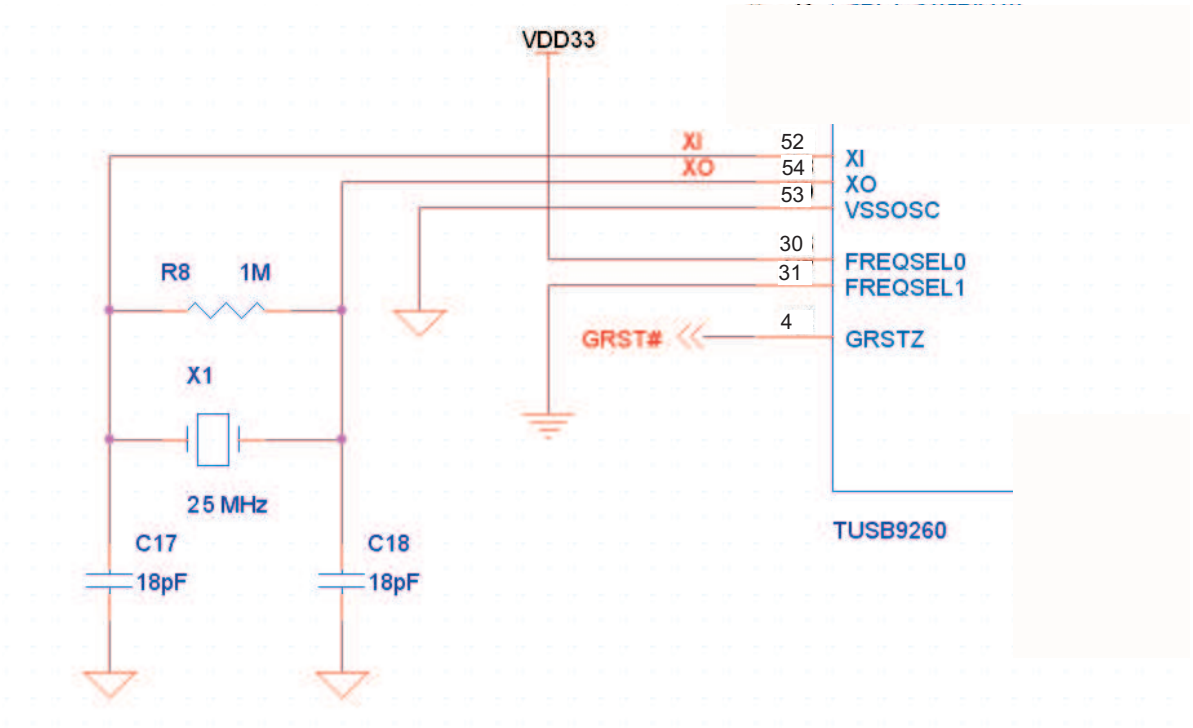


Figure 2. Example Crystal Implementation

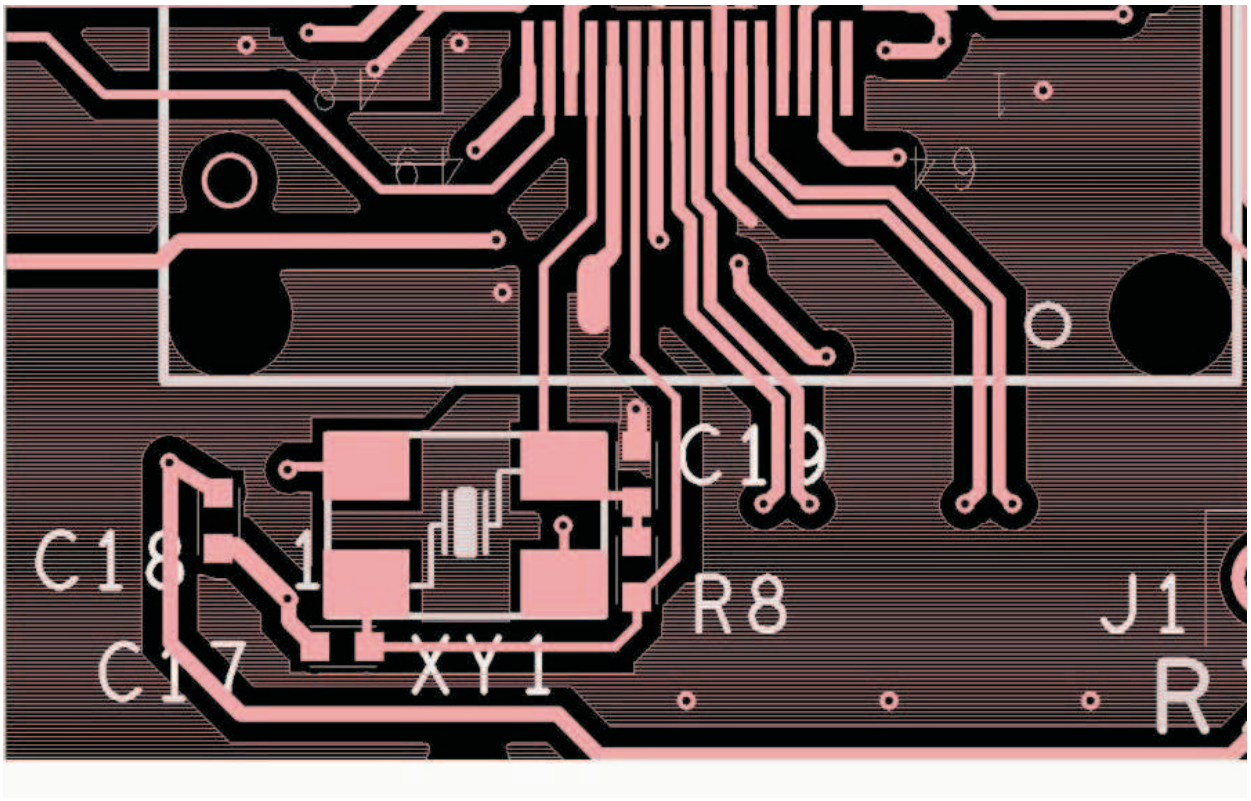


Figure 3. Example Reference Clock Layout

9.2 External Clock/Oscillator Selection

When using an external clock source such as an oscillator, the reference clock should have ±100 PPM (or better) frequency stability and have less than 50-ps absolute peak to peak jitter or less than 25-ps peak to peak jitter after applying the USB 3.0 jitter transfer function.

Connect the output of the clock source or oscillator to the XI terminal. Leave the XO terminal unconnected as shown in Figure 4. Try to keep the clock trace to a minimum length with few or no vias.

Note that the TUSB9260 has a VSSOSC terminal. This terminal is the reference ground for the internal oscillator. This reference ground should be used for the crystal circuit, which is also shown in Figure 4.

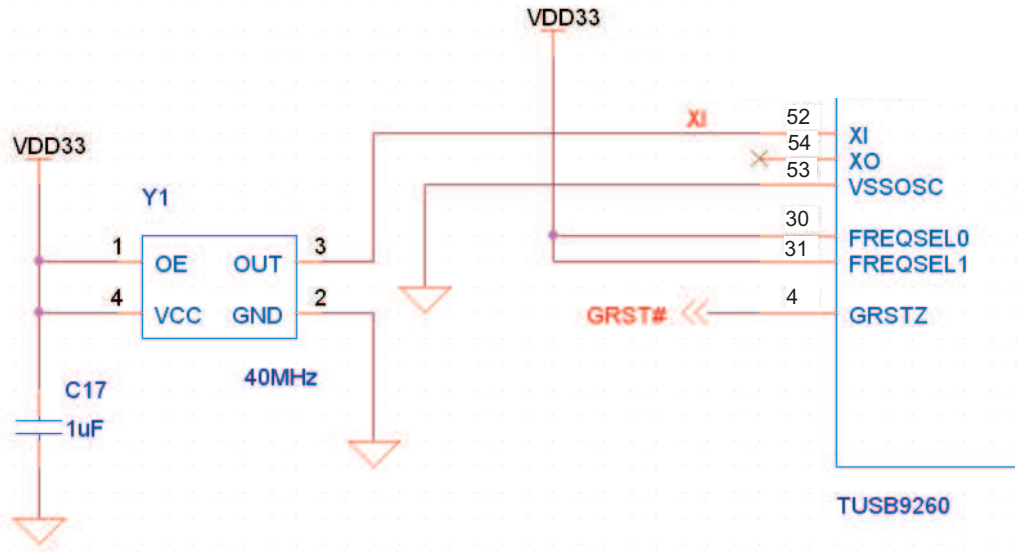


Figure 4. Example Oscillator Implementation

10 Serial Peripheral Interface (SPI)

A SPI system consists of one master device and one or more slave devices. The TUSB9260 is a SPI master providing the SPI clock, data-in, data-out and up to three chip select terminals.

The SPI has a 4-wire synchronous serial interface. Data communication is enabled with a low active Chip Select terminal (SPI_CS[2:0]#). Data is transmitted with a 3-terminal interface consisting of terminals for serial data input (SPI_DATA_IN), serial data output (SPI_DATA_OUT) and serial clock (SPI_SCLK). All SPI terminals have integrated pull-up resistors. No external components are required to connect the SPI interface to an external SPI flash device. See Figure 5 for an example implementation of the SPI interface using one SPI slave device.

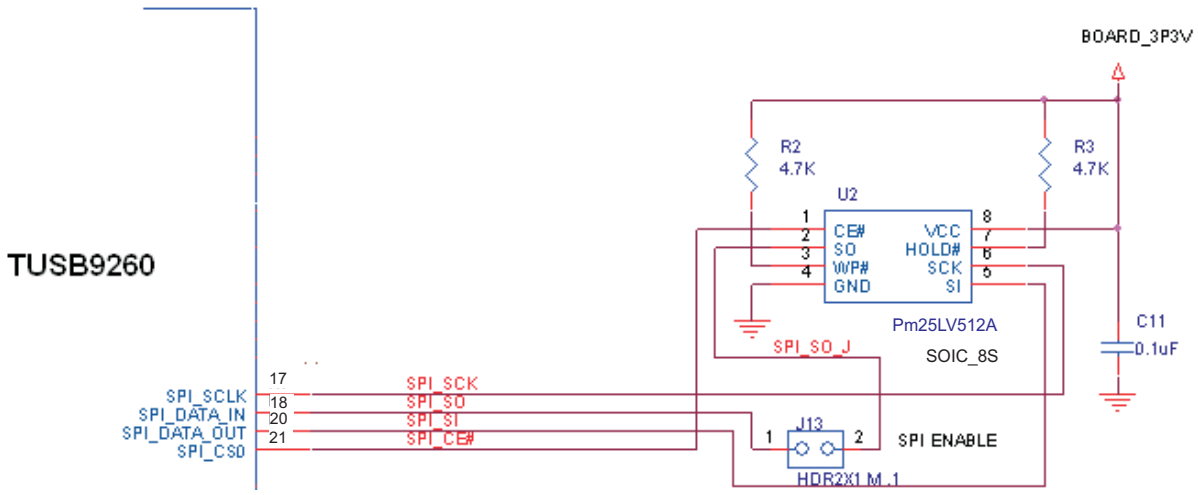


Figure 5. SPI Connection

The SPI interface can operate over a frequency range of 100 kHz to 50 MHz. The word size for the flash must be 8 bits. A minimum flash size of 512 kbits (64 k x 8) is recommended. Table 4 shows SPI flash devices that have been tested with the TUSB9260.

Table 4. Flash Devices Tested on the TUSB9260

MANUFACTURER	PART NUMBER	DENSITY (kbit)	PAGE SIZE (bytes)	MAX CLOCK FREQUENCY READ COMMAND (MHz)
Numonyx/ST	M25P05A	512	256	20 / 25
Numonyx/ST	M25P10A	1024	256	20 / 25
Atmel	AT25FS010	1024	256	50
Pflash	Pm25LV512A	512	256	33
Pflash	Pm25LV010A	1024	256	33

11 Precision Reference Return Resistor

The TUSB9260 requires an external precision reference return resistor. This resistor is part of the USB2.0 PHY core used for internal calibration. A 10-kΩ, ±1% (1/20 W or greater) precision resistor should be placed between terminals USB_R1 and USB_R1RTN. This resistor should be placed no further than 500 mils from the two terminals.

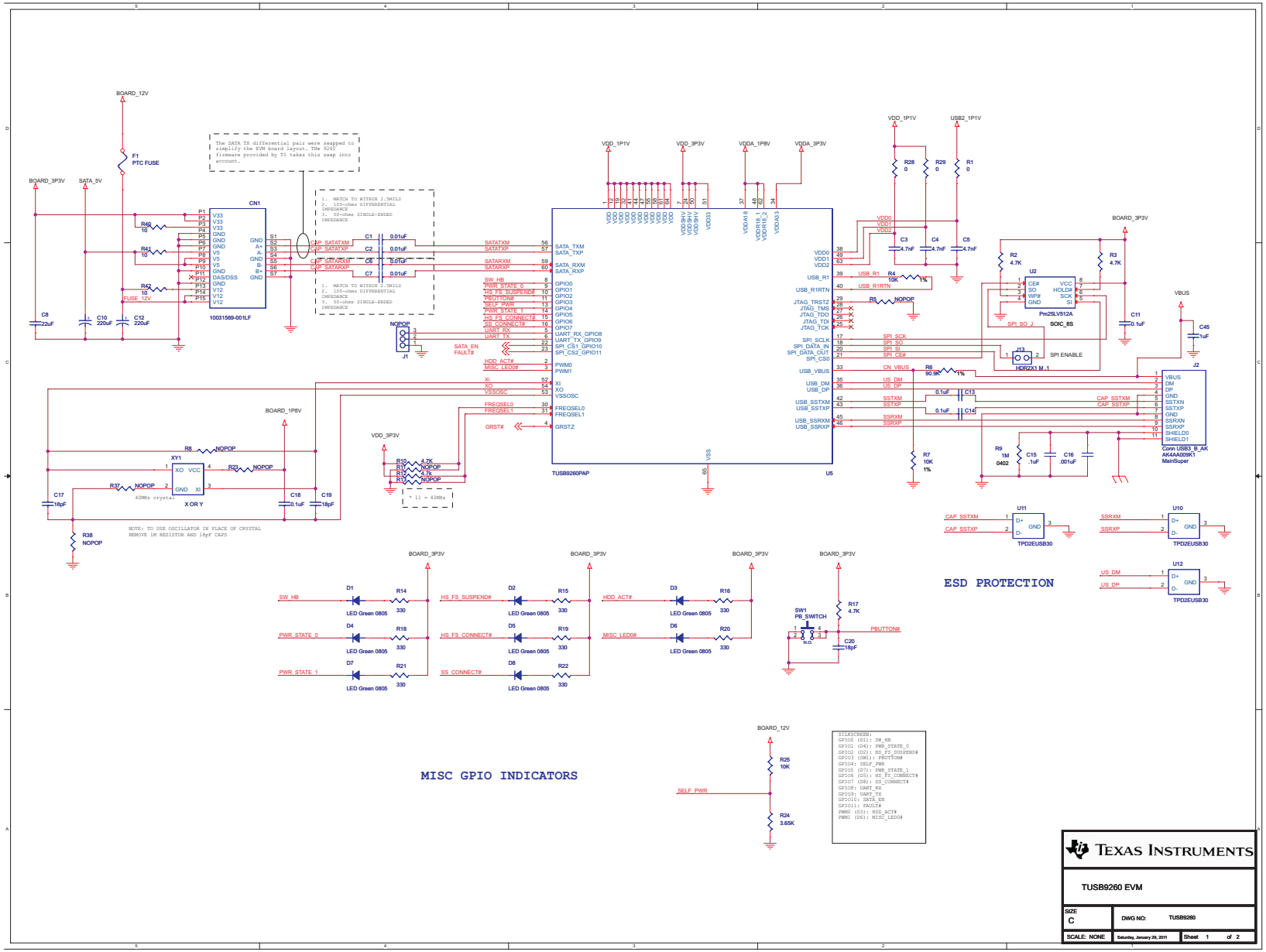
12 External PLL Loop Capacitors

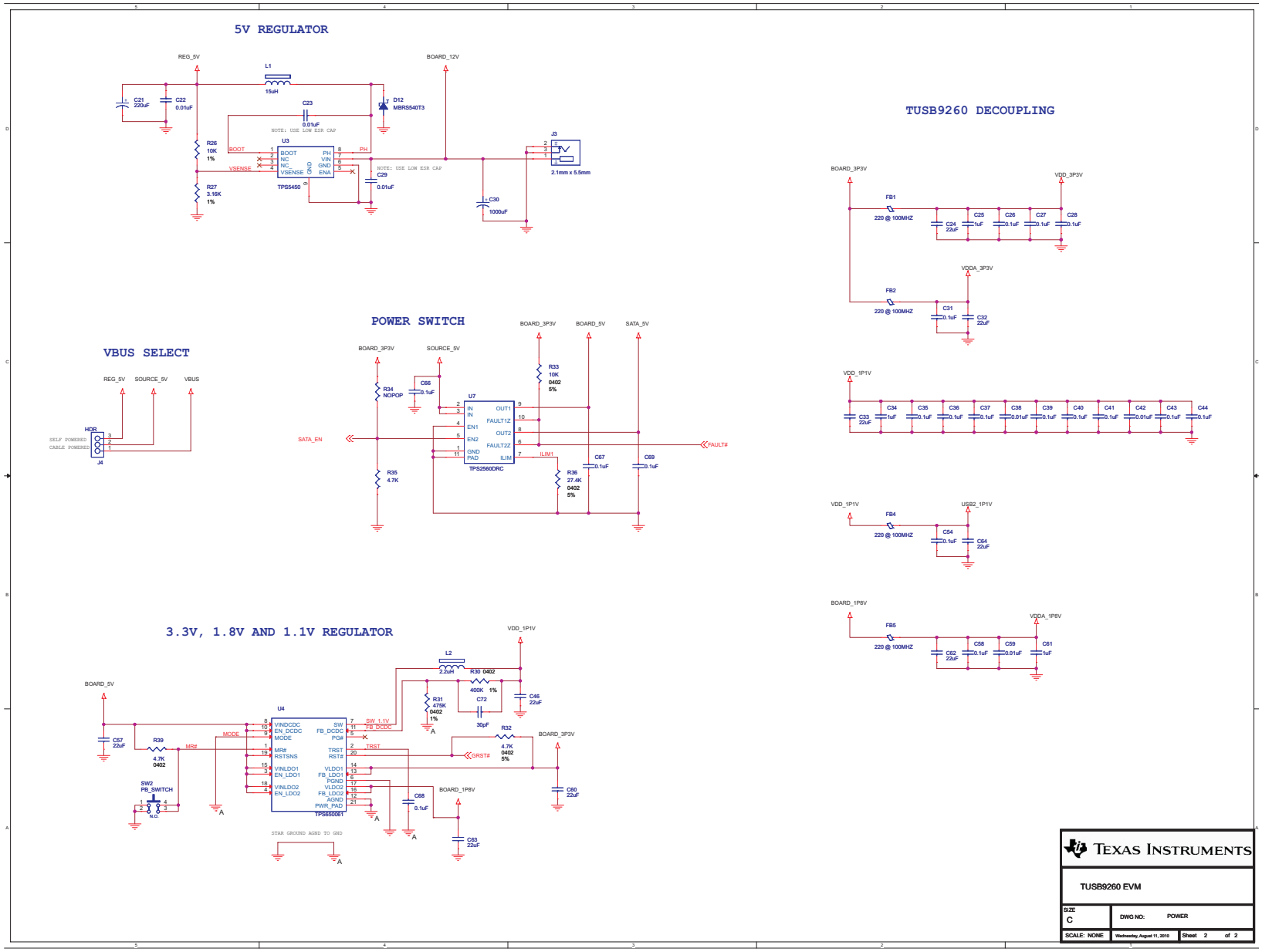
There are three terminals on the TUSB9260 that require external capacitors. These are the external loop capacitors for each of the three PLL's in the TUSB9260. CEXT0 terminal is used for the USB 2.0 PHY PLL, CEXT1 terminal is used for the SuperSpeed PHY PLL, and terminal CEXT2 is used for the SATA PLL.

All three CEXTx terminals require a 4.7-nF capacitor connected to ground. Each capacitor should be placed within 500 mils of its associated terminal and provide adequate shielding from external noise sources.

13 Example Schematics

The following schematic is provided as a reference design. There is one user configurable jumper (J4) on the board. A jumper must be placed across pins 1 and 2 or across pins 2 and 3 depending on the desired power option. When the jumper is placed across pins 1 and 2 a flash drive can be powered directly from the USB cable power eliminating the need for an external wall-wart. However it should be noted that SATA devices that require 12 V will not operate in this mode. To support all SATA devices place the jumper across pins 2 and 3 and connect a 12-V / 2-A wall-wart to DC jack J3 (positive tip).





IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265