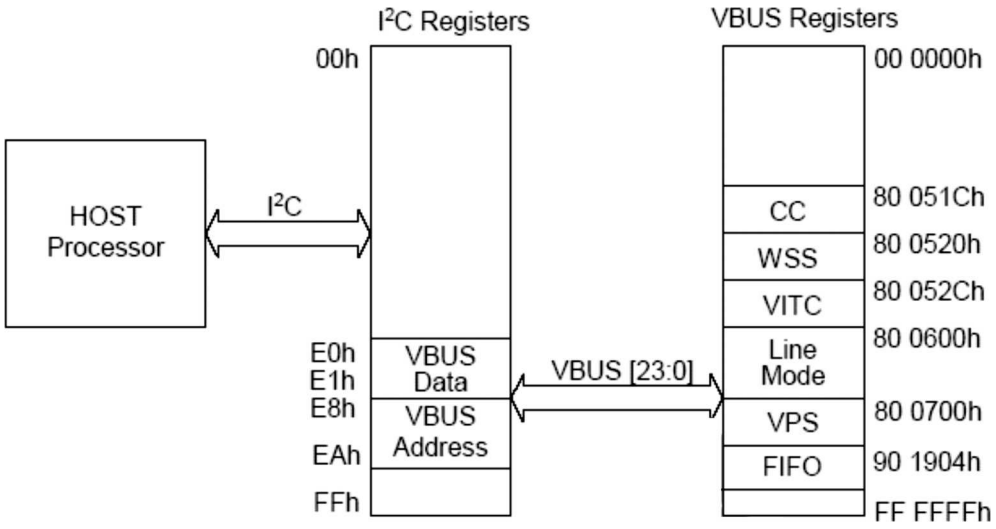
TVP5146M2 Patch Code Download Guidelines

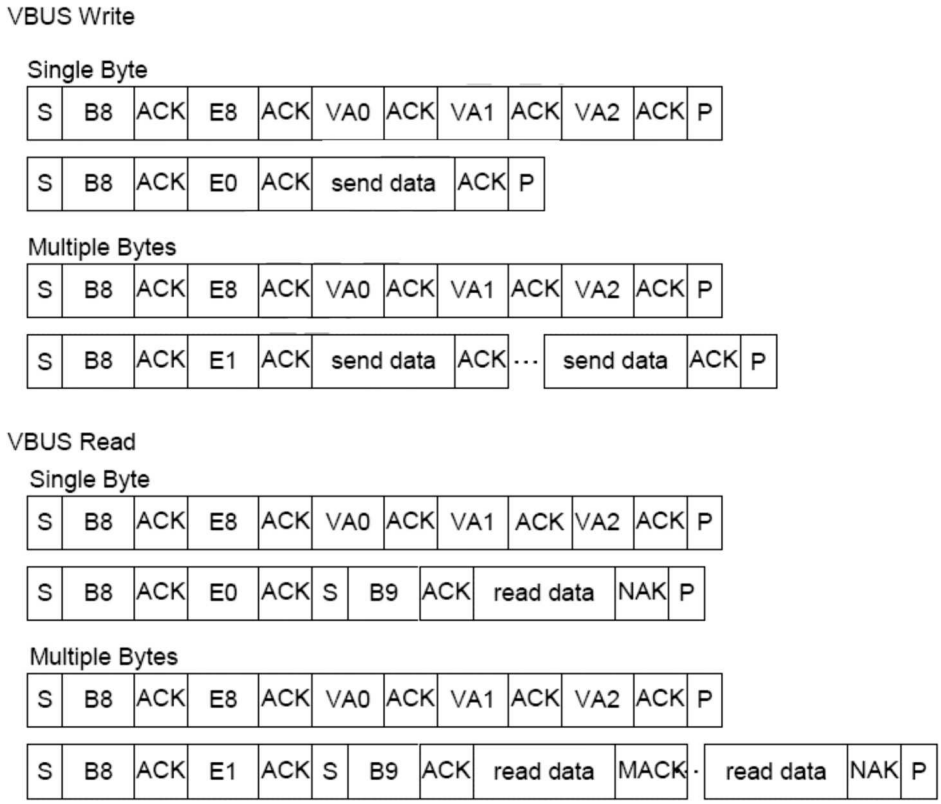
1 Overview

This application note explains how to load RAM code into the TVP5146M2 video decoder. The TVP5146M2 video decoder by default executes firmware from internal ROM on power up. Special functions or optimizations are available by utilizing the internal RAM of the TVP5146M2. The following describes the processed required to access and load code into the TVP5146M2 RAM.

2 Understanding the VBUS

It is important to understand that loading RAM code is not a feature provided by the standard I^{2}C register map. This procedure requires I^{2}C writes to the physical hardware of the TVP5146M2 CPU. These internal registers of the TVP5146M2 video decoder are known as VBUS registers. The follwoing figures show a typical VBUS register access.





The examples above use default the I^2C address, 0xB8. The acronyms used in the example are:

ACK – Acknowledge generated by the slave

MACK – Acknowledge generated by the master

NAK – No Acknowledge generated by the master

3 The Process

There are six steps required to properly load RAM code into the TVP5146M2. There is an additional optional step that performs a CRC on the RAM code load if desired.

1. Place the CPU into Reset

   By writing a 1 to bit 0 of the first byte in the 0xB00060 VBUS address, the internal processor is placed into a reset state. This is necessary in order to load RAM code. To do this the VBUS address must first be set. Set VBUS address to 0xB00060 by making the following I^2C writes.

   0xE8, 0x60

   0xE9, 0x00

   0xEA, 0xB0

   Where:

   0xE8, 0xE9, 0xEA indicate the bytes of the address being setup (byte1, etc.)

   0x60, 0x00, 0xB0 indicate the bytes of the physical VBUS address

   Once these writes have been performed, the current VBUS address is set to 0xB00060. Use the non-incrementing data register, 0xE0, to set the Reset bit by setting bit 0 to 1.

   0xE0, 0x01

2. Set the VBUS to the Beginning of Program RAM

   Now that the internal processor is in a reset state, the following I^2C writes will set the VBUS to the beginning of Program RAM. This is the location in which the RAM code will be stored during the loading process. Set the VBUS address to the beginning of Program RAM, 0x400000.

   0xE8, 0x00

   0xE9, 0x00

   0xEA, 0x40

3. Load the RAM Code

   With the VBUS now set to the beginning of Program RAM, start loading the provided RAM code *.bin file using the following writes. Since the firmware code data is loaded at once, the incrementing VBUS data register, 0xE1 must be used, where:

   0xE1, (RAM Code Data)

   Using the above technique, all of the bytes of the firmware should be written using a single I^2C transaction. See below for details.

   ST B8 E1 D0 D1 ... DN-1 SP

   Where:

   ST = I^2C start condition

   B8 = TVP5146M2 device I^2C address for writes (could also be BA depending on the GLCO/I^2CA pin at the end of RESET)

   E1 = I^2C sub-address of the incrementing VBUS data register

   D0 D1 ... DN-1D = Data from the binary firmware file. N is the number of bytes in the firmware file.

   SP = I^2C stop condition

4. Set the RAM Loaded Bit

   For the default ROM code to understand RAM load has been used, the RAM Loaded bit must be used. This is used by the internal CPU to execute out of RAM instead of ROM. To set the RAM Loaded Bit set VBUS address to 0xB00060.

   0xE8, 0x60

   0xE9, 0x00

   0xEA, 0xB0

   Write 0x03 to the non-incrementing VBUS data register, 0xE0 sets the RAM Loaded Bit and keeps the CPU RESET bit set.

   0xE0, 0x03

5. OPTIONAL – Run CRC

As an optional step, it is possible to perform a CRC after downloading RAM code to the TVP5146M2. This optional step allows the system to verify whether RAM code was successfully loaded into the TVP5146M2.

By default, CRC is disabled. To enable Run CRC, set VBUS address 0xB00063 bit 2 to 1 (0x04). To set up the address, write the following:

0xE8, 0x63

0xE9, 0x00

0xEA, 0xB0

To write 0x04 to the VBUS data register, write the following:

0xE0, 0x04

Now that Run CRC bit has been enabled, CRC will start once the CPU has been released from reset as described in the next step, 6. Release the CPU Reset.

NOTE: Once the CPU is taken out of the reset state and CRC is enabled, the processor will execute the CRC process. This process requires approximately 20ms to complete during which time I^2C transactions will be unavailable.

To view the results of the CRC read bits[1:0] of VBUS address 0xB00063, where:

00 = CRC was not performed

01 = PASS - RAM code loaded successfully

10 = Reserved

11 = FAIL - RAM code not loaded successfully

If the CRC fails, re-start the load RAM process from the beginning.

6. Release the CPU Reset

To restart the CPU and release it from its reset state, a write of 0x02 to the same VBUS address as above (0xB00060) is necessary.

0xE8, 0x60

0xE9, 0x00

0xEA, 0xB0

0xE0, 0x02

NOTE: If running CRC, this step must be performed first before the result of the CRC is available.

7. The patch code should now be running.

The revision number can be verified by reading the ROM version, RAM version MSB, and RAM version LSB from I^2C registers 0x70, 0x71, and 0x82, respectively.

For example,

Patch Release = v08.00.06

ROM Version = 0x08

RAM Version MSB = 0x00

RAM Version LSB = 0x06

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