

Implementation of Power Supply Volume Control

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ABSTRACT

This document gives design guide lines for applications using the power supply volume control (PSVC). The power supply volume control increases system performance by:

- Volume can be decreased without loss of audio resolution, in the range where PSVC is active.
- When supply voltage for PVDD is decreased, the noise voltage at the output decreases as well. The ratio between noise voltage and maximum RMS voltage (DNR) then increases. The user experiences better noise performance at usual listening levels. E.g. a system having 102 dB in DNR and a power supply range of 18 dB will have a SNR up to 120 dB.
- Reduces power consumption and heat in the system at usual listening levels, thereby increasing the lifetime of the system.
- Many EMI tests are performed at a reduced volume setting. FTC requires 1/8 of maximum output power equal to a volume setting of -9 dBFS. By use of the PSVC operating voltage during EMI, the test will be reduced giving reduced switching noise in the system.

The PSVC is supported in Texas Instruments PWM processors like the TAS5508, which makes implementation easy. For other modulator types like the TAS5066 and TAS5076, the PSVC can also be implemented. However, on these devices all calculations and control must be handled by the micro controller.

This document gives design guidelines, how to implement PSVC correctly for the TAS5508. To implement PSVC for other PWM processors like the TAS5066 and TAS5076, contact the Texas Instruments digital audio applications team.

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1 Introduction

1.1 PSVC Advantages

Using a combination of digital gain and power supply to the control volume setting gives several advantages:

- Volume can be decreased without loss of audio resolution, in the range where PSVC is active.
- When supply voltage for PVDD is decreased, the noise voltage at the output decreases as well. The ratio between noise voltage and maximum RMS voltage (DNR) then increases. The user experiences better noises performance at usual listening levels. E.g. a system having 102 dB in DNR and a power supply range of 18 dB will have an SNR up to 120 dB.
- Reduces power consumption and heat in the system at usual listening levels. Thereby increasing lifetime of the system.
- Many EMI tests are performed at reduced volume setting. FTC requires 1/8 of maximum output power equal to a volume setting of -9 dBFS. By use of PSVC, the operating voltage during EMI test will be reduced, giving reduced switching noise in the system.

With only a minimum extra complexity audio performance can be improved and EMI tests become easier to pass.

1.2 PSVC Concept

Speaker output voltage can at be calculated as:

$$V_{SPEAKER}(t) = d(t) \cdot V_{PSU}$$

Where d is the duty cycle that varies according to the audio signal and V_{PSU} is the power supply voltage. From this equation it can be seen that the output volume can be controlled from either the duty cycle or the power supply voltage. Note that when the output volume level is calculated in dB, the following formula is used:

$$V_{SPEAKER}(dB) = d(dB) + V_{PSU}(dB)$$

Using this formula it becomes easier to calculate total output volume. The concept pf PSVC is to have the power supply to control from 0 dBFS to e.g. -24 dBFS and then use digital gain to control volume above 0 dBFS and below -24 dBFS. The lower crossover point (e.g. -24 dBFS) can be selected differently depending on the power supply configuration.

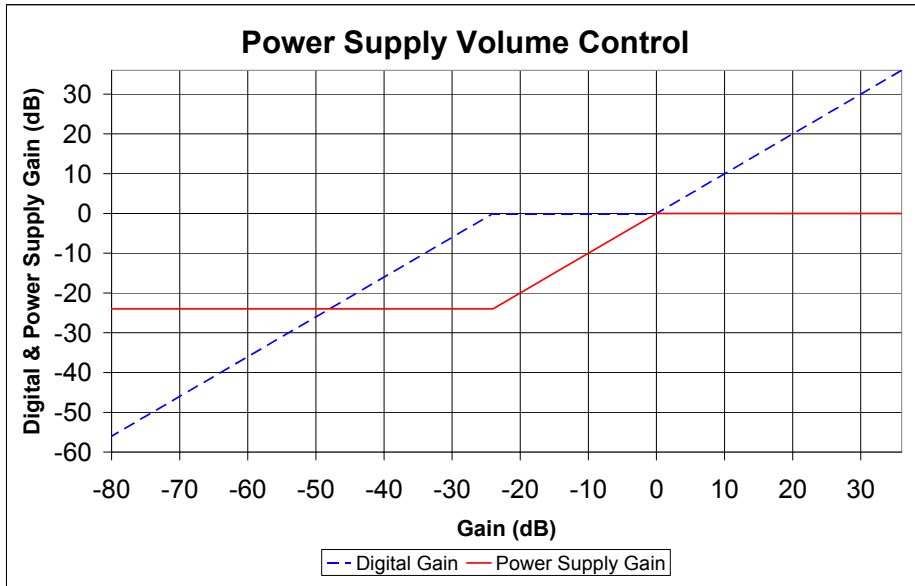


Figure 1. Digital and Power Supply Gain

Figure 1 shows gain settings for both digital circuits and a power supply at different desired gains. The resulting gain (or volume level) is the two gains, digital and power supply gain, added together. This is shown in Figure 2 according to the previous formula.

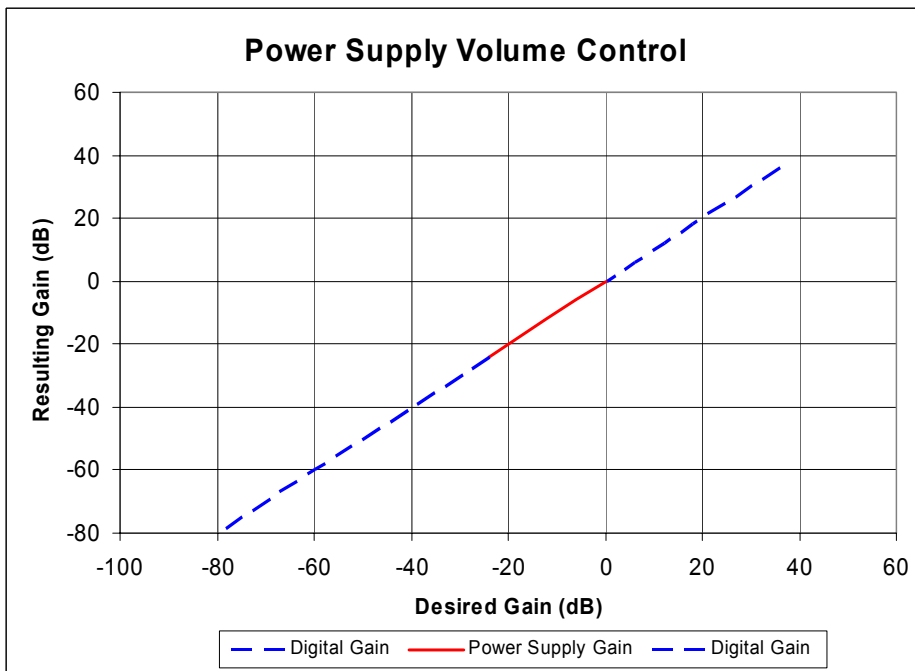


Figure 2. Resulting Gain

The resulting gain is linear to the desired gain, where the power supply controls the gain from -24 dBFS to 0 dBFS.

Note that minimum power supply gain (lower crossover point of -24 dBFS) must be selected different depending on the power supply capability, e.g. -18 dBFS or -12 dBFS.

2 General Structure

To set the volume correctly, the volume setting must be split into a digital gain setting and a power supply gain setting. Care must be taken to get these calculations right. Especially the calculations at the two crossover points can cause non linear volume control if not done correctly. The TAS5508 automatically calculates settings for digital gain and power supply gain.

A flow chart to calculate volume settings is shown in Figure 3. The principle is to set the power supply volume according to the channel having the highest volume setting and then recalculate gain setting for the digital circuits. The TAS5508 uses a sequence based on this flow chart to calculate gain settings for digital gain and power supply gain.

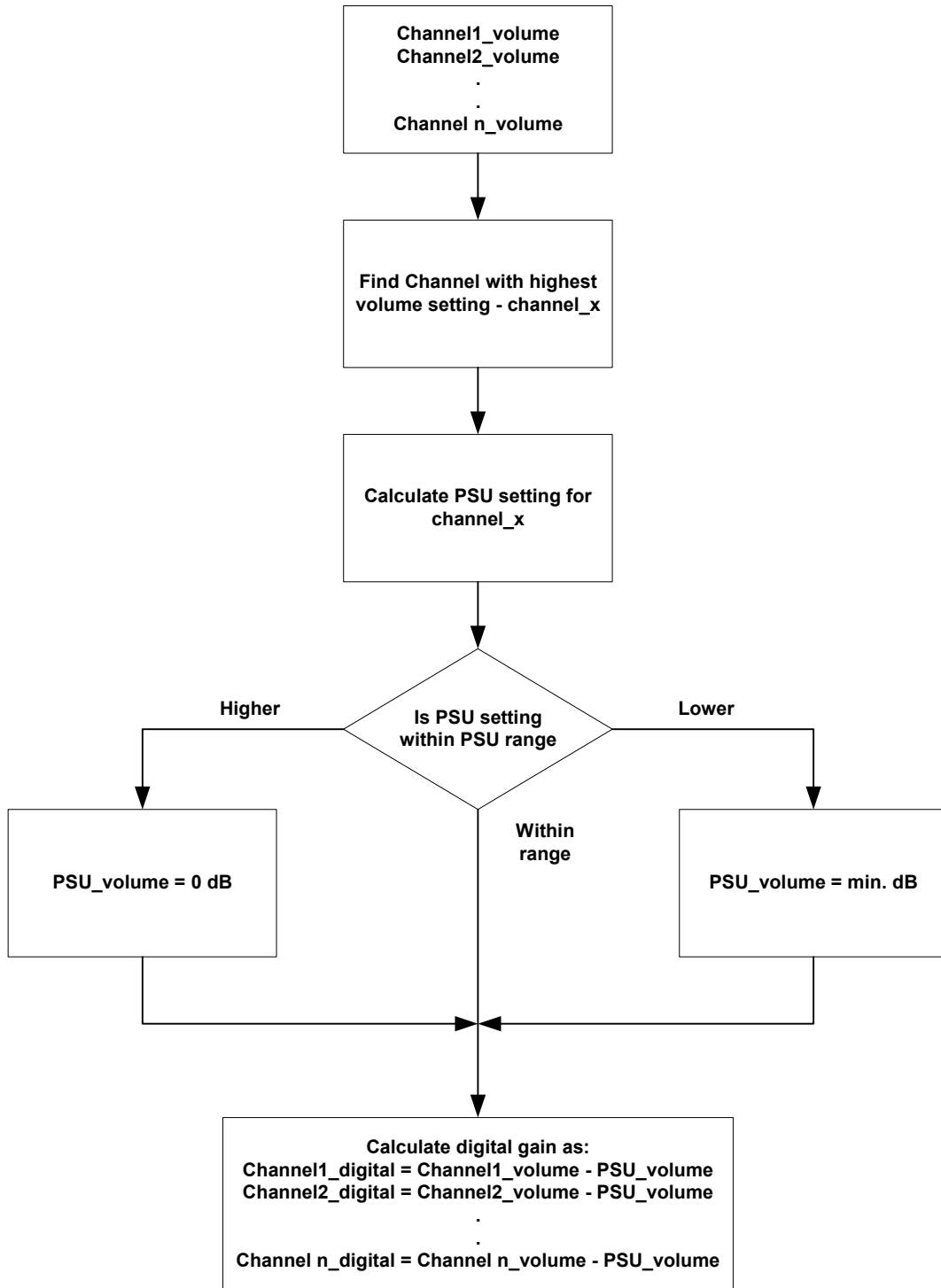


Figure 3. Volume Calculation Flow Chart

2.1 Examples of Gain Settings

The following examples are for a three channel system. The power supply can be controlled from -18 dB to 0 dB.

2.1.1 Gain Setting Within the PSU Range

System requirement settings:

Channel1_volume = -14 dB

Channel2_volume = -28 dB

Channel3_volume = -22 dB

Channel 1 is found to have the highest volume setting of -14 dB. The PSU_volume is then set to -14 dB.

Digital gain is then calculated as:

Channel1_digital = -14 dB – (-)14 dB = 0 dB

Channel2_digital = -28 dB – (-)14 dB = -14 dB

Channel3_digital = -22 dB – (-)14 dB = -8 dB

2.1.2 Gain Setting Higher Than the PSU Range

System requirement settings:

Channel1_volume = -14 dB

Channel2_volume = 4 dB

Channel3_volume = -22 dB

Channel 2 is found to have the highest volume setting of +4 dB. The PSU_volume is then set to 0 dB, which is highest setting for the power supply.

Digital gain is then calculated as:

Channel1_digital = -14 dB – 0 dB = -14 dB

Channel2_digital = 4 dB – 0 dB = 4 dB

Channel3_digital = -22 dB – 0 dB = -22 dB

2.1.3 Gain Setting Lower Than the PSU Range

System requirement settings:

Channel1_volume = -28 dB

Channel2_volume = -28 dB

Channel3_volume = -22 dB

Channel 3 is found to have the highest volume setting -22 dB. The PSU_volume is then set to -18 dB, which is lowest setting for the power supply.

Digital gain is then calculated as:

Channel1_digital = -28 dB – (-)18 dB = -10 dB

Channel2_digital = -28 dB – (-)18 dB = -10 dB

Channel3_digital = -22 dB – (-)18 dB = -4 dB

2.2 Power Supply Control

The output voltage of the power supply PVDD is controlled by adjusting the reference voltage. The control loop in the power supply uses this reference voltage to regulate the output. When the reference voltage is changed, PVDD will change accordingly.

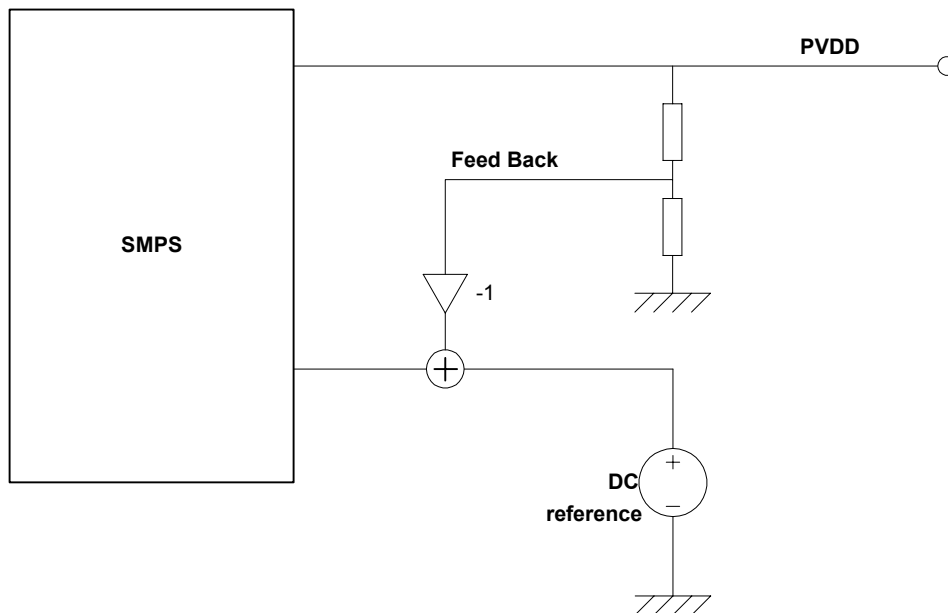


Figure 4. Control of the Power Supply

The reference voltage must be controlled from the TAS5508. If the reference voltage is an analog voltage that has to pass from the TAS5508 at the amplifier board to the power supply board, the output voltage of the power supply will be erroneous. The voltage may drop when crossing from one board to the next. This makes the volume setting inaccurate. Also, if noise or hum is injected into the reference voltage, this noise will be coupled into the power supply output and then into the speaker output.

This is solved in the TAS5508 by using a PWM signal instead of an analog reference voltage.

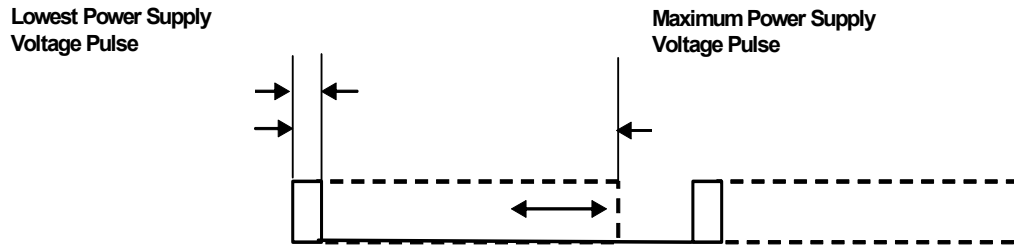


Figure 5. PSVC PWM Pulse

The PSVC PWM pulse has a duty cycle corresponding to the power supply volume setting. The advantage is that all volume information is independent of the voltage level. This means that any voltage drop can be compensated by reclocking the PWM signal at the power supply board. PWM pulses are then converted to the analog reference voltage through a low-pass filter.

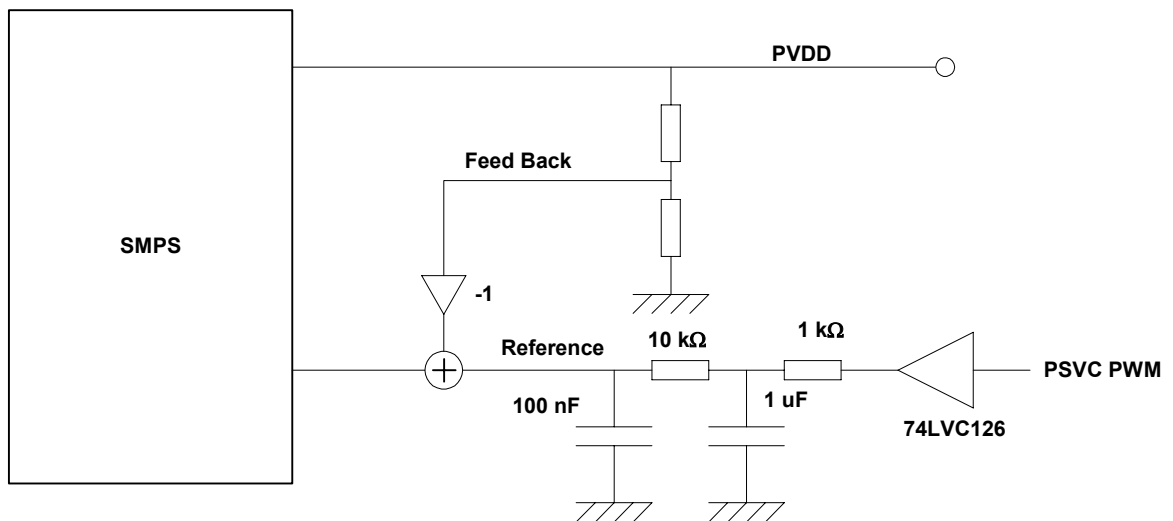


Figure 6. Configuration Using PWM

The PSVC PWM frequency must be above 20 kHz to insure that no audible leftovers from PSVC PWM are coupled into the speaker outputs.

2.3 TAS5508 PSVC PWM Output

When PSVC is enabled, the TAS5508 generates a PWM signal at a frequency of 44.1 kHz or 48 kHz. The PWM frequency is synchronized to the LRCLK of the I2S.

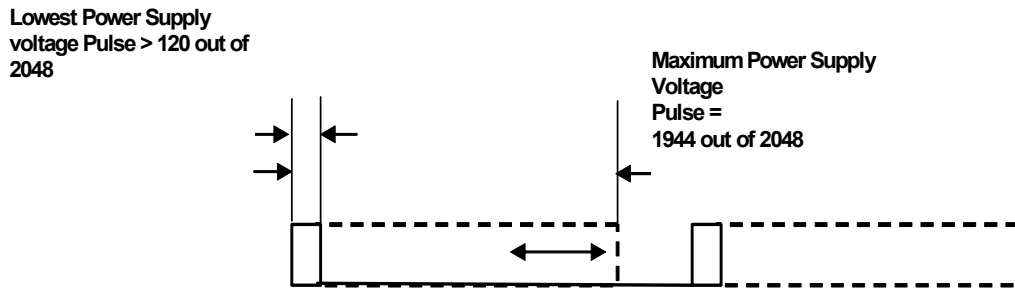


Figure 7. PSVC Output of the TAS5508

The output has a maximum duty cycle of 95% corresponding to 0 dBFS and a minimum duty cycle of 6% corresponding to -24-dB attenuation.

Note that during start up, error recovery, and reset the duty cycle is 0%, 0 V. This can be changed by programming system control register 1 (0x03).

Table 1. System Control Register 1 (0x03)

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	-	-	-	-	-	-	-	PWM High Pass Disabled
1	-	-	-	-	-	-	-	PWM High Pass Enabled
-	0	-	-	-	-	-	-	/Auto Clock Set
-	1	-	-	-	-	-	-	Manual Clock Set
-	-	-	0		-	-	-	Soft Unmute on Recovery from Clock Error
-	-	-	1		-	-	-	Hard Unmute on Recovery from Clock Error
-	-	-	-	1	-	-	-	PSVC Hi-Z Enable
-	-	-	-	0	-	-	-	PSVC Hi-Z Disable
0	0	0	1	0	0	0	0	Default Setting

D0 to D2 is unused bits.

If D3 bit is set high, the PSVC output will go into Hi-Z during error recovery. This is however not recommended, since this interferes with the reclocking gate at the power supply board, causing PVDD voltage to be too high. For most applications, PSVC Hi-Z must remain disabled.

The function of D4 to D7 is not covered in this document, see Reference 1.

2.4 Programming the TAS5508 for PSVC

The TAS5508 modulator has a PWM output for the power supply control. This provides an easy implementation of the PSVC. The modulator does all calculations to get the correct volume setting and generates the PSVC PWM pulse required at a frequency of 44.1 kHz or 48 kHz, depending on the audio sample rate.

The TAS5508 can be configured to provide PSVC with 12.04-dB, 18.06-dB, or 24.08-dB attenuation of the power supply. The attenuation level should be selected as high as possible. The limiting factor is that the power supply must remain stable at all power levels. Some power supplies can have difficulties when regulating over a wide voltage range. Hence, the PSVC range must be selected smaller.

The PSVC control range is set in register 0xDF.

Table 2. PSVC Range Register (0xDF)

D31 – D2		D1	D0	Function
0	0	0	0	12.04-dB control range for PSVC
0	0	0	1	18.06-dB control range for PSVC
0	0	1	0	24.08-dB control range for PSVC
0	0	1	1	Ignore – retain last value
0	0	1	0	Default Setting

Subwoofer configuration must be selected. In case that the subwoofer output is a line output, the digital volume setting is not to be affected when setting the power supply volume.

This is done in register 0xE0. This register also enables/disables the PSVC.

Table 3. General Control Register (0xE0)

D31 – D4	D3	D2	D1	D0	Function
0		-	0		/8 Channel Configuration
0		-	1		6 Channel configuration
0		0	-		Power Supply Volume Control Disable
0		1	-		Power Supply Volume Control Enable
0	0	-	-		Subwoofer Part of PSVC
0	1	-	-		Subwoofer Separate from PSVC
0	0	0	0	0	Default Setting

The D1 bit is used to select between eight channel configuration and six channel configuration. This item is not covered in this document.

The D2 bit is used to enable/disable PSVC. Default is disabled. When PSVC is disabled, the output of PSVC is 0. All volume control is performed using digital gain only. Enabling of the PSVC starts the PSVC PWM. The TAS5508 automatically calculates the volume setting for the power supply and digital volume for all channels based on the flow chart shown in Figure 3.

If D3 is set to 1, the subwoofer channel (channel 8) is not included in the PSVC, only digital volume is used. This is needed if the subwoofer output is a line out (e.g. a 7.1 system using active subwoofer).

3 Power Supply Implementation

3.1 TAS5508 0% Duty Cycle Handling

As discussed in the previous section, the TAS5508 during start up and error recovery has a PSVC output of 0% duty cycle. The power supply must then be able to handle this situation properly. When the reference voltage to the power supply is 0 V, PVDD will also be 0 V if no special arrangements are made.

NOTE: Texas Instruments power stages can handle PVDD being 0 V, since no audio is present during these events. Texas Instruments power stages does not need protection against PVDD = 0 V. However, the power supply must not be damaged nor become unregulated during these events.

If the power supply cannot handle a 0-V output, the following arrangements can be made:

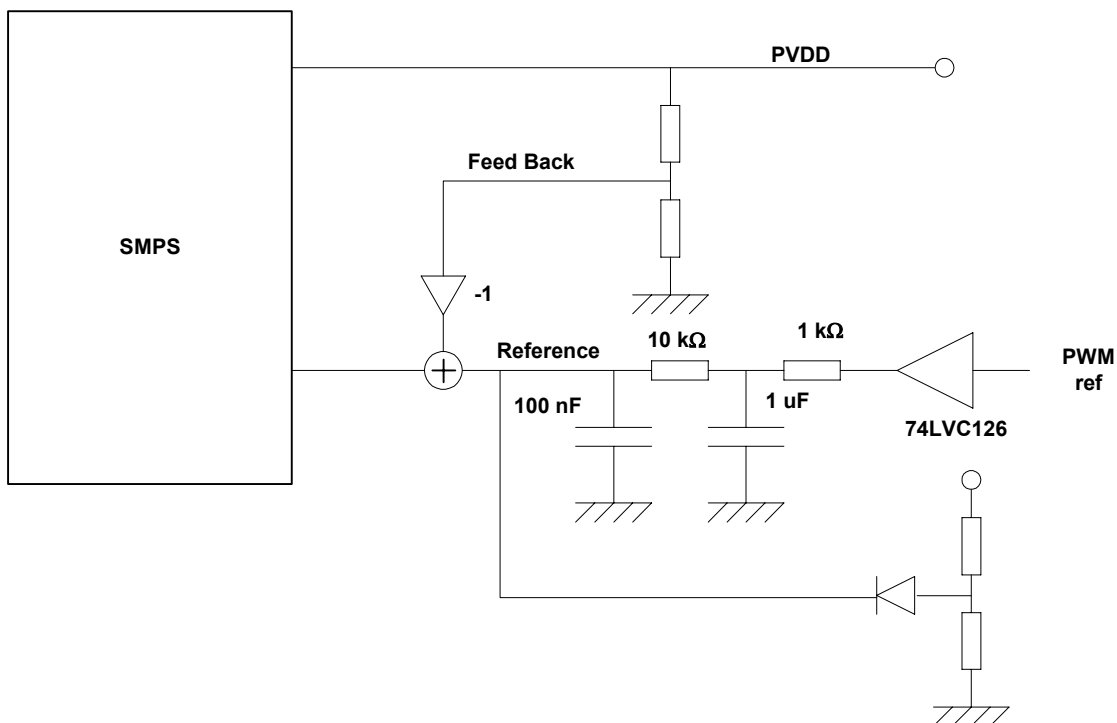


Figure 8. PSVC With Saturation

Figure 8 shows a power supply implementation, where PVDD is kept at a minimum voltage when PWM is 0%. The voltage is set by a resistor divider and the forward drop of the diode.

Another way of controlling 0% situation is to shut down the power supply when the duty cycle falls below a given level. This is shown in Figure 9.

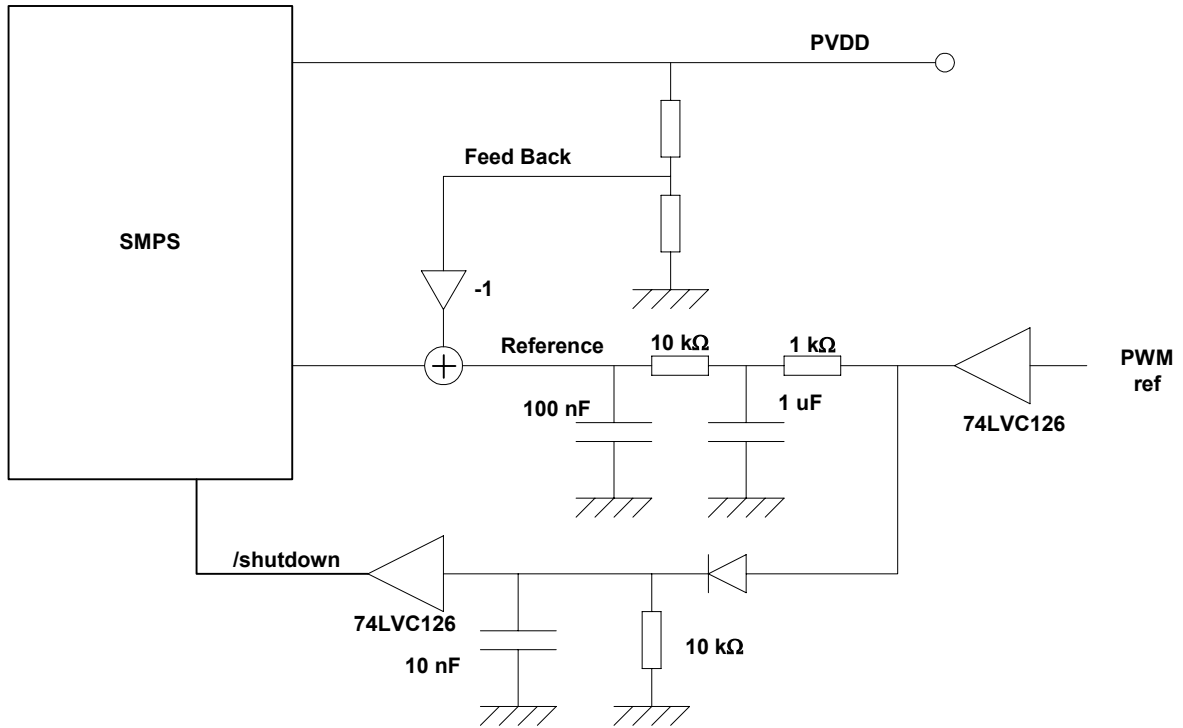


Figure 9. PSVC With Shutdown

3.2 Power Supply Sink / Source

Most power supplies are only capable of sourcing current. This is due to implementation of the rectifying circuit on output. In most cases, this is done by using a rectifying diode.

Figure 10 shows basic components for a buck converter. The buck converter creates an output voltage (PVDD) lower than its input voltage (V_I). It can be seen that current can only flow out of the converter due to the direction of the diode and since the input voltage is higher than the output voltage, no current can flow from the PVDD to V_I . Decreasing of the output voltage can only happen by loading the output.

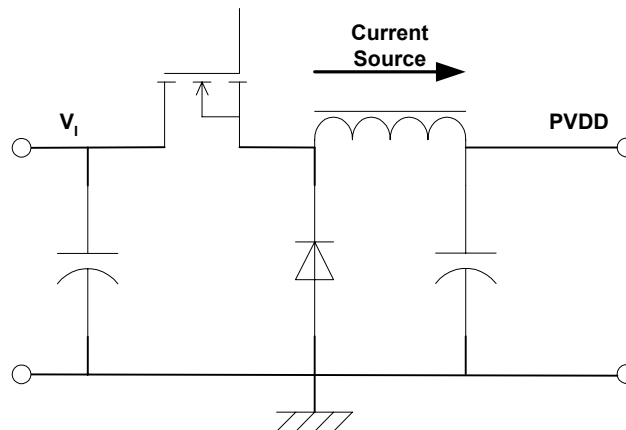


Figure 10. Basic Schematic for a Buck Converter

When using PSVC, this can cause a problem when ramping down volume. When the volume is ramped down, the PVDD voltage must decrease. If the power supply can only source current, only the amplifier load can decrease the PVDD voltage. This causes an uncontrolled ramp down of the volume.

To make the power supply able to sink current as well, one of following solutions is recommended.

Use of synchronous rectification. The basic theory is to replace the rectifying diode with a controlled MOSFET. A controlled MOSFET has the advantage to allow current in both directions when turned on. Actual implementation of a synchronous rectification depends on the power supply topology. Figure 11 shows an example of synchronous rectification for a buck converter.

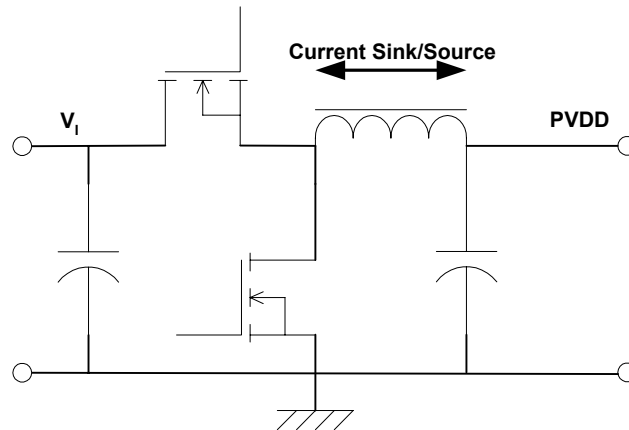


Figure 11. Buck Converter Using Synchronous Rectification

Use of bleeder resistor. A resistor can be placed at the PVDD output to bleed down the output voltage. In order not to decrease efficiency, this resistor must be connected through a switch or a transistor. The bleeder resistor will then only be active when needed.

Figure 12 shows how a controlled bleeder resistor can be used to decrease the output voltage. The bleeder resistor is turned on by the switch when the PVDD voltage is too high.

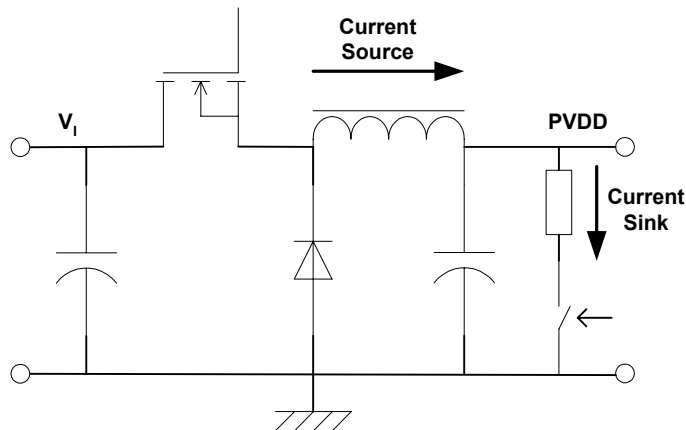


Figure 12. Use of a Bleeder Resistor to Sink Current

4 DC/DC Converter Application Example

The following application example is a dc/dc converter optimized for the full advantage of the TAS5508. The converter is designed for:

- Input voltage 50 V to 55 V
- Output voltage 2 V to 40 V, giving the full 24.08-dB attenuation provided by the TAS5508
- Current limitation level set to 12 A

4.1 Implementation

The power supply is designed with the possibility to use remote voltage sensing, which improves audio performance, see Reference 2. The output voltage is sensed through a separate connector J704 pin 2. The voltage can then be sensed at the amplifier board eliminating impedances in wires and connectors.

For using the PSVC, a jumper must be placed at J703 between pin 1 and pin 2. If a manual voltage setting is required, the jumper must be placed between pin 2 and pin 3.

The PWM input for power supply control from the TAS5508 is at J703 pin 5. The input has a pulldown resistor, R827, to insure that the output voltage drops to 0 V in case of loss of PWM input. To restore the PWM signal and adapt it to the power supply reference voltage, the PWM input is reclocked in an AND-gate, U703. This removes voltage drops and noise that might have been injected in the transmission from the modulator to the power supply. Converting the PWM signal level to the power supply reference voltage improves the accuracy of the output voltage.

The converter itself is a BUCK topology. Basic components can be identified as: C708, C710, C711, and C712 as the input capacitor, Q706 and Q707, L704 and C725 plus capacitors at the amplifier board as the output capacitor. U706 is an integrated power supply controller.

Synchronous rectification is used in this application. Q707 is the synchronous rectifier instead of a diode. The dc/dc converter is then capable of transferring current from output side to the input side.

Since the dc/dc converter can be supplied from a rectified transformer output, there must be a bleeder at the primary side, to be able to sink current. The bleeder resistor is R707 and is controlled by Q701. Q701 is turned on by U701C, if the input voltage exceeds 65 V.

References

1. TAS5508 – 8 Channel Digital Audio PWM Processor (SLES091)
2. Power Supply Considerations for A/V Receivers (SLEA028)

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