Initializing the TVP5145 Video Decoder

Digital Video & Imaging

1 Overview

This document defines the initialization process required for the TVP5145 Video Decoder. It discusses the strapping terminals, the power up and reset requirements, starting the microprocessor, and initializing the internal registers.

1.1 Scope

This application note pertains only to the initialization of the TVP5145. Information on required software or application circuits is not within the scope of this application note. See *Section 7: References* for a list of application notes that may provide this information.

1.2 Description of the TVP5145 Video Decoder

The TVP5145 is a high performance, digital video decoder that converts base-band analog NTSC, PAL and SECAM video into digital component video. It supports analog component, composite and S-video inputs and utilizes two 10-bit ADCs. The supported output formats include 8-bit, 10-bit, 16-bit 4:2:2 YCbCr or 8-bit, 10-bit ITU-R BT.656. The available sampling rates are square-pixel or ITU-R BT.601.

The TVP5145 also utilizes Texas Instruments' patented technology for locking to weak, noisy, or unstable signals. These algorithms and many other functions are executed from internal ROM by an embedded microprocessor. Unlike previous TI video decoders, microcode download is not required to operate the TVP5145.

Depending on the user's system requirements, it may be necessary to initialize the internal registers. Access to the internal registers is provided via the host port interface, I2C or PHI (three modes).

2 Initialization Sequence

The initialization sequence of the TVP5145 consists of four steps:

1. Strapping Terminals
2. Power up and Reset
3. Microprocessor Start
4. Register Initialization

3 Strapping Terminals

The states of the terminals in Table 1 and Table 2 are sampled at power up or at the trailing edge of RSTINB and are used to configure the TVP5145 for various modes of operation. These terminals return to their normal operation after reset.

The states of the terminals in Table 1 are used to determine the clock and sync output states during and after reset. These terminals have a weak internal pull-down resistor which establishes a default low state during power up and reset. The user may use a 10-kΩ pull-up resistor to establish a high state on these terminals during power up and reset.

Table 1. Strapping Terminals for Clocks and Syncs

Terminal Name	Terminal Number	Description
AVID	28	0 = Y[9:0], UV[9:0], HSYN, VSYN, AVID, PALI, and FID outputs are high-impedance* 1 = Y[9:0], UV[9:0], HSYN, VSYN, AVID, PALI, and FID outputs are enabled* *during and after a power up or reset
PREF	26	0 = SCLK and PCLK outputs are high-impedance** 1 = SCLK and PCLK outputs are enabled** **during and after power up or reset

Note: While RSTINB is asserted low, these configuration pins must not be driven by external logic.

Table 2 shows the strapping terminals required for host port selection. These terminals do not have internal pull-down resistors. It is necessary for the user to use either a 10-kΩ pull-up or a 10-kΩ pull-down resistor on each terminal in order to select the desired host port configuration.

Table 2. Strapping Terminals for Host Port Selection

GLCO Pin 31	PALI Pin 32	FID Pin 33	Function Selected
0	0	1	I2C Host Port Enabled
1	0	1	PHI Host Port Mode A
1	1	0	PHI Host Port Mode B
1	1	1	PHI Host Port Mode C

Note: The system design must ensure that the crystal-generated clocks are oscillating before the end of the RSTINB pulse. This is required for the power-up configuration pins to be sampled correctly.

4 Power up and Reset

The TVP5145 is in a stable operating mode when the digital power supply, DVDD, reaches 3.0V. By design, the TVP5145 utilizes an internal power on reset circuit that holds the device in reset for 128 pixel clocks once DVDD reaches 3.0V.

It is recommended though that RSTINB, pin 23, be asserted low for roughly 1us to ensure proper initialization of the TVP5145.

Table 3 below shows the state of the I/O pins during and after a reset.

Table 3. Initial Power up Sequence

Pin Name	During Reset	Reset Completed
Y[9:0], UV[9:0], HSYN, VSYN	High impedance if AVID is pulled down during reset. Active output if AVID is pulled up during reset.	High impedance if AVID is pulled down during reset. Active output if AVID is pulled up during reset.
FID, PALI, AVID	Input	High impedance if AVID is pulled down during reset. Active output if AVID is pulled up during reset.
SCLK, PCLK	High impedance if PREF is pulled down during reset. Active if PREF is pulled up during reset.	Active Output
PREF	Input	Active Output
GLCO	Input	Active Output
D[7:0]	Input	High Impedance
A[1:0] in PHI mode	Input	Input
RSTINB, VC0(SCL), VC1(SDA), VC3(I2CA), OEB, GPCL	Input	Input

5 Microprocessor Start

The TVP5145 incorporates a proprietary microprocessor that performs many device functions including PLL operation, AGC, sync configuration, and register configuration.

On power up, the microprocessor is disabled to prevent the output of invalid video data. After a hardware reset, any register other than 7Eh must be written with any data in order to start operation of the TVP5145. This will start the microprocessor and begin normal operation of the TVP5145. Register 7Fh is recommended for this purpose.

6 User Register Initialization

After the microprocessor has been enabled, the TVP5145 internal registers are initialized to the default values as specified in the *TVP5145 Data Manual* (SLES029).

Register initialization may take place as soon as 5ms after the start of the microprocessor.

For I2C host interface based applications, the timing mechanism must be supplied. While with PHI host interface based applications, the TVP5145 generates an interrupt indicating it is ready for register initialization.

The following register settings are recommended for an auto-switch configuration.

1. Microprocessor Start - write any data to I2C register 7Fh.
2. Input Channel Selection - the default input channel is VI_1A. No register settings are required unless a channel other than the default is used. †
3. Sampling Rate - the default sample rate is ITU-R BT.601. No register settings are required unless the square pixel sampling rate will be used. †
4. Output Format Selection - the default output format is 20-bit 4:2:2 YCbCr. No register settings are required unless another output format will be used. †

† See the TVP5145 Data Manual for the complete registers definitions.

7 References

For more information on the TVP5145, refer to the following documents:

1. *TVP5145 Data Manual* (SLES029)
2. *TVP5145 Using the I2C Host Port Interface* (To Be Determined)
3. *TVP5031/5040/5145EVM User's Guide* (SLAU078)

8 Technical Support

For technical support, please visit www.ti.com/sc/support.

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