

TAS5825M Advanced Features

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ABSTRACT

This application report explains a few TAS5825M advanced features in details. Thermal foldback smoothly attenuate the audio output to keep the TAS5825M output stage within its safe power dissipation limit to avoid unexpected shutdown. The PVDD sensing avoids speaker output clipping when the supply voltage varies, and the Hybrid modulation dynamically minimizes the power consumption without compromising audio performance, making the TAS5825M suitable for battery-powered audio systems such as Smart speakers and Bluetooth speakers.

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1 Thermal Foldback

Thermal Foldback is a power limiting feature (a type of thermal protection). The prime purpose of foldback power limiting is to keep the output stage within its safe power dissipation limit to avoid unexpected OTSD (Over-Temperature Shutdown)

The audio DSP core of the TAS5825M monitors junction temperature continuously in real-time to ensure safe operations. The TAS5825M can warn the host if junction temperature is approaching the OTW (Over-Temperature Warning) limits. The OTW has four different temperature thresholds. Each threshold is indicated in I2C register 0x73 bits 0, 1, 2 and 3.

The TAS5825M still functions until the temperature reaches the OTSD threshold, at which time the amplifier outputs are shut down. As the junction temperature rises above the threshold of set by OTW, the thermal foldback circuit initially activates. It ensures a smooth audio response and allows for uninterrupted music playback when OTW limits are crossed. That means the TAS5825M will not simply shut down, but continue to operate with considerable music output power to avoid triggering OTSD.

The following figures show a few examples of Thermal Foldback performance using different configurations. Test conditions are

1. PVDD = 24V
2. No load connected
3. 155°C air from a thermal stream is used to heat up the TAS5825M device and 25°C air to cool it down

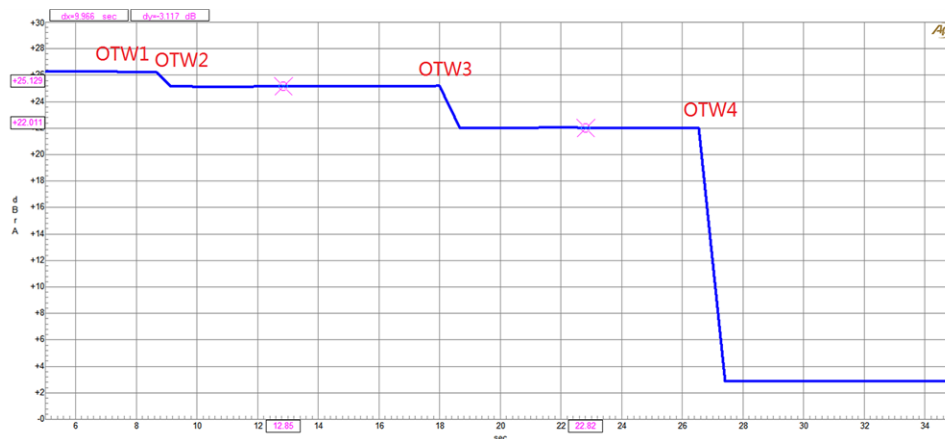


Figure 1. Thermal Foldback Example 1: Attenuation Applied with Default Settings

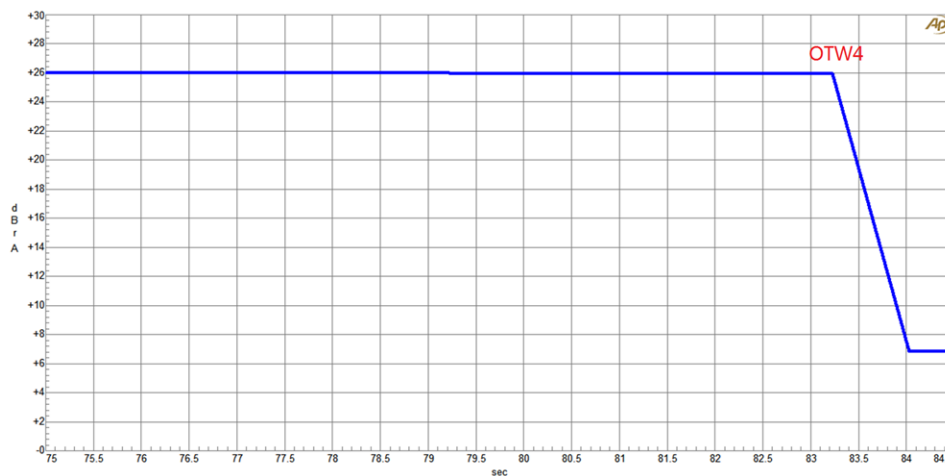


Figure 2. Thermal Foldback Example 2: Attenuation Applied with TAS5825M Configured to only Respond to OTW Level 4

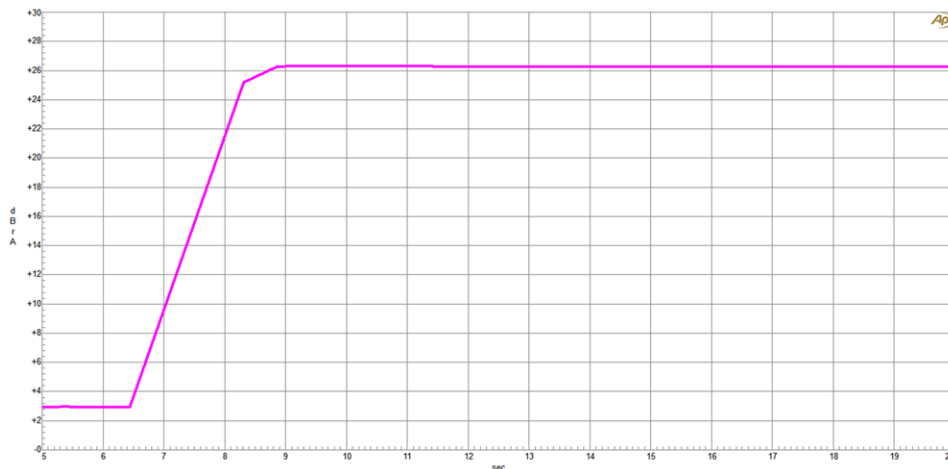


Figure 3. Thermal Foldback Example 3: Attenuation Removed with Default Settings

2 PVDD Sensing

The PVDD sensing applies smooth compression to maintain consistent dynamic range when the supply voltage (PVDD) varies. This feature is quite useful in the following two scenarios.

1. Customers have the volume turned up too high.
2. PVDD voltage drops due to battery discharging but the input signal still stays same amplitude.

An 8-bit PVDD supply voltage ADC enables the PVDD sensing circuit. Its output provides the necessary inputs to calculate the amount of compression that needs to be applied to signal peaks. In addition, the PVDD ADC results can be read back via I2C through the PVDD_ADC Register located at 0x5E. Refer to the TAS5825M datasheet for more detailed descriptions of this register.

The PVDD sensing has two functional modes, depending on the measured value of supply voltage (PVDD).

Mode 1: If PVDD voltage is greater than maximum peak output voltage (MPOV), no action will be taken by the PVDD sensing circuit since there is still sufficient headroom for the amplifier to reproduce the audio signals up to 0 dBFS;

Mode 2: If PVDD voltage is less than MPOV, the PVDD sensing circuit will reduce gain to ensure that signals can fit within the available PVDD voltage to avoid clipping.

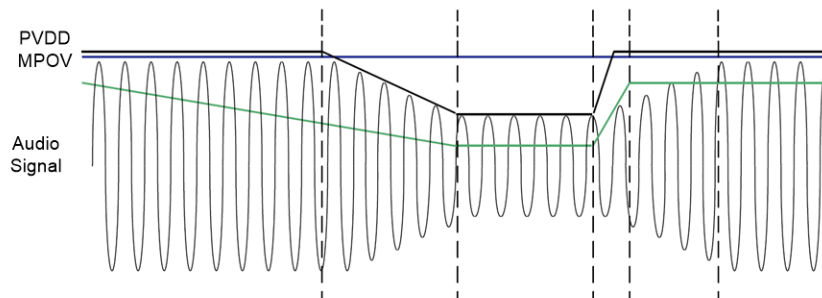


Figure 4. PVDD Sensing Example

3 Hybrid Mode

Traditional Class-D amplifiers use a fixed output duty cycle for all signal levels. However, a fixed 50% duty cycle of common mode (known as BD modulation) suffers a big idle loss.

In a typical audio application using external LC filters, the peak ripple current can be expressed using Equation 1.

$$I_{Rip,peak} = duty \cdot P_{VCC} / (2 \cdot f_s \cdot L) \tag{1}$$

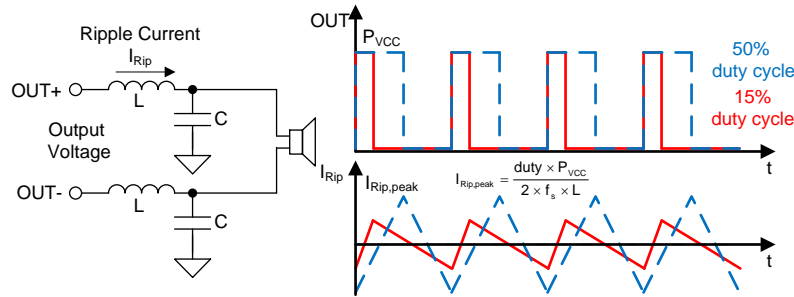


Figure 5. Peak Ripple Current

Where P_{VCC} is the power supply voltage, f_s is the switching frequency, L is the inductance of the LC filter. In order to decrease system power loss, a larger external filter is required, which would add BOM cost and board space as well. A low duty cycle (such as fixed 15%, 1SPW modulation) helps to decrease the idle loss but causes a slight penalty in THD degradation when output power is high.

Hybrid mode is an innovative modulation scheme, which has been designed to reduce system power loss without using large expensive inductor and still maintain good THD+N performance at the same time. This method can effectively increase efficiency at a low cost.

The principle of Hybrid mode is to dynamically adjust the output duty cycle according to input signal levels and power voltage levels. As Figure 6 shows, when input signal levels are high, the output duty cycle stays at 50% just like the BD modulation. When input signal levels are low, the output duty decreases gradually. Finally, the output duty becomes 10% when the input is idle.

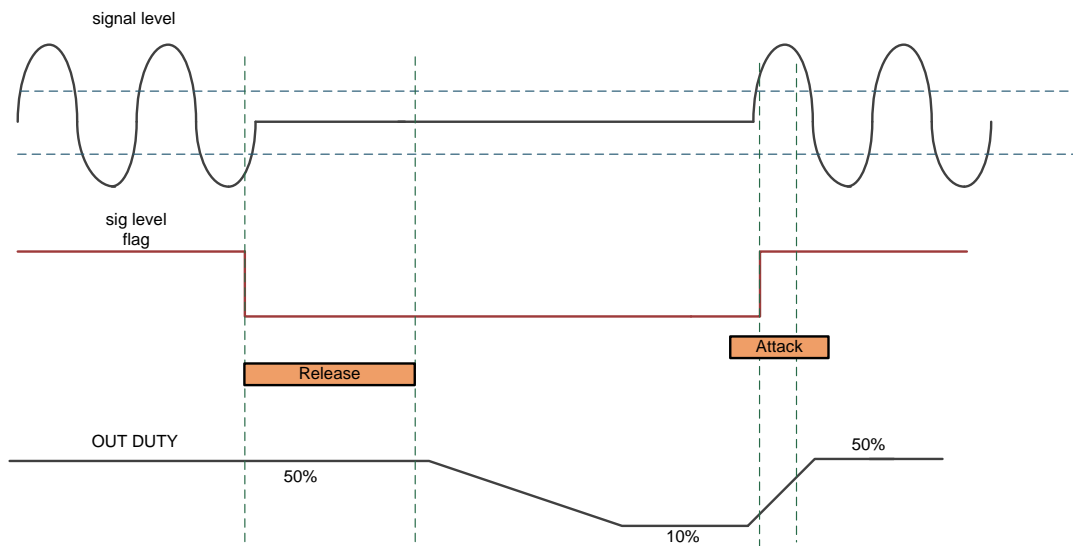


Figure 6. Hybrid Mode

The biggest benefit of Hybrid mode is to save power. Figure 7 shows a real life example of different power consumption in Hybrid mode and BD mode. Basically, the operation time of a battery powered system can be extended quite a bit if the Hybrid mode is enabled.

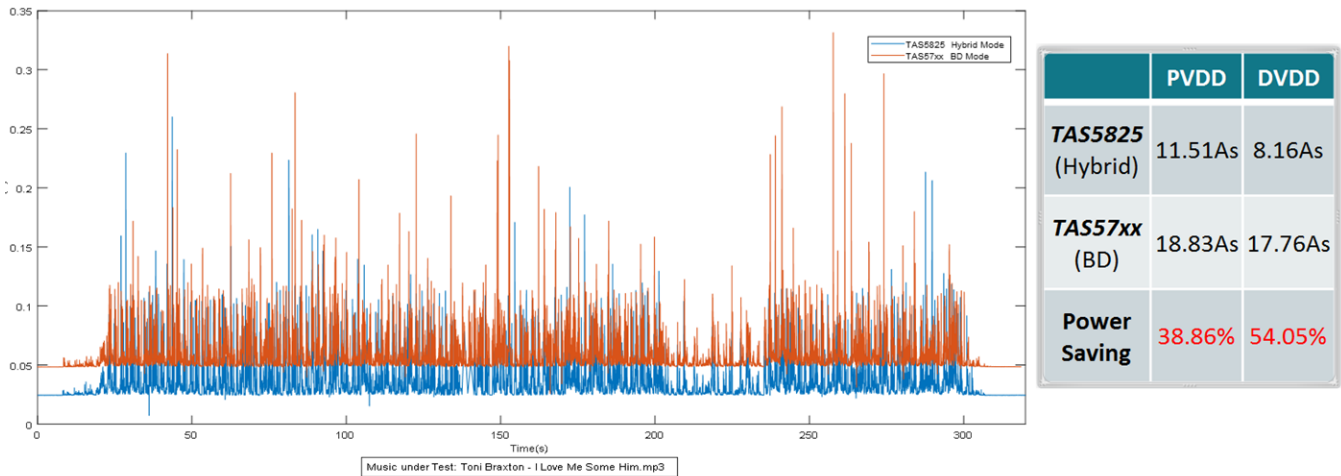


Figure 7. Hybrid Mode vs BD Mode

Another is much lower idle current than that in the BD mode. See Figure 8 below for comparisons of idle current in 3 different modulations schemes.

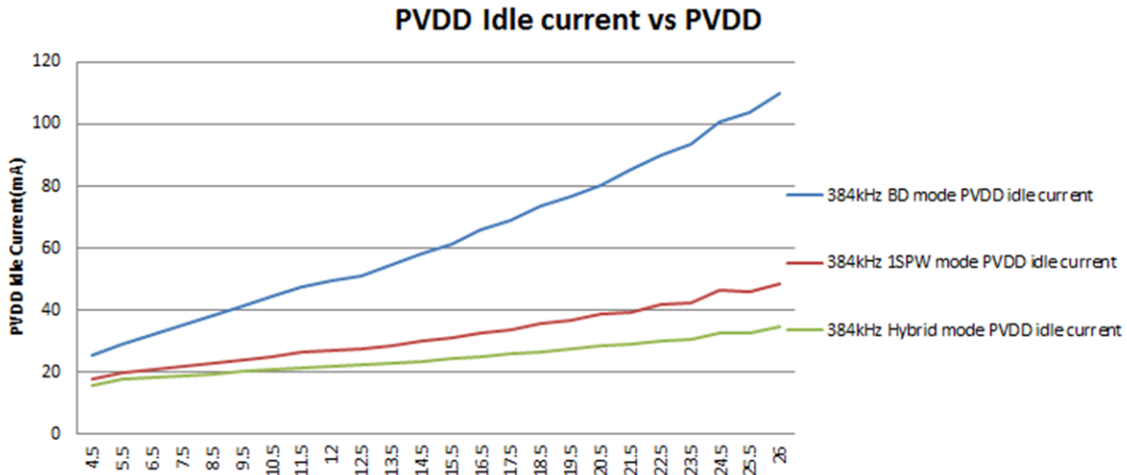


Figure 8. Comparisons of Idle Current vs PVDD in BD, 1SPW and Hybrid Modes (Load = 6Ω, LC filter =10μH + 0.68μF)

A third advantage is the much better THD+N performance than that in the 1SPW mode. Figure 9 show the THD+N vs output power in the BD, 1SPW and Hybrid Modes.

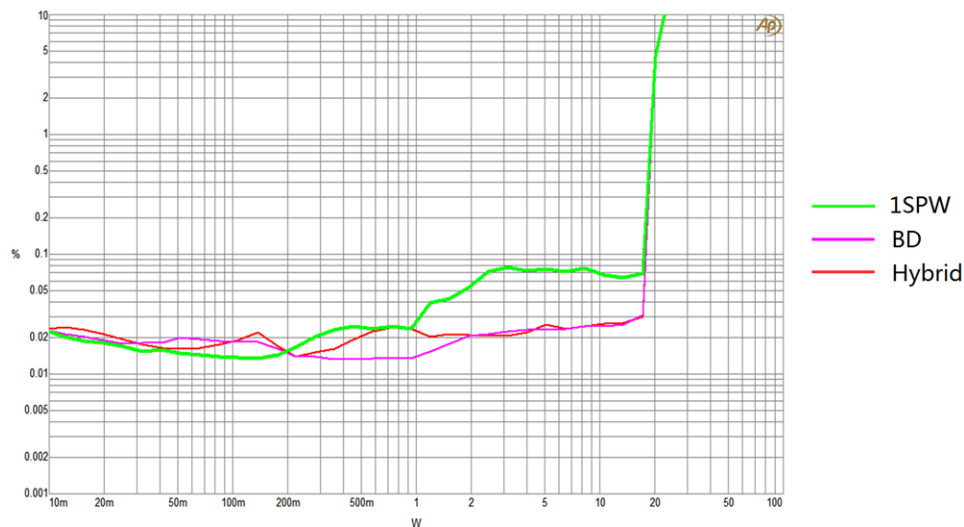


Figure 9. Comparisons of THD+N vs Output Power in BD, 1SPW and Hybrid Modes (PVDD = 18V, Load = 8Ω)

4 FAQ

4.1 Thermal Foldback

4.1.1 Is the thermal foldback feature available in all process flows?

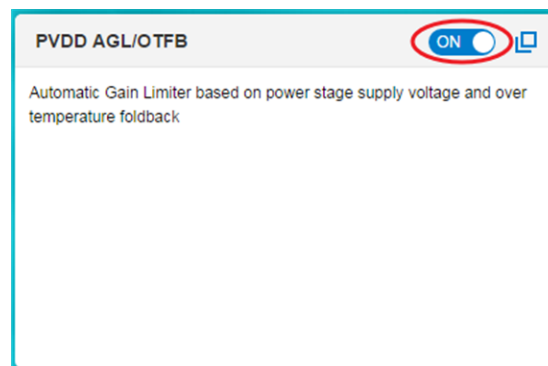
No. It is only available in a few process flows. At the time of writing, the following process flows can support the thermal foldback feature:

- FIR (2.0, 48 kHz)
- Base/Pro (2.0, 48 kHz)
- Housekeeping (2.0)
- Base/Pro Hybrid (2.0, 48 kHz)

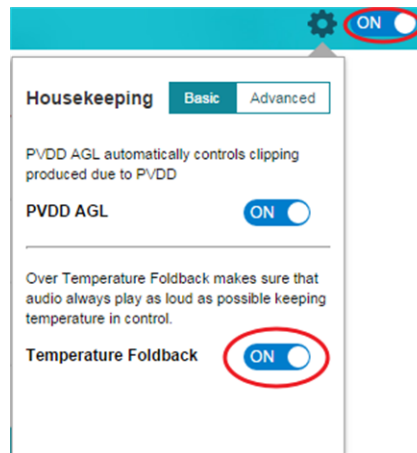
4.1.2 How to enable / disable the thermal foldback feature?

Step 1: Make sure the process flow you select supports the thermal foldback feature.

Step 2: Make sure the ON/OFF button is switched to ON in the PVDD AGL/OTFB tab after going into the Tuning and Audio Processing window.



Step 3: Click the icon next to ON/OFF button on the top right corner after going into the PVDD/AGL/OTFB tuning window. Toggle the ON/OFF button next to the “Temperature Foldback” label to enable or disable thermal foldback.



4.2 PVDD Sensing

4.2.1 Is the PVDD sensing feature available in all process flows?

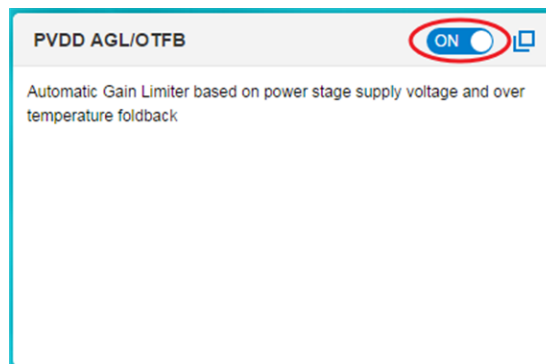
No. It is only available in a few process flows. At the time of writing, the following process flows can support the PVDD sensing:

- FIR (2.0, 48 kHz)
- Base/Pro (2.0, 48 kHz)
- Housekeeping (2.0)
- Base/Pro Hybrid (2.0, 48 kHz)

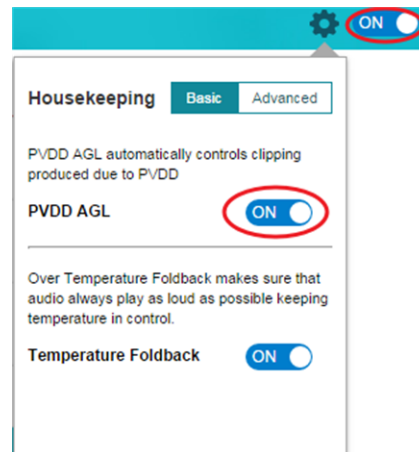
4.2.2 How to enable/disable the PVDD sensing feature?

Step 1: Make sure the process flow you select supports the PVDD sensing feature.

Step 2: Make sure the ON/OFF button is switched to ON in the PVDD AGL/OTFB tab after going into the Tuning and Audio Processing window.



Step 3: Click the icon next to ON/OFF button on the top right corner after going into the PVDD/AGL/OTFB tuning window. Toggle the ON/OFF button next to the “PVDD AGL” label to enable or disable the PVDD sensing.



4.2.3 Is the PVDD voltage sensed by TAS5805M can be read back by host processor via I2C?

Yes. The internal PVDD ADC results can be read back via I2C through the PVDD_ADC Register located at 0x5E. Refer to the [TAS5825M](#) datasheet.

4.3 Hybrid

4.3.1 Is Hybrid available in all available process flows?

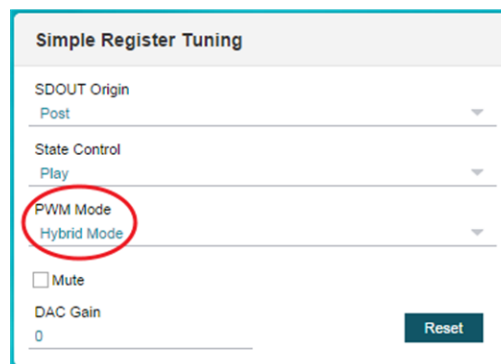
No. The hybrid modulation scheme is only available in a few process flows. At the time of writing, hybrid mode is supported by the following process flows:

- Housekeeping (2.0)
- Base/Pro Hybrid (2.0, 48 kHz)
- Base/Pro Hybrid (1.1, 48 kHz)
- Base/Pro Hybrid (2.1, 48 kHz)
- 2-Band DRC&AGL Hybrid (2.0, 48 kHz)

4.3.2 How to enable the hybrid mode?

Step 1: Make sure the process flow you select supports the hybrid mode.

Step 2: Select the Hybrid mode in the Simple Register Tuning tab after going into the Tuning and Audio Processing window.



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