SimpleLink™ MSP432P4 – Low-Power 2MB MCU

Introduction

Microcontrollers in industrial applications need ever-growing amounts of storage as they evolve from simple single-purpose designs to more complex systems with multiple interfaces, wireless protocols, LCDs with multiple languages and graphics features, and extensive measurement and data logging capabilities. Yet, the system power budget has not increased along with the growing memory and peripheral needs. Ultra-low-power capabilities are therefore vital to maintain small form factors and to enable these feature-rich devices to be powered from batteries or current loops, further reducing costs by eliminating the need for separate cabling.

The MSP432P4111 microcontroller (MCU) offers the active and standby power features as well as the performance specifications needed to meet these demanding requirements. This document describes these features and how to use them to get the lowest possible power for any given application.

Table 1. MSP432P4111 Low-Power Specifications

Mode or Feature	Typical Specification
CPU-Active	100 µA/MHz
CPU-LPM0	960 µA
CPU-LPM3 w/ RTC	820 nA
CPU-LPM4	690 nA
CPU-LPM4.5	22 nA
Low-Power Precision ADC	385 µA At 1 Msps
RAM Retention	30 nA / 8KB block

Implementing Low Power On MSP432P4 Devices

The MSP432P4 has many low-power capabilities that can be leveraged to dramatically reduce system power. These include advanced power management, ultra-low power peripherals and memory hierarchy. The first and most impactful features to consider are those that affect the active power, as shown in Table 1. This table shows that the power drawn by both the CPU and the analog blocks is a large component of overall power. These two values also indicate how much work can be done while in active mode within a given power budget constraint.

Core voltage voltage control. Referring to the familiar CV^2F equation for power, it is evident that the core voltage for the digital logic is a primary driver of overall power consumption during active modes. The core voltage also impacts the available CPU frequency, which should be set to the minimum necessary to meet the application requirements.

Table 2. Tradeoffs Between Maximum Frequency and Active Power

Mode	VCORE0	VCORE1
	At f_{MAX} = 24 MHz	At f_{MAX} = 48 MHz
LDO	4000 µA	7300 µA
DCDC	2390 µA	4650 µA

In a typical 3.3-V system, the input voltage to an MCU has a range of >1 V (V_{DD} = 2.6 V to 3.6 V), so an internal regulator is provided to create the constant 1.2-V (typical) voltage used by the digital logic. A low-dropout regulator (LDO) is common in MCUs due to its simple design and low start-up requirements. However, as Table 2 shows, the DC-DC converter in the MSP432P4 MCU consumes far less current than the LDO at the same internal voltage (VCORE0 or VCORE1). Table 2 also highlights the power savings of a lower operating voltage and frequency. Example 1 (an excerpt from the pcm_active_dcdc_dco sample code) shows how to set the voltage and flash wait states to accommodate a 6-MHz core system clock using the lower (VCORE0) core voltage.

Example 1. Clock- and Voltage-Selection DriverLib APIs

```
// Settings for 6MHz operation internal DCO
// and DCDC usage
MAP_PCM_setPowerState(PCM_AM_DCDC_VCORE0);
MAP_FlashCtl_A_setWaitState(FLASH_A_BANK0, 0);
MAP_FlashCtl_A_setWaitState(FLASH_A_BANK1, 0);
MAP_FPU_enableModule(); // For DCO Freq Calc
MAP_CS_setDCOCenteredFrequency(CS_DCO_FREQUENCY_
6);
/* Set MCLK = DCO = 6MHz */
MAP_CS_initClockSignal(CS_MCLK,
CS_DCOCLK_SELECT, CS_CLOCK_DIVIDER_1);
```

Analog Active Power

When selecting an MCU, analog functions and their associated power must be considered separately from the digital logic, as their power does not scale with the core voltage. Achieving high-precision analog conversions at a high sampling rate with low noise often translates to high system power despite the best efforts on containing power on the digital side. For this reason, the MSP432P4 devices include a high-precision ADC with a low ENOB that supports up to 16-bit conversions. These features, coupled with converter power that requires only 490 µA at 1 Msps, enables more frequent and higher-accuracy data collection without sacrificing the overall power budget.

Static Power Management

In most embedded applications, the MCU spends a large percentage of time in a sleep mode. The next few sections address methods to maximize the use of the low-power modes shown in Table 1 to minimize overall power.

Wake-up sources. While the CPU and memories (or any component) is powered, leakage power is greatly increased. To ensure that an application spends as little time as possible performing the required tasks before returning to a low-power sleep mode, Arm® CPUs have a *SleepOnISRexit* control (see Example 2). This control automatically returns the device to the previous sleep mode before the interrupt-triggered wakeup, without the need for CPU intervention after the interrupt service routine.

Example 2. Lowest-Power Sleep Mode Settings

```
// Force sleep mode regardless of Clk requests
MAP_PCM_enableRudeMode();
// Enable Sleep on ISR Exit
MAP_Interrupt_enableSleepOnIsrExit();
```

Because the device spends much of the time in a low-power mode waiting for an interrupt, it is important to have a rich array of wake-up sources to handle a variety of events including periodic measurements from the ADC, fault conditions triggers from a comparator, incoming serial communications events, or timer events. All of these wakeups can occur even from deep sleep modes (LPM3 or LPM4), which lets the device fully leverage these lowest-power states. Table 3 lists the peripherals of the MSP432P4111 MCU that support wake-up sources.

Table 3. Peripherals With LPM3 and LPM4 Wake-up Sources

Peripheral	LPM3	LPM4
eUSCI_A	Yes	Yes
eUSCI_B	Yes	Yes
Timer_A	Yes	Yes
Comparator_E	Yes	Yes
ADC14	Yes	No
LCD	Yes	No
Real-Time Clock	Yes	Yes
Watchdog Timer	Yes	Yes
GPIO Pins	Yes	Yes

Transition latencies. Deeper sleep modes mean lower power, but they also result in more components being placed in low-power retention states or powered down altogether. This increases the time needed to restore the CPU, clocks, memories, and peripherals to an active state. Another consideration is that longer power transition latencies can also result in lost data if the device cannot power up quickly enough to process incoming serial communications. Having an MCU with low transition latencies is important to fully leveraging the low static power that it offers. Table 4 summarizes the tradeoffs between power and entry or exit times for the LPM low-power modes on the MSP432P4111 MCU.

Table 4. LPM Mode Transition Latencies and Power (Typical, at 25°C)

Mode	Entry Time	Exit Time	I_{DD} (µA)
LPM0	1 MCLK cycle	4 MCLK cycle	77.0
LPM3 (with RTC)	60 µs	9 µs	0.82
LPM4	60 µs	9 µs	0.69
LPM4.5	60 µs	9-1200 µs	0.02

SRAM retention and block enable granularity. SRAM memories can be a significant consumer of standby power. Whenever possible, SRAM banks should be powered down or placed in a low-power state that retains data when the MCU is in a LPM mode. For devices with large amounts of SRAM, having a memory structure that provides SRAM-enable and memory retention at a fine level of granularity allows the selection of just the right amount of data retention with little wasted power. For the MSP432P4111 with 256KB of total SRAM, memory retention can be controlled at the 8KB block size. Example 3 shows the API that enables block retention control without keeping track of block sizes or locations. The only required parameters are start and end addresses. An alternate approach is also shown that directly accesses the system control register.

Example 3. SRAM Memory Retention Control

```
// Disable SRAM retention for SRAM blocks
SysCtl_A_enableSRAMRetention(startAddr,endAddr);
 Or, for direct register-write
// Disable all SRAM blocks except top (stack)
//  and bottom (Blk0, for variables).
SYSCTL_A->SRAM_BLKRET_CTL0 = 0x80000001;
```

GPIO and system resources. Setting GPIOs to the proper state is perhaps one of the simplest and most important power-saving measures. Unused I/Os should be configured as outputs and driven to ground to avoid floating nodes on transistor inputs and the associated high flow-through current on device input buffers that could result. For further device power savings, system resources such as voltage monitors can also be shut down for an additional reduction in power. Example 4 shows how the GPIOs and PSS (high-side power supervisor) can be set for lowest power (only one GPIO port is shown).

Example 4. GPIO and Supply Supervisor Low-Power Settings

```
// Turn off unused GPIOs (example)
MAP_GPIO_setAsOutputPin(GPIO_PORT_PA,
PIN_ALL16);
MAP_GPIO_setOutputLowOnPin(GPIO_PORT_PA,
PIN_ALL16);
// Repeat the above for each GPIO Port (A-J)
// Turn off PSS (High-side Power supervisor)
MAP_PSS_disableHighSide();
```

Software Considerations: EnergyTrace™

In any low-power application, software that leverages the power-saving features offered by the MCU plays an outsized role in minimizing the overall power footprint for the project. When designing systems with power consumption in the microamp range, even small segments of code can have a significant affect on overall power. However, at higher CPU speeds, it can be difficult to identify what portion of the application is responsible for excess current consumption, because the events in question are fleeting and typically difficult to measure without expensive dedicated equipment.

TI provides a low-cost tool called EnergyTrace™ technology that is built into select LaunchPad™ development kits to enable developers to pinpoint problem areas of code that are consuming excess current. EnergyTrace technology continually samples the energy supplied to the microcontroller to allow the visualization of even the shortest device events. This is a clear benefit over shunt-based measurement systems, which cannot detect extremely short durations of energy consumption.

The SimpleLink™ MSP432P4 LaunchPad development kits support both EnergyTrace and EnergyTrace++ technology. EnergyTrace++ technology can measure energy of a microcontroller in the same way that EnergyTrace does but also lets the developer access information about the internal state of the microcontroller. These states include the on or off status of the peripherals and all system clocks (regardless of clock source) as well as the low power mode currently in use. More information on EnergyTrace technology can be found in MSP Advanced Power Optimizations: ULP Advisor SW and EnergyTrace Technology.

References

1. Designing an Ultra-Low-Power (ULP) Application With SimpleLink™ MSP432™ Microcontrollers
2. Scaling Across the SimpleLink™ MSP432P4 MCU Family
3. MSP432P411x, MSP432P401x SimpleLink™ Mixed-Signal Microcontrollers
4. MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual

Table 5. Device Recommendations

Part Number	Key Features
MSP432P4111I	2MB Flash, Precision ADC, LCD
MSP432P4011I	2MB Flash, Precision ADC

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