

Common Noise Issues in Audio Codecs

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ABSTRACT

This application note describes methods that can be used to improve noise performance in systems using audio codecs. Noise is present in all circuit board systems; however, common design practices can help minimize overall noise contribution to improve the audio quality using audio codecs. Recommendations in this document apply to the TLV320AICxxxx, TLV320ADCxxxx, and TLV320DACxxxx audio converter families. Some information in this document may be used to reduce noise in other audio converter devices as well.

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1 Introduction

In signal processing systems, *noise* is a term used to describe a random fluctuation or an unwanted modification to a electronic system or signal. In audio applications, noise can be added to the audible signal, effecting the audio signal quality. Common design practices target eliminating or reducing noise sources to improve the overall system performance.

Noise sources vary in audio converters but there are a few ways to optimize a design. Understanding how to properly design the layout, power supplies, and internal registers to maximize performance is key for any successful audio design. The following section describes some of the common noise cases in audio codecs boards and recommendations to reduce or eliminate those cases.

2 Common Noise Issues in Audio Codecs

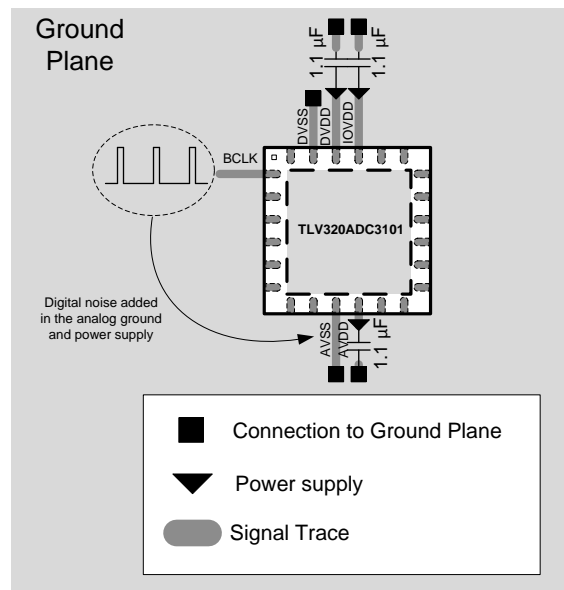
2.1 Noise Coupling Between Ground Planes

Audio converter integrated circuits (ICs) are composed of analog and digital sections. The analog section refers to the portion of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) where analog signals are either input or output. This includes programmable gain amplifiers (PGA), analog mixers, and analog inputs and outputs (I/Os). The digital section refers to all the portion of ADCs and DACs where digital signals are either input or output. This includes the digital volume blocks, processing blocks or miniDSP (if available), audio serial interface, I2C/SPI, clocks generation blocks, digital filters, and digital I/Os.

All the audio codecs are divided into an analog and digital domain, each requiring dedicated power supplies. The analog power supply in the audio codecs is called AVDD while AVSS is the analog ground. Similarly, the digital power supply in the audio codecs is normally called DVDD with DVSS as the digital ground. IOVDD is an additional digital power supply responsible for the digital I/O pins threshold values.

Digital activity can be noisy and its intensity may vary from application to application. Clock slewing and other digital line toggling can couple into the analog activity as a parasitic signal. Clocks are the principal root cause of this noise case. Its high-frequency activity generates signal content on the analog signals. This content results in high-frequency signals that may be coupled in the audible and nonaudible bands.

The noise generated from the digital lines is most prominent when all the ground pins are routed to the same plane. The TLV320ADC3101 device (see Figure 1) is taken as an example that could cause digital noise on the analog side (the rest of the traces have been removed for better comprehension).



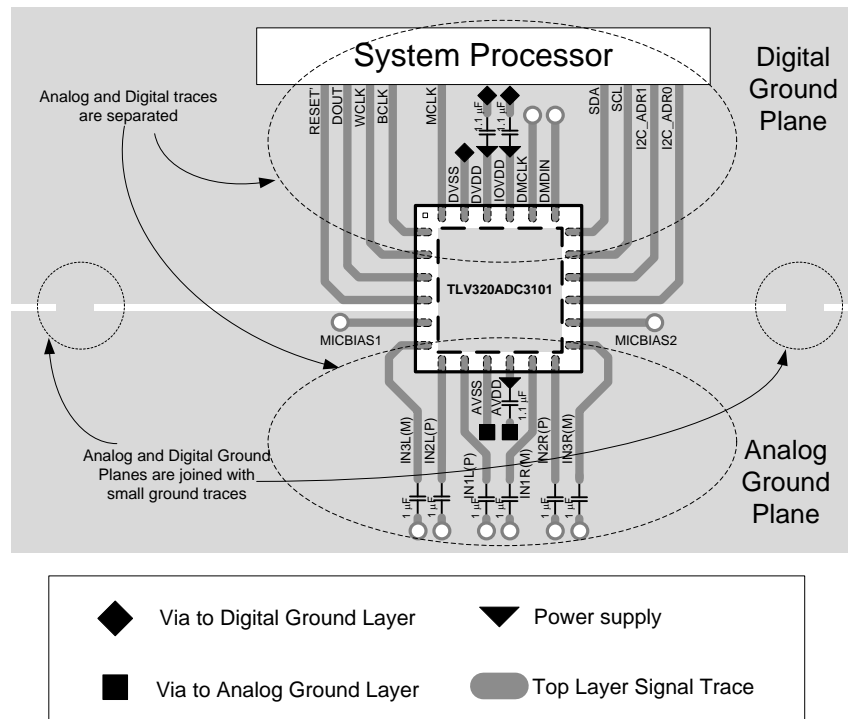
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Figure 1. TLV320ADC3101 Noise Coupling Example

To reduce digital noise on the analog side, TI recommends following these suggestions:

- Separate the ground plane into two different planes. Then, join both planes with a 0-Ω resistor or a single, small ground trace.
- Separate the digital activity from the analog activity. The digital pins and traces must be on the digital ground plane side. Similarly, analog pins and traces must be on the analog ground plane side.

The following example was taken from the [TLV320ADC3101 data sheet](#). For more details, see the Layout section of the data sheet.



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Figure 2. TLV320ADC3101 Layout

In this example, all the system processor signals and digital microphone pins are routed on the digital ground plane side. Similarly, all the analog inputs and MICBIAS pins are routed on the analog ground plane. This design provides the best performance to the application and reduces digital noise on the analog side.

2.2 Phase-Locked Loop Noise Level

TI audio codecs have frequency dividers that can be used to get the required sampling rate from an input clock. Additionally, many devices in the TI audio codec portfolio contain a programmable phase-locked loop (PLL), which can be used to get a sampling rate value from a nonstandard, audio-input, clock frequency.

Typically, external clock values with frequencies 256 times the sampling rate are selected. For example, 12.288 MHz and 11.2896 MHz are common clock values for applications that require 48-kHz or 44.1-kHz sampling rates, respectively. Using clocks with these values avoids the use of the internal PLL and, consequently, the system will consume less current.

When it is not possible to use a common clock frequency, the internal PLL is required. Each audio codec has different conditions and rules for a PLL configuration. TI strongly recommends following the PLL conditions in the data sheet. Otherwise, the noise level in the audio codec may increase.

The TLV320AIC3254 device is used as an example to get a correct PLL configuration.

The [2.7 Clock Generation and PLL](#) section of the [TLV320AIC3254 Application Reference Guide](#) describes the rules for correct PLL use. In summary, the following three rules must be respected:

- P and D values – P and D PLL values must be correctly selected to ensure that the PLL_CLKIN clock is in the correct range.
 - If $D = 0$, the value PLL_CLKIN / P is limited in a range from 512 kHz to 20 MHz.
 - When $D \neq 0$, PLL_CLKIN / P is limited from 10 MHz to 20 MHz.
- AVDD and PLL mode – In the TLV320AIC3254 device, the PLL result or PLL_CLK varies depending of the AVDD level and the selected PLL mode.
 - With a low AVDD level and low PLL mode, the PLL_CLK can be as low as 80 MHz.
 - With a high AVDD level and high PLL mode, the PLL_CLK can be as high as 137 MHz.
- Maximum clock frequencies – The TLV320AIC3254 device has limits to each internal clock. During the sampling rate calculation, the maximum frequencies must be followed to avoid conflicts. The *Maximum TLV320AIC3254 Clock Frequencies* table in the Application Reference Guide contains all the details about the maximum frequencies.

Equation 1 and Equation 2 describe an incorrect configuration.

Observe that the configuration results in a 44.1-kHz sampling rate.

$$\text{PLL_CLKIN} / P = 3 \text{ MHz} \quad (1)$$

$$\text{PLL_CLK} = \text{PLL_CLKIN} \times R \times J.D / P = 745.1136 \text{ MHz} \quad (2)$$

where:

- PLL_CLKIN = 24 MHz
- P = 8; R = 4; J = 62; D = 0928

This results in an out-of-range frequency. Under these conditions, the maximum frequency of PLL_CLK is 132 MHz.

$$\text{ADC_CLK} = \text{PLL_CLK} / \text{NADC} = 62.0928 \text{ MHz} \quad (3)$$

$$\text{DAC_CLK} = \text{PLL_CLK} / \text{NDAC} = 62.0928 \text{ MHz} \quad (4)$$

$$\text{ADC_MOD_CLK} = \text{PLL_CLK} / (\text{NADC} \times \text{MADC}) = 5.6448 \text{ MHz} \quad (5)$$

$$\text{DAC_MOD_CLK} = \text{PLL_CLK} / (\text{NDAC} \times \text{MDAC}) = 5.6448 \text{ MHz} \quad (6)$$

where:

- MADC = 11; NADC = 12; AOSR = 128
- MDAC = 11; NDAC = 12; DOSR = 128
- AVDD = 1.8 V; DVDD = 1.65 V; PLL mode = 0

$$\text{ADC_fs} = 44.1 \text{ kHz} \quad (7)$$

$$\text{DAC_fs} = 44.1 \text{ kHz} \quad (8)$$

The first and second rules previously listed are not being followed in the example leading to the wrong result. Consequently, the audio codec could generate additional noise or possibly distortion with the incorrect settings. Equation 9 and Equation 10 show an example of the correct configuration to get 44.1 kHz from 24 MHz.

$$\text{PLL_CLKIN} / P = 12 \text{ MHz} \quad (9)$$

$$\text{PLL_CLK} = \text{PLL_CLKIN} \times R \times J.D / P = 84.672 \text{ MHz} \quad (10)$$

where:

- PLL_CLKIN = 24 MHz
- P = 2; R = 1; J = 7; D = 0560

$$\text{ADC_CLK} = \text{PLL_CLK} / \text{NADC} = 16.9344 \text{ MHz} \quad (11)$$

$$\text{DAC_CLK} = \text{PLL_CLK} / \text{NDAC} = 16.9344 \text{ MHz} \quad (12)$$

$$\text{ADC_MOD_CLK} = \text{PLL_CLK} / (\text{NADC} \times \text{MADC}) = 5.6448 \text{ MHz} \quad (13)$$

$$\text{DAC_MOD_CLK} = \text{PLL_CLK} / (\text{NDAC} \times \text{MDAC}) = 5.6448 \text{ MHz} \quad (14)$$

where:

- MADC = 3; NADC = 5; AOSR = 128
- MDAC = 3; NDAC = 5; DOSR = 128
- AVDD = 1.8 V; DVDD = 1.65 V; PLL mode = 0

$$\text{ADC_fs} = 44.1 \text{ kHz} \quad (15)$$

$$\text{DAC_fs} = 44.1 \text{ kHz} \quad (16)$$

2.3 Power Supplies Noise Level

As mentioned in [Section 2.1](#), the audio codecs are divided to have an analog and digital partition requiring a specific power supply. The performance of the analog and digital sections is dependent on the power supply level and its noise contribution. If the power supply is not well regulated or has a voltage level problem, device performance could suffer.

To understand the relationship between a codec block and a power supply, the MICBIAS1 and AVDD pins of the TLV320ADC3101 device are the focus in this example (see [Figure 3](#)).

MICBIAS Control is used to control the MICBIAS1 level. This register can be configured as 2 V, 2.5 V, or AVDD. A switch inside the TLV320ADC3101 device is used to select the desired voltage level.

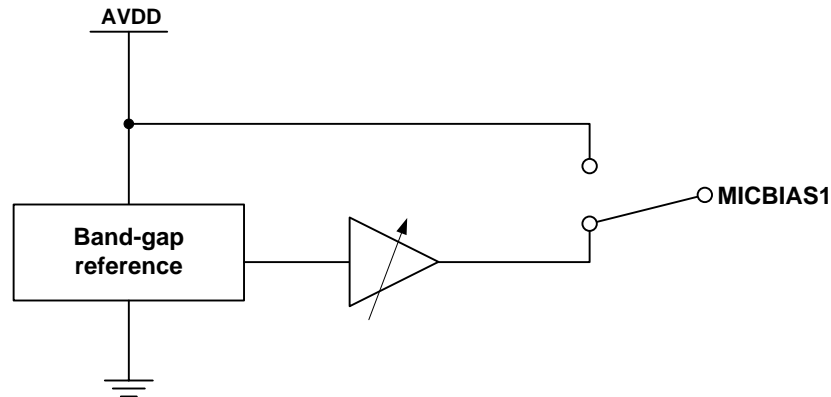


Figure 3. MICBIAS Pin Internal Configuration

TI recommends reducing the noise level at the power supplies in all TI audio converters. In this particular example, MICBIAS1 can be configured to take the AVDD level directly. If the AVDD is not regulated properly, all the noise effects will be coupled into the MICBIAS1 pin. If a microphone is connected to the MICBIAS1 pin, the microphone signal will directly see this noise contribution at the converter input.

Recommendations to reduce the power supply noise follow:

- Add the suggested decoupling capacitors (0.1 μF and 10 μF) as close as possible to the audio codec power pins and in the same layer as the IC.
- If the power supply contains a high-frequency noise level, add a low-pass filter to eliminate the noise. EMI filters are suggested as well.
- Use ground splitting

2.4 Out-of-Band Noise

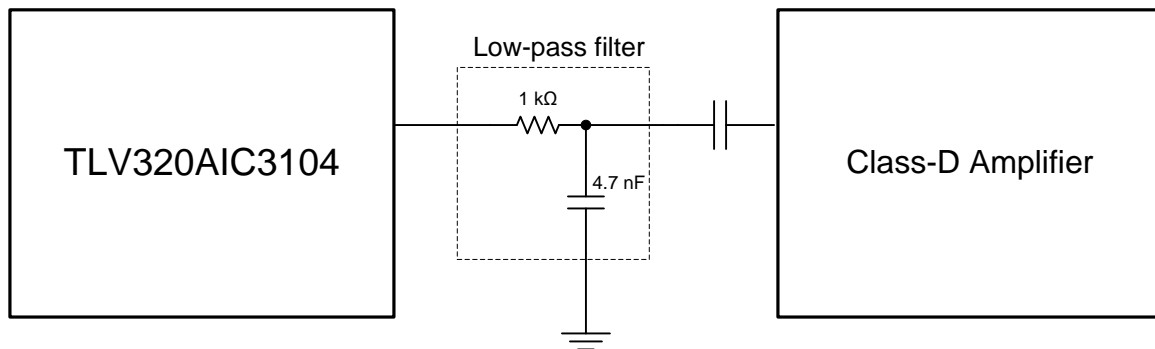
Out-of-band noise is defined as the noise contained in frequencies outside of the audible frequency band. This noise is typically seen on the audio codecs due to the aliasing effect and the sigma-delta architecture of the ADCs and DACs.

This phenomenon does not allow having a clean measurement. Additionally, it affects the audio applications when a Class-D amplifier is connected to the audio codec. The Class-D amplifier increases the noise level and it is added on the audio signal.

The TLV320AIC3104 device is used as an example (see [Figure 4](#)).

The LEFT_LOP/M and RIGHT_LOP/M line outputs are normally used as a Class-D amplifier input. Even if the out-of-band noise is not in the audible band, the external Class-D amplifier can increase this noise. Consequently, the harmonics level is increased as well and the audible band is affected.

TI suggests adding a low-pass filter at the audio codec output to avoid these issues. A 1-k Ω resistor and 4.7-nF capacitor are suggested for noise reduction. These values were chosen to create a pole at 33 KHz, which is good for audio applications.



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Figure 4. Suggested Low-Pass Filter

For more information, see the [Out-of-Band Noise Measurement Issues for Audio Codecs](#) application report.

2.5 Line Output Routing in TLV320AIC310x Family

The TLV320AIC310x family of devices is a low-power, stereo, audio codec family used for portable applications. These devices contain high-power (or headphone) outputs and line outputs. The [TLV320AIC3104 block diagram](#) is used as an example.

In the TLV320AIC310x family, the DAC blocks may be routed to the headphone and/or line outputs. These DAC blocks have three different ways to route the DAC data to the outputs. These three optional paths are used to select the output mixer, line output, or headphone output.

- [Figure 5](#) shows the mixer path. This mixer allows for routing multiple signal paths, such as the PGA output and the DAC output. The mixer result is routed to the headphone and/or line output.

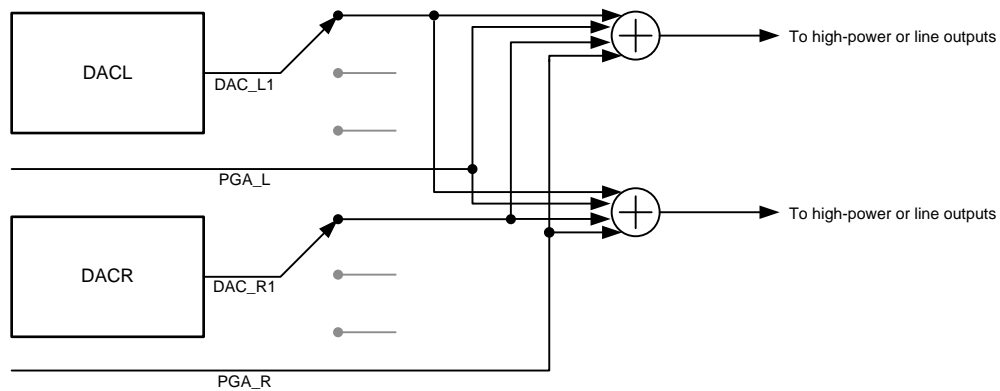


Figure 5. Mixer Path

- [Figure 6](#) shows the headphone (or high-power) path. This path is a low-power path that routes the DAC output to the headphone output directly.

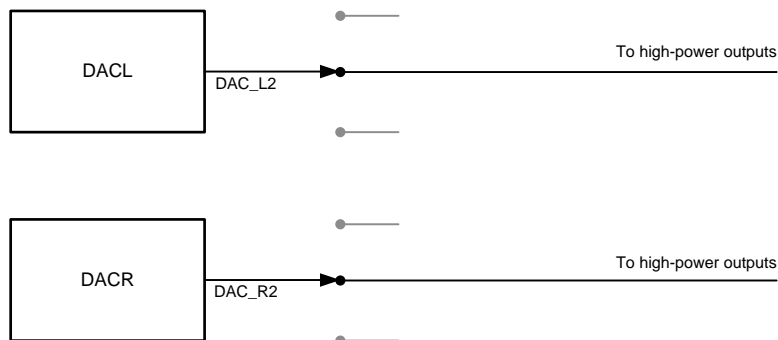


Figure 6. Headphone Path

- [Figure 7](#) shows the line output path. Similar to the headphone path, this is a low-power path. The line output path routes the DAC output to the line output.

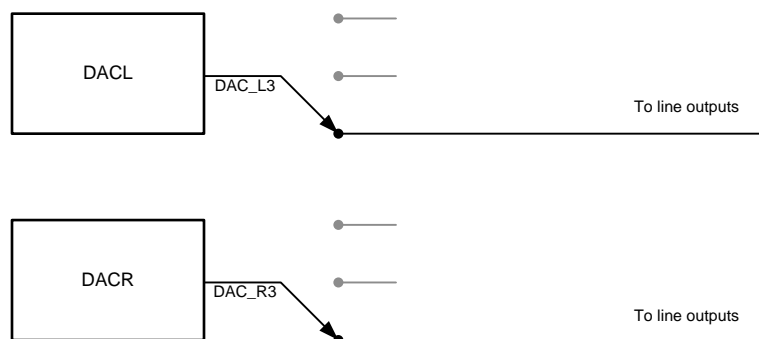


Figure 7. Line Output Path

The headphone and line output paths are the low-power paths, and the mixer path is ideal when the user seeks the best performance. Each output mixer contains a low-pass filter that eliminates the high-frequency content and improves the signal quality. The cutoff frequency of the filters is set by the DAC Quiescent Current Adjustment (register 109 used to configure the current level).

The three possible options to adjust the DAC Quiescent Current follow:

- Default – Typical cutoff frequency is 424 kHz.
- 50% increase in DAC reference current – Typical cutoff frequency is 637 kHz.
- 100% increase in DAC reference current – Typical cutoff frequency is 849 kHz.

The selection of the DAC Quiescent Current depends of the filter characteristic that the user requires for the audio application. If the out-of-band noise level is not considerably high, TI recommends selecting the 100% increase in DAC reference current option. This option allows for having the DAC in high-performance operation.

3 Conclusion

Audio codecs can be sensitive to noise issues generated from multiple sources. It is important to anticipate all noise events to get the best performance of the codec and design accordingly. Even if the audio codec offers some filters and audio processing, many noise issues can be related to hardware configuration. The user must ensure that the PCB layout is properly designed. The audio codecs data sheets have specific sections that can be used as a guide to design the audio codec board. If these sections are not properly followed, the noise probability increases.

If you there is abnormal noise on the board even after following the advice in this application report, contact our [TI E2E Community](#).

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