Application Report
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Clock System Design for Digital Audio Application Based on DIR9001, PCM3070 and MSP430

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ABSTRACT

Digital Audio is widely used in consumer electronics such as Soundbar, Smart TV, Home Theater, and so on. Audio sampling frequency and system clock source are varied in different application. Clock design is key for system reliability and performance. This paper presents clock system design technique for Digital Audio application base on TI hero solution. Guideline and analysis of hardware design, software design and register configuration for different scenarios are discussed. And Issue of Real Case are shared. It can help customer to solve common issue, optimize system design and accelerate design cycle.

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1 Traditional Digital Audio System Overview

Figure 1 is a block diagram of one digital audio system.

There is biphase input through Optical / Coaxial. A digital audio interface receiver is needed to convert the biphase input signal such as S/PDIF to serial audio data formats such as I^2S for audio processor. Analog signal input is usually present in system. Operational-Amplifier is used for analog signal conditioning, and then the analog signal goes to ADC to convert to serial audio data Output formats for audio processor. Audio processor output the audio data which has been processed by analog or serial audio data formats, and transmits to audio amplifier. Audio amplifier will drive speaker or headphone to output the sound.

MCU configure Codec and digital audio interface receiver, and detect different input source. If biphase input signal is chosen, digital audio interface receiver will retrieve MCLK (Master Clock) from biphase input signal. If analog input is chosen, it will pass frequency of crystal for MCLK.

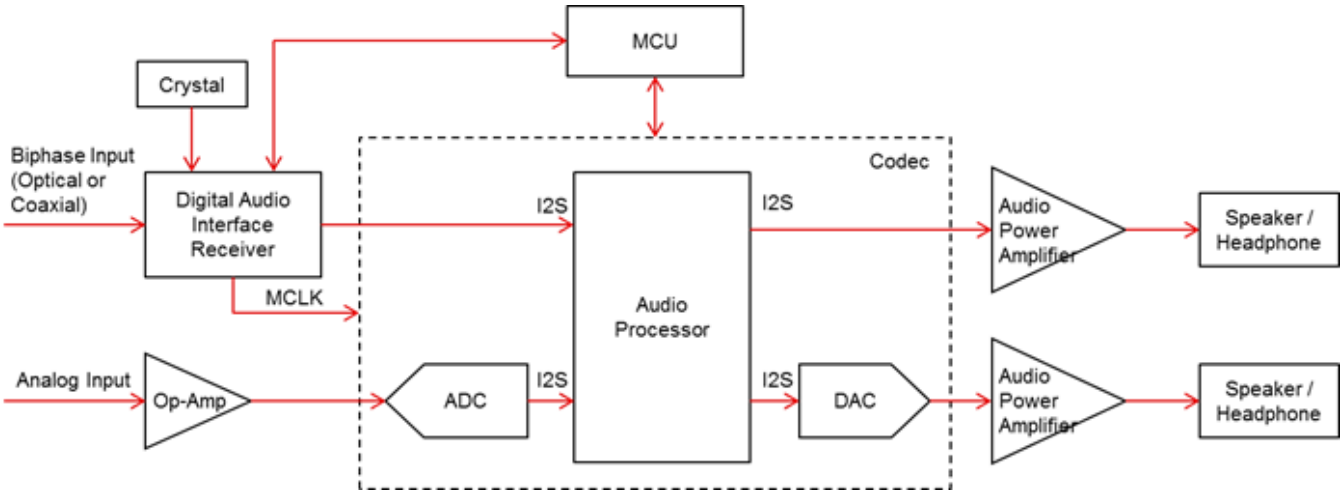

Figure 1. Traditional Digital Audio System Block Diagram

There are multiple sampling frequencies in digital input source, including 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, and so on. And ADC sampling frequency and clock path of analog input source is also different. Improper clock configuration may cause noise, whistle or silence. Therefore, proper clock configuration is key to ensure system functionality and stability.

2 Digital Audio Interface Receiver (DIR9001) Configuration Technique

The DIR9001 is a digital audio interface receiver that can receive a 28-kHz to 108-kHz sampling-frequency, 24-bit-data-word, biphase-encoded signal and convert to serial audio data formats output such as I^2S DIR9001 can work in 2 modes. These modes are selected by the connection of the CKSEL pin.

1. When CKSEL = 0, PLL Mode is selected. PLL integrated in DIR9001 will be activated, and recover MCLK by demodulating the biphase input signal.
2. When CKSEL = 1, XTI Mode is selected. DIR9001 will always output frequency of crystal on XTI pin for MCLK.

NOTE: MCLK (Master Clock) output on SCKO pin of DIR9001;

BCLK (Bit Clock) output on BCKO pin of DIR9001;

LRCLK (Left/Right channel Clock, Actual Sampling Frequency) output on LRCKO pin of DIR9001

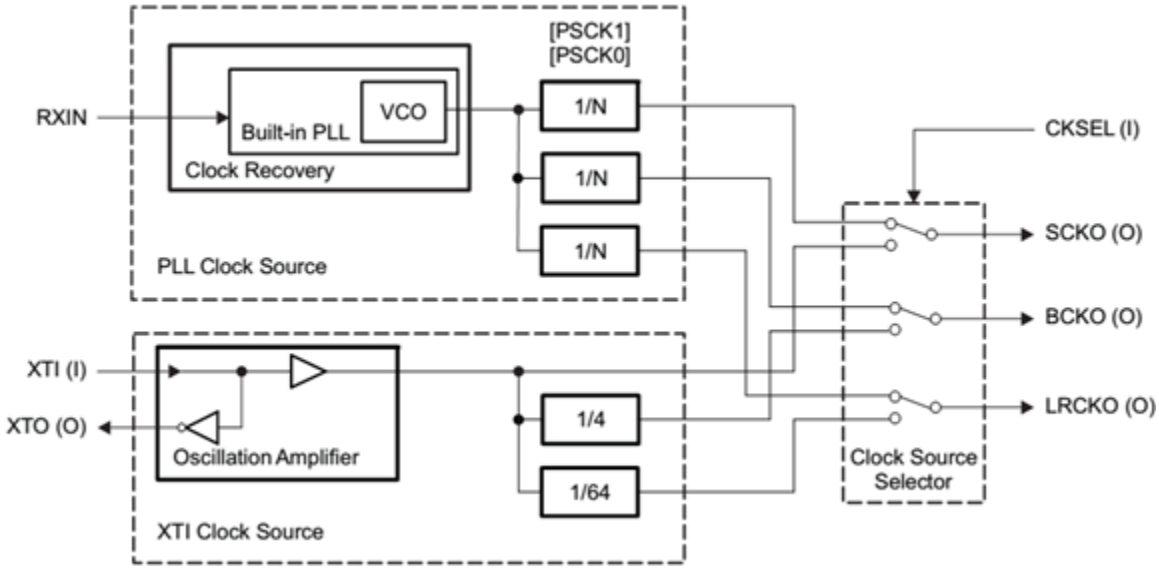

Figure 2. DIR9001 Internal Clock Tree

2.1 Clock Configuration for PLL Mode

In this mode, there should be valid biphase input signal on RXIN pin. MCLK is recovered from biphase input signal.

2.1.1 Clock Frequency Control

LRCLK is actual sampling frequency of biphase input signal. Actual MCLK and BCLK frequency are set by pin PSCK1 and PSCK0.

The relationship between the PSCK[1:0] selection and the output clock (SCKO, BCKO, LRCKO) from the PLL source, and common clock frequency examples are shown in Table 1.

Table 1. SCKO, BCKO, and LRCKO Frequencies Set by PSCK[1:0]

LRCKO (kHz)	BCKO (MHz)	SCKO (MHz)			
		PSCK[1:0] Setting			
		00	01	10	11
fs	64 x fs	128 x fs	256 x fs	384 x fs	512 x fs
32	2.048	4.096	8.192	12.288	16.384
44.1	2.8224	5.6448	11.2896	16.9344	22.5792
48	3.072	6.144	12.288	18.432	24.576
88.2	5.6448	11.2896	22.5792	33.8688	45.1584
96	6.144	12.288	24.576	36.864	49.152

2.1.2 Sampling Clock Frequency Monitoring

DIR9001 can calculate the actual sampling frequency of the biphase input signal and outputs its result through FSOUT1 and FSOUT0 pins. MCU can use the sampling clock frequency information to adjust clock setting of Audio Processor.

To use this function, a 24.576-MHz clock source must be supplied to the XTI pin as a measurement reference clock to calculate the actual sampling frequency. If the XTI pin is connected to DGND, calculation of the actual sampling frequency is not performed. If there is an error in the XTI clock frequency, the calculation result and range are shifted correspondingly.

There is an ERROR pin which indicates whether biphase input data is valid and PLL is lock. It can be used together with FSOUT[1:0] for more sampling frequency.

The relationship between the FSOUT[1:0] outputs and the range of sampling frequencies is shown in Table 2.

Table 2. Calculated Sampling Frequency Output

Nominal Fs (kHz)	Actual Sampling Frequency Range (kHz)	Sampling Frequency Information Output on FSOUT[1:0] Pins	ERROR Pin
PLL unlock	PLL unlock	10	1
32	31.2 ~ 32.8	11	0
44.1	43 ~ 45.2	00	0
48	46.8 ~ 49.2	01	0
Out of range e.g. 88.2 or 96	49.2 ~ 108	10	0

2.2 Clock Configuration for XTI Mode

In this mode, an external crystal or clock source should be connected to XTI pin. MCLK is same as XTI clock. BCLK is 1/4 of MCLK, and LRCLK is 1/256 of MCLK.

In applications with biphase digital signal input, 24.576-MHz crystal or clock on XTI pin is recommended, as it can ensure correct sampling frequency information output.

Table 3. SCKO, BCKO, and LRCKO Frequencies in XTI Mode

XTI Frequency (MHz)	SCKO (MHz)	BCKO (MHz)	LRCKO (kHz)
f_{XTI}	f_{XTI}	$f_{XTI}/4$	$f_{XTI}/256$
24.576	24.576	6.144	96

In most application, XTI mode is used only when analog signal is chosen for system input. Only MCLK (SCKO) will be used in audio processor in this situation.

2.3 System Design Technique

2.3.1 System with Analog Input Signal Only

In this case, only MCLK is needed to provide to audio processor, data converter or digital amplifier. Most common and low cost solution is using crystal and inverter to generate MCLK. The crystal frequency can be selected by desired ADC/DAC sampling rate and recommend MCLK range of audio processor, data converter or digital amplifier.

For example, desired sampling rate is 48 kHz, and MCLK is selected to 256 x fs according to data converter specification. MCLK is 256 x 48 kHz = 12.288 MHz. Figure 3 is reference circuit of MCLK generation.

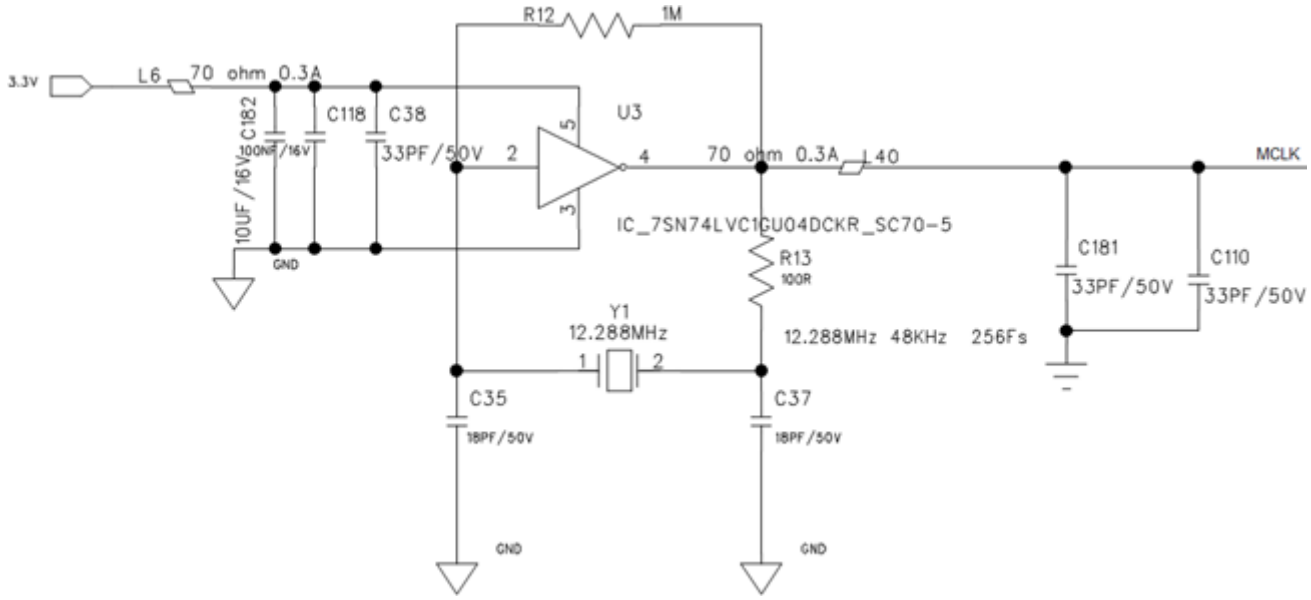

Figure 3. Crystal MCLK Generation Circuit

2.3.2 System with Biphase Digital Input Signal Only

In this case, DIR9001 is the best choice for demodulate biphase input signal and generate clock for audio processor, data converter or digital amplifier in system.

According to Section 2.2 and Section 2.3, the recommended configuration of several common cases is listed as follows.

2.3.2.1 MCU Does Not Need to Know the Actual Sampling Rate

1. No crystal is needed, and connects XTI to GND, as sampling frequency measurement and analog input is not need.
2. Set CKSEL = 0. DIR9001 works in PLL mode, and recover MCLK, LRCLK, BCLK from biphase input signal.
3. Choose PSCK[1:0] to set appropriate multiplier where MCLK = multiplier x fs. For example, 256 is a common value.

2.3.2.2 MCU Needs to Know the Actual Sampling Rate

1. Connect 24.576MHz crystal or clock source to XTI pin, in order to ensure correct sampling rate measurement.
2. Set CKSEL = 0. DIR9001 works in PLL mode, and recover MCLK, LRCLK, BCLK from biphase input signal
3. Choose PSCK[1:0] to set appropriate multiplier where MCLK = multiplier x fs. For example, 256 is a common value.
4. Connect ERROR pin to MCU, if MCU need to know the invalid biphase data input or PLL unlock.
5. If there are only 44.1-kHz and 48-kHz sampling frequency are allowed in system, connect FSOUT0 to MCU.
6. If 32 kHz ~ 96 kHz sampling frequency are allow in system, connect both FSOUT1 and FSOUT0 to MCU.

2.3.3 System with Both Biphase Digital Input Signal and Analog Input Signal

In this case, DIR9001 demodulate biphase input signal or pass XTI clock signal and generate clock for audio processor, data converter or digital amplifier in system.

According to Section 2.2 and Section 2.3, the recommended configuration of several common cases is listed as follows.

1. Connect 24.576-MHz crystal or clock source to XTI pin, making sure there is 24.576-MHz MCLK output on SCKO pin when analog input is chosen.
2. If biphase input has higher priority than analog input, connect CKSEL pin to ERROR pin. Once biphase signal is invalid, ERROR = 1. That makes CKSEL = 1 and clock source is switch to XTI for analog input.
3. If input source is selected by end user manually, connect CKSEL to MCU.
4. Choose PSCK[1:0] to set appropriate multiplier where MCLK = multiplier x fs. For example, 256 is a common value
5. Connect ERROR pin to MCU, if MCU need to know the invalid biphase data input or PLL unlock, and perform auto audio source detection.
6. If there are only 44.1-kHz and 48-kHz sampling frequency are allowed in system, connect FSOUT0 to MCU.
7. If 32 kHz ~ 96 kHz sampling frequency are allow in system, connect both FSOUT1 and FSOUT0 to MCU.

2.3.4 MCU Work Flow Example

Take system configuration in Section 2.3.3 for example. Figure 4 is the MCU software flow chart switching input source and sampling rate. Interrupt mode is also good for ERROR and FSOUT[1:0] detection. Configuration of audio processor is discussed in Section 3.

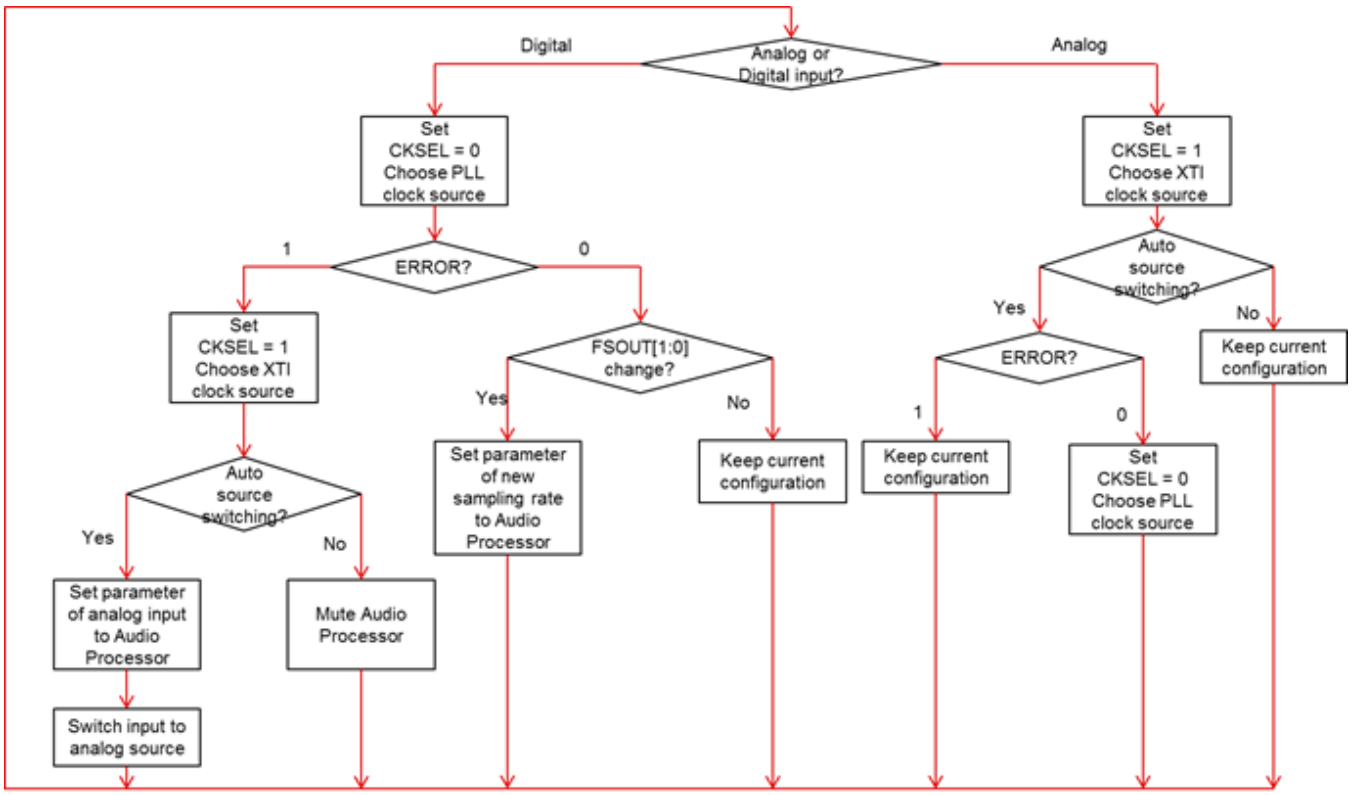

Figure 4. MCU Software Flow Chart Switching Input Source and Sampling Rate

3 Codec (PCM3070) Clock Configuration Analysis

The PCM3070 is a flexible stereo audio codec with programmable inputs and outputs, fully-programmable miniDSP, fixed predefined and parameterizable signal processing blocks, integrated PLL, integrated LDOs and flexible digital interfaces.

The required internal clock of the PCM3070 can be derived from MCLK pin, BCLK pin, GPIO pin or the output of the internal PLL. And the input to the PLL can also be derived from MCLK pin, BCLK or GPIO pins. The PLL is highly programmable and can accept available input clocks in the range of 512 kHz to 50 MHz. Figure 5 is the Clock distribution tree of PCM3070.

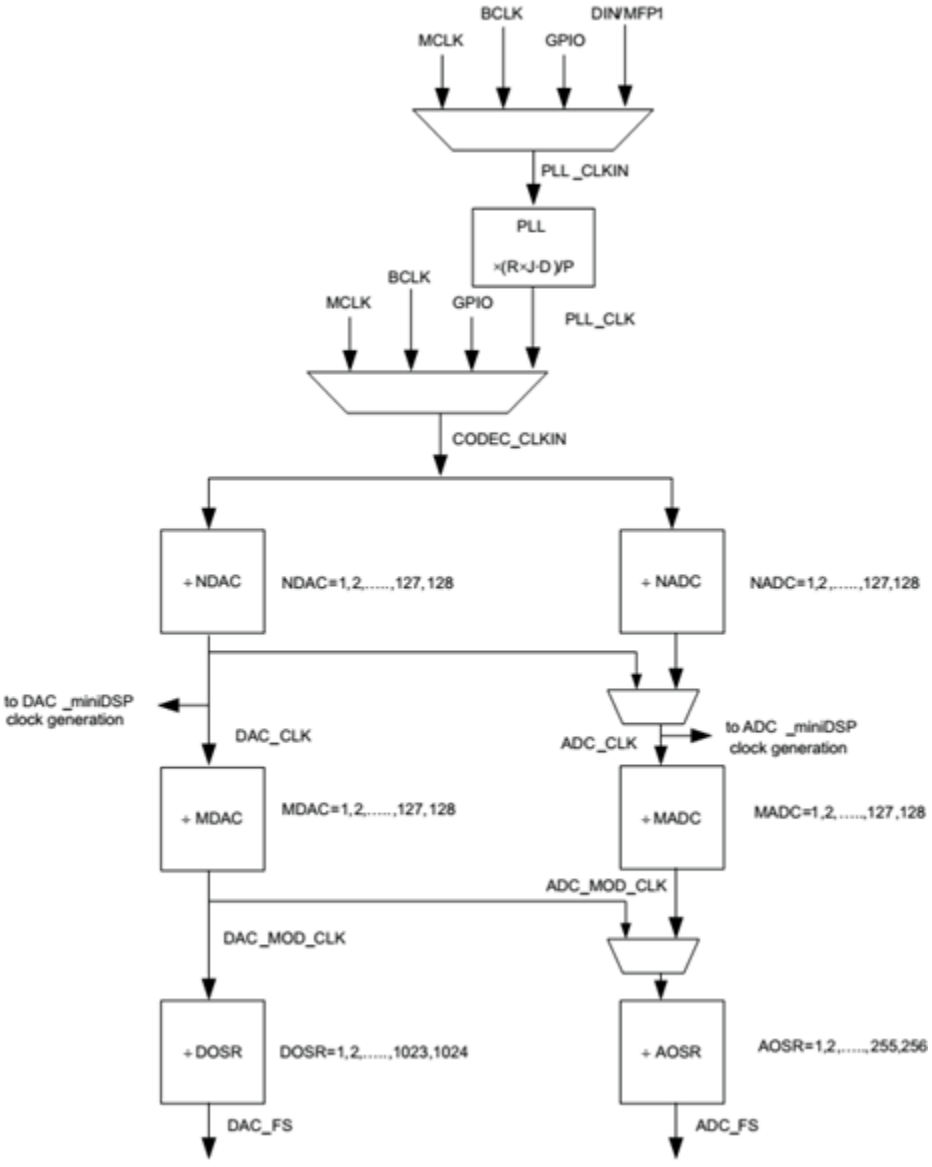

Figure 5. Clock Distribution Tree of PCM3070

3.1 PLL Configuration

According to Figure 5, Codec Clock and PLL Clock can come from multiple sources. In most of the cases, MCLK is used for PLL input, as it exists in most of audio system, and it is related to sampling frequency. It is easy to sync up all devices in system using MCLK.

PLL_CLKIN = MCLK = SCKO from DIR9001 (1)

When the PLL is enabled, the PLL output clock PLL_CLK is given by the following equation:

PLL_CLK = (PLL_CLKIN x R x J.D) / P

where

- R = 1, 2, 3, 4
- J = 1, 2, 3, 4,… 63, and D = 0, 1, 2, 3, 4, … 9999
- P = 1, 2, 3, 4, … 8
- R, J, D, and P are register programmable. (2)

There are 2 points that should be taken caution. PCM3070 may work abnormally if these requirements are not meet.

1. Input clock range of PLL

   When the PLL is enabled,

   If D = 0, the following conditions must be satisfied for PLL_CLKIN

   512 kHz ≤ PLL_CLKIN / P ≤ 20 MHz (3)

   If D ≠ 0, the following conditions must be satisfied for PLL_CLKIN:

   10 MHz ≤ PLL_CLKIN / P ≤ 20 MHz (4)

2. Output clock rage of PLL.

   The PLL_CLK must be within following rage in Table 4.

Table 4. PLL_CLK Frequency Range

AVdd	PLL Mode Page 0, Reg 4, D6	Min PLL_CLK Frequency (MHz)	Max PLL_CLK Frequency (MHz)
≥1.5 V	0	80	103
	1	95	110
≥1.65 V	0	80	118
	1	92	123
≥1.8 V	0	80	132
	1	92	137

3.2 Codec Clock Configuration

The Codec clock input CODEC_CLKIN can be set to MCLK, BCLK, GPIO or PLL_CLK. And then CODEC_CLKIN will be divided by several clock dividers (NDAC, NADC, MDAC, MADC, DOSR, AOSR) to generate different clock for different components of PCM3070 as shown in Figure 5.

ADC_miniDSP_CLK = CODEC_CLKIN / NADC (5)

ADC_MOD_CLK = CODEC_CLKIN / (NADC x MADC) (6)

ADC_fs = CODEC_CLKIN / (NADC x MADC x AOSR) (7)

DAC_miniDSP_CLK = CODEC_CLKIN / NDAC (8)

DAC_MOD_CLK = CODEC_CLKIN / (NDAC x MDAC) (9)

DAC_fs = CODEC_CLKIN / (NDA x MDAC x DOSR) (10)

All clock frequency must meet requirement in Table 5.

Table 5. Maximum PCM3070 Clock Frequencies

	DVdd ≥ 1.26V	DVdd ≥ 1.65V
CODEC_CLKIN	50 MHz	137 MHz when NDAC is even, NADC is even 112 MHz when NDAC is even, NADC is odd 110 MHz when NDAC is odd, NADC is even 110 MHz when NDAC is odd, NADC is odd
ADC_CLK	25 MHz	55.296 MHz
ADC_miniDSP_CLK	20 MHz	55.296 MHz 51 MHz if AGC is on
ADC_MOD_CLK	6.758 MHz	6.758 MHz
ADC_FS	0.192 MHz	0.192 MHz
DAC_CLK	25 MHz	55.296 MHz
DAC_miniDSP_CLK	20 MHz	55.29 MHz
DAC_MOD_CLK	6.758 MHz 4.2 MHz when Class-D Mode Headphone is used	6.758 MHz
DAC_FS	0.192MHz	0.192MHz
BDIV_CLKIN	25 MHz	55.296MHz
CDIV_CLKIN	50 MHz	112 MHz when M is odd 137 MHz when M is even

The clock setting is flexible. The higher miniDSP_CLK is chosen, the higher performance will be, but the power consumption is high. In order to get optimized value, obtain the recommended NDAC, NADC, MDAC, MADC, DOSR, AOSR, CODEC_CLKIN values from PurePath™ Studio.

Place framework of Codec on the file, select “SystemSettingCode” in right sidebar, and then press “…” button. A text file will pop up. Recommended value for common sampling rate can be get in it. Recommended values are shown in Table 6.

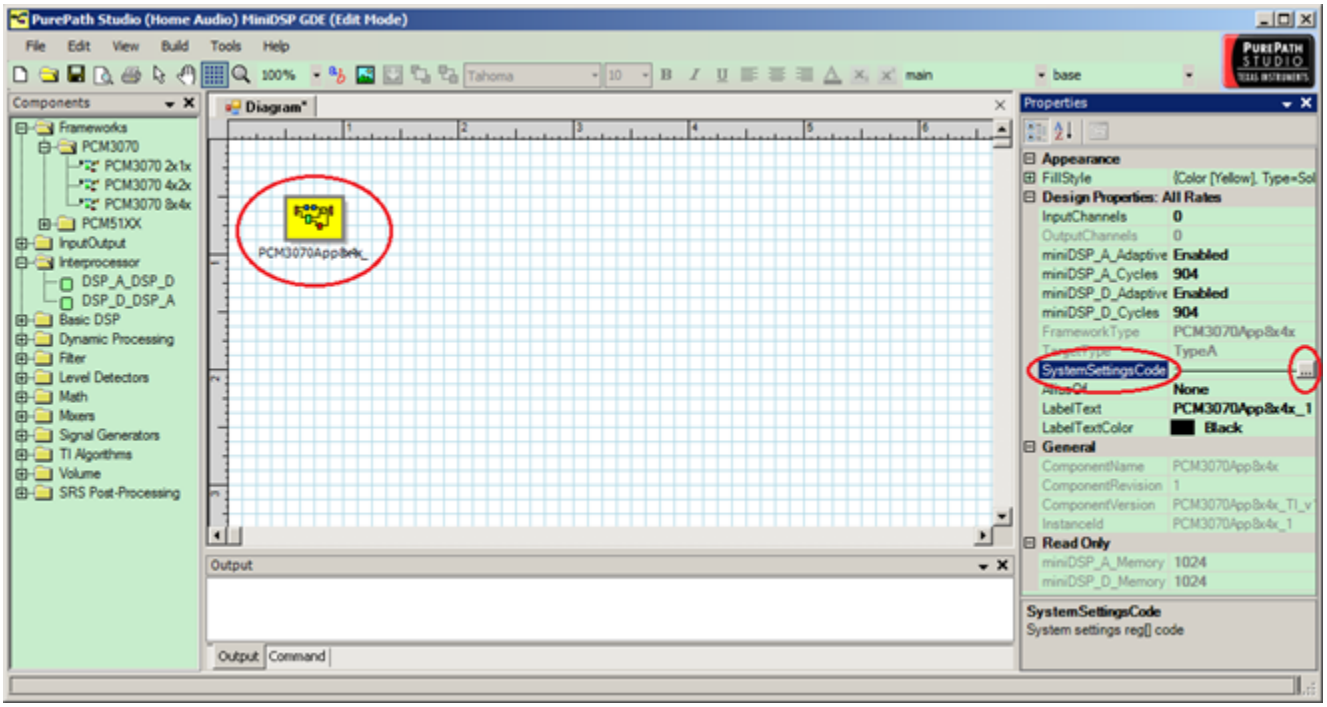

Figure 6. Way to Open SystemSettingCode in PurePath Studio

Table 6. Recommend Parameter Setting for Common Sampling Rate

Sampling Rate (kHz)	NDAC	MDAC	DOSR	NADC	MADC	AOSR	CODEC_CLKIN (MHz)
8	2	8	768	2	48	128	98.304
11.025	2	8	512	2	32	128	90.3168
16	2	8	384	2	24	128	98.304
22.05	2	8	256	2	16	128	90.3168
24	2	8	256	2	16	128	98.304
32	2	8	192	2	12	128	98.304
44.1	2	8	128	2	8	128	90.3168
48	2	8	128	2	8	128	98.304
88.2	2	8	64	2	8	64	90.3168
96	2	8	64	2	8	64	98.304
176.4	2	8	32	2	8	32	90.3168
192	2	8	32	2	8	32	98.304

3.3 PCM3070 Clock and PLL Design Flow

Example will be used together with design flow description for better understanding.

Table 7. PCM3070 Clock and PLL Design Flow and Example

Step	Content	Example 1	Example 2	Example 3
0	Start condition	AVdd = DVdd = 1.8 V MCLK = 12 MHz fs = ADC_fs = DAC_fs = 44.1 kHz	AVdd = DVdd = 1.8 V MCLK = 2.048 MHz fs = ADC_fs = DAC_fs = 96 kHz	AVdd = DVdd = 1.8 V MCLK = 8 MHz fs = ADC_fs = DAC_fs = 44.1 kHz
1	Does integer m, n exist, and let fs x m / n = MCLK? (1) If yes, go to Step 3. (2) If no, go to Step 2.	m and n do not exist.	m and n exist.	m and n do not exist.
2	MCLK ≥ 10 MHz? (1) If yes, go to Step 3. (2) If no, PCM3070 not support. **Design Terminated.**	MCLK ≥ 10 MHz.		MCLK < 10 MHz PCM3070 can not support.
3	Confirm NDAC, NADC, MDAC, MADC, DOSR, AOSR, CODEC_CLKIN from Figure 6 Go to Step 4.	NDAC = NADC = 2 MDAC = MADC = 8 DOSR = AOSR = 128 CODEC_CLKIN = 90.3168 MHz	NDAC = NADC = 2 MDAC = MADC = 8 DOSR = AOSR = 64 CODEC_CLKIN = 98.304 MHz	
4	MCLK = CODEC_CLKIN? (1) If yes, route MCLK to CODEC_CLKIN. **Design Complete.** (2) If no, PLL should be used, route MCLK to PLL_CLKIN, and route PLL_CLK to CODEC_CLKIN Go to Step 5.	12 MHz ≠ 90.3168 MHz PLL should be used. PLL_CLKIN = MCLK = 12 MHz PLL_CLK = CODEC_CLKIN = 90.3168 MHz	2.048 MHz ≠ 90.3168 MHz PLL should be used. PLL_CLKIN = MCLK = 2.048 MHz PLL_CLK = CODEC_CLKIN = 98.304 MHz	
5	Does integer m, n exist, and let fs x m / n = MCLK? (1) If yes, D = 0, and 512 kHz ≤ PLL_CLKIN / P ≤ 20 MHz; (2) If no, D ≠ 0, and 10 MHz ≤ PLL_CLKIN / P ≤ 20 MHz. Select P value. Go to Step 6.	m and n do not exist. So D ≠ 0. 12 MHz / 20 MHz ≤ P ≤ 12 MHz / 10 MHz 0.6 ≤ P ≤ 1.2 Select P = 1	m and n exist. So D = 0. 2.048 MHz / 20 MHz ≤ P ≤ 2.048 MHz / 512 kHz 0.1024 ≤ P ≤ 4 Select P = 1, for smaller value of R, J and D	
6	Calculate R x J.D = PLL_CLK x P / PLL_CLKIN Select R, J and D value. **Design Complete.**	R x J.D = 90.3168 MHz x 1 / 12 MHz = 7.5264 Select R = 1, J = 7, D = 5264	R x J.D = 98.304 MHz x 1 / 2.048 MHz = 48 Select R = 4, J = 12, D = 0	

When modifying clock setting,

1. All the root clock dividers should be powered down only after the child clock dividers have been powered down for proper operation.
2. All the root clock dividers should be powered on only before the child clock dividers have been powered on for proper operation

4 System Design Example and Case Sharing

4.1 System Design Example

4.1.1 System Specification

Input:

Coaxial and Optical Biphase input. Support sampling rate: 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz; USB input. Sampling rate 48 kHz;

Line in, 48kHz ADC sampling rate;

Microphone input, 8kHz sampling rate.

Output:

Speaker output: 15 W x 2;

Headphone output.

4.1.2 Hardware Design

DIR9001 is used to decode biphase signal from Optical, Coaxial or USB, and generate MCLK for system. PCM3070 is used to convert and process data. 24.576-MHz crystal is selected for MCLK source for analog input, and biphase sampling rate measurement reference. MSP430 monitor FSOUT0, FSOUT1 and ERROR pin to monitor input biphase signal validation and sampling, in order to modify clock configuration in PCM3070 when input source changes. MSP430 also control CLKSEL pin to select input source. TAS5707 is used for 15 W x 2 audio amplifier.

When Line in is selected, MCLK = 24.576 MHz and fs = 48 kHz. So MCLK = 512 x fs. As most common biphase sampling rates are 44.1 kHz and 48 kHz today. In order to keep PCM3070 clock setting unchanged when switching between analog input and biphase input (44.1 kHz or 48 kHz), 512 x fs is selected for biphase clock recover. So both PSCK1 and PSCK0 are connected to 1. Figure 7 is the hardware design block diagram.

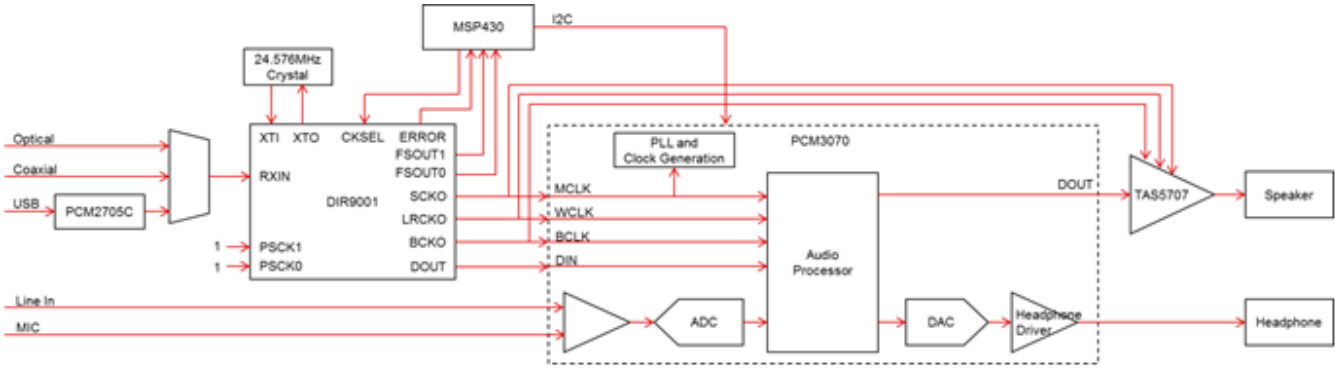

Figure 7. Hardware Design Block Diagram

4.1.3 PCM3070 Clock Setting

According to specification in 5.1.1, and design flow in Table 7, Table 8 is clock setting parameter. R keeps unchanged for all conditions. J keeps unchanged except in 32-kHz sampling rate. NDAC, MDAC and NADC keep unchanged for all conditions. When clock source switches between Line in, 44.1-kHz biphase, and 48-kHz biphase, no clock setting needs to change in PCM3070.

Table 8. Clock Setting Parameter

Input	Sampling Rate fs (kHz)	MCLK (MHz)	P	R	J	D	PLL_CLK (MHz)	NDAC	MDAC	DOSR	NADC	MADC	AOSR
Biphase	32	16.384	1	1	6	0	98.304	2	8	192	2	12	128
	44.1	22.5792	2	1	8	0	90.3168	2	8	128	2	8	128
	48	24.576	2	1	8	0	98.304	2	8	128	2	8	128
	88.2	45.1584	4	1	8	0	90.3168	2	8	64	2	8	64
	96	49.152	4	1	8	0	98.304	2	8	64	2	8	64
MIC in	8	24.576	2	1	8	0	98.304	2	8	768	2	48	128
Line in	48	24.576	2	1	8	0	98.304	2	8	128	2	8	128

4.1.4 Software Design

The software flow chart is similar with Figure 4.

4.2 Case Sharing

4.2.1 Background

A customer used DIR9001 and PCM3070 to develop value soundbar. There are analog and coaxial digital inputs. Sampling rate of analog is 48 kHz. Sampling rate of coaxial is 44.1 kHz or 48 kHz. SRS process is implemented in PCM3070. TAS5707 is used as amplifier.

After MP, more than 2% of the PCM3070 are abnormal. When analog input is chosen, there is no issue. When digital input is chosen, there will be abnormal noise. The noise is there once system power up.

4.2.2 Approach to Solve the Issue

1. Checked I2S waveform. There was no issue.
2. Deleted all signal processing blocks and just bypassed signal in miniDSP of PCM3070. There was still abnormal noise.
3. Connected DIR9001 to TAS5707, there was no issue.

An issue with PCM3070 was suspected. After a review of the hardware and software design of PCM3070, an issue was found in the PCM3070 clock setting.

Customer connected 12.288-MHz crystal on the XTI pin of DIR9001. Clock setting of PCM3070 was based on 12.288-MHz MCLK. When the input was switched to a 44.1-kHz or 48-kHz coaxial input, the same clock setting is still be used. Table 9 is the original clock setting.

Table 9. Original Clock Setting with Issue

Input	Sampling Rate fs (kHz)	MCLK (MHz)	P	R	J	D	PLL_CLK (MHz)	NDAC	MDAC	DOSR	NADC	MADC	AOSR
Coaxial	44.1	22.5792	1	1	8	0	180.6336	2	8	128	2	8	128
	48	24.576	1	1	8	0	196.608	2	8	128	2	8	128
Line in	48	12.288	1	1	8	0	98.304	2	8	128	2	8	128

When line in was selected, PLL setting is OK. When coaxial is selected, the PLL output clock is up to 180.6336 MHz and 196.608 MHz, which exceeded maximum value in Table 4.

As there is different tolerance in different PCM3070, the issue did no appear in all PCM3070.

4.2.3 Solution

4.2.3.1 Hardware solution

Connect PSCK1 pin of DIR9001 to 0, which set MCLK = 256 x fs. The PCM3070 clock setting will be correct.

Table 10. Clock Setting of Hardware Solution

Input	Sampling Rate fs (kHz)	MCLK (MHz)	P	R	J	D	PLL_CLK (MHz)	NDAC	MDAC	DOSR	NADC	MADC	AOSR
Coaxial	44.1	11.2896	1	1	8	0	90.3168	2	8	128	2	8	128
	48	12.288	1	1	8	0	98.304	2	8	128	2	8	128
Line in	48	12.288	1	1	8	0	98.304	2	8	128	2	8	128

4.2.3.2 Software solution

Modified J to 4 when coaxial is selected. The PCM3070 clock setting will be correct.

Table 11. Clock Setting of Software Solution

Input	Sampling Rate fs (kHz)	MCLK (MHz)	P	R	J	D	PLL_CLK (MHz)	NDAC	MDAC	DOSR	NADC	MADC	AOSR
Coaxial	44.1	22.5792	1	1	8	0	90.3168	2	8	128	2	8	128
	48	24.576	1	1	8	0	98.304	2	8	128	2	8	128
Line in	48	12.288	1	1	8	0	98.304	2	8	128	2	8	128

As it was MP product, customer did not want to modify hardware, software solution is selected.

5 Conclusion

Clock design is critical in digital audio system, but many customer may be careless about it during design phase. As there is different tolerance in IC, the issue caused by incorrect clock design may not appear before MP. It cost a lot to fix issue after MP. Clock design guideline and technique are discussed in this artical. Issue of Real Case is shared. It not only can help customer to solve common issue, but also help customer to determine correct design in design phase, and accelerate design cycle.

6 Reference

DIR9001 Datasheet (SLES198)

PCM3070 Datasheet (SLAS724)

PCM3070 Application Reference Guide (SLAU332)

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