Application Report
SLAA412A–June 2009–Revised August 2017

LDO Noise Demystified

Sanjay Pithadia and Ankur Verma — *PMP - LP Linear Regulators*

ABSTRACT

This application report explains the difference between noise and PSRR of an LDO. It also explains the different ways noise is specified in LDO datasheets and which specification should be used in the application. Finally it explains how LDO noise is reduced.

Contents

List of Figures

List of Tables

Trademarks

1 LDO Noise and PSRR

Low dropout linear regulators (LDOs) are a simple way to regulate an output voltage that is powered from a higher voltage input. Though it is simple to operate, its self generated noise is most of the times confused with its Power Supply Rejection Ratio (PSRR). Many times the two are combined together and loosely called just “noise”. This is not correct. Noise is generated by the transistors and resistors in the LDO’s internal circuitry and by the external components. The type of noise may include thermal, flicker and shot noise. PSRR is a measure of circuit’s power supply rejection expressed as a ratio of output noise to noise at the power supply input. It provides a measure of how well a circuit rejects ripple at various frequencies injected from its input power supply. In the case of a LDO, it is a measure of the output ripple compared to the input ripple over a wide frequency range and is expressed in decibels (dB). The basic equation for PSRR is given in Equation 1:

$$PSRR = 20 \log \frac{Ripple_{Input}}{Ripple_{Output}} \quad (1)$$

Figure 1 explains how noise and PSRR are different from each other. The noise is something which may be internal and external to the LDO whereas PSRR is an internal parameter of the LDO. LDO users generally concentrate on PSRR and not on the self-generated output noise. PSRR rejects noise coming from outside of LDO but there is always noise generated inside the LDO. So an LDO with high PSRR may not be better for noise rejection. The user should always think of both parameters.

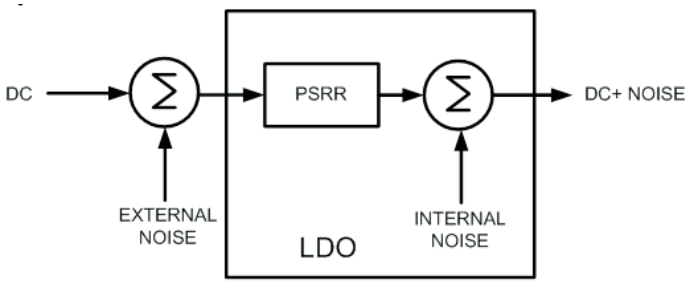

Figure 1. PSRR and Noise in LDO

2 LDO Noise Types

Noise is purely physical phenomenon that occurs with transistors and resistors. Transistors generate shot noise and flicker noise. The resistive element of MOSFETs also generates thermal noise like resistors. Thermal and shot noise is truly random in nature and its power is flat over frequency. It remains flat up to the bandwidth of the amplifier. Flicker noise is the noise due to trapped charges at the gate of the MOSFET. It follows Poisson's Distribution with 1/f roll-off in power versus frequency hence it is higher at low frequencies. This noise dominates until it becomes smaller than thermal noise. (See Figure 2)

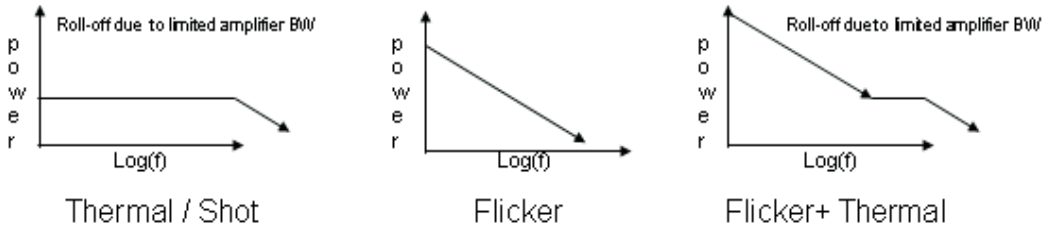

Figure 2. LDO Noise (types)

3 Noise Specifications in LDO Data Sheets

Typically noise in an LDO is specified by datasheets in two fashions. One is "Total (Integrated) output noise – in μVrms", which is RMS value of the spectral noise density integrated over a finite frequency range. The second method is to show a "Spectral Noise density curve – in $\mu V/\sqrt{Hz}$", which is a plot of Noise density vs Frequency. Figure 3 shows both the specifications for TPS717xx series LDOs.

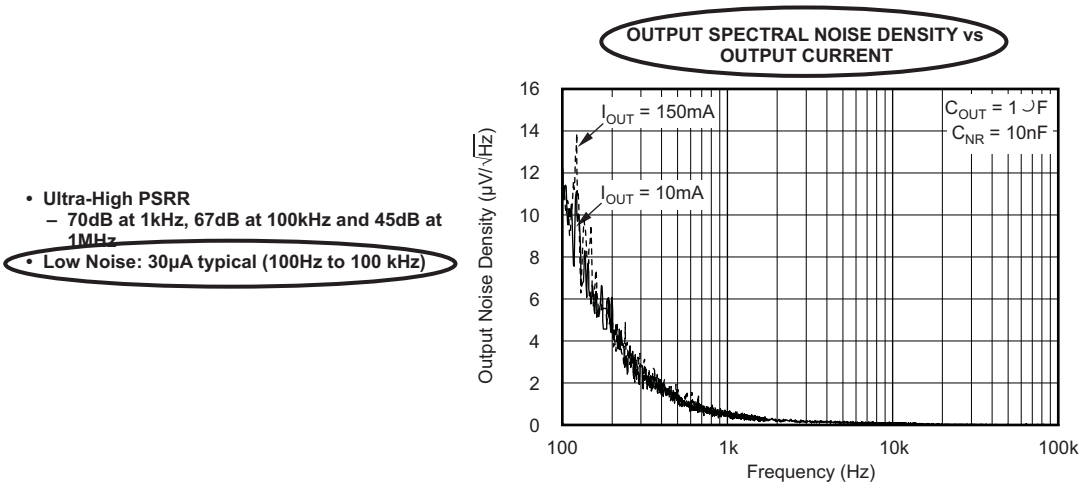

Figure 3. Noise Specified in Two Ways (for TPS717xx LDOs)

Since the output noise voltage is specified by a single number, it is very useful for comparison purposes. When noise specifications of different LDOs are compared, it is imperative that the two regulators' noise measurements be taken over the same frequency range and at the same output voltage and current values.

4 Which Specification is for Your Application?

The user should know which noise specification of the LDO is to be used in the application, because there are some application where the Spectral noise density is pertinent and some applications where total (integrated) noise can be used. The following examples explain this.

1. Consider an RF system, where an LDO powers a Voltage Controlled Oscillator (VCO). VCO takes two input signals and mixes them together. If the two signals are sin(ω1t) and sin(ω2)t, then the result is two outputs sin((ω1–ω2)t), sin((ω1+ω2)t) and harmonics. The RF signal chain following the VCO is typically a band-pass system tuned for only one frequency, that means, only higher frequency remains after mixing. Most broadband applications have very tight regulation on the frequency spectrum and the power in each band. For any band, the spurious noise has to be controlled to meet what is called the "transmit mask". This mask is very important for agency certification of the final product. Any humps in the noise floor at higher frequencies may cause the transmitted signal to be outside of the transmit mask and thus fail the certification testing.

   Now if the noise is present on the conductors that are supplying power or in the LDO output then that noise at a frequency, FR, gets mixed with the carrier frequency and produces two sidebands as shown in the Figure 4. If the noise is so high that the sideband produced due to noise is out of transmit mask then it results in failure of the system.

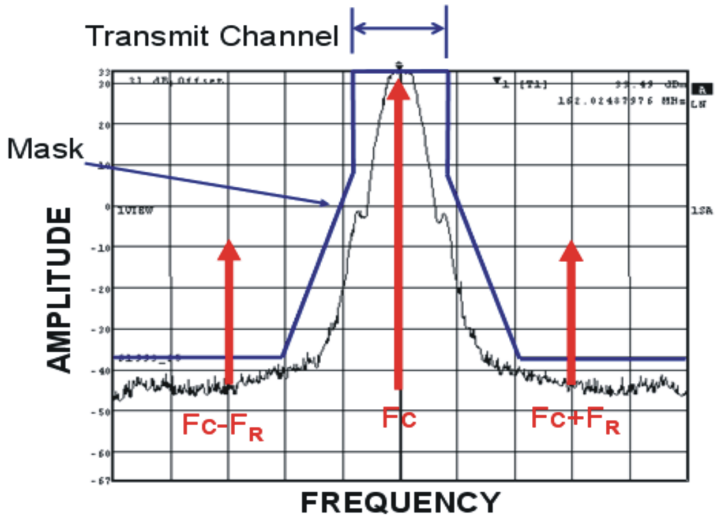

Figure 4. Transmit Mask and Sidebands Due to Noise

Also, if we assume that the RF system is working at a frequency of 2.4GHz, then LDO noise contributes to the VCO noise spectrum both above and below 2.4GHz with up to bandwidth of LDO. The LDO noise shown in Figure 2 adds to the original VCO noise plot which increases the VCO noise floor level around the center frequency.

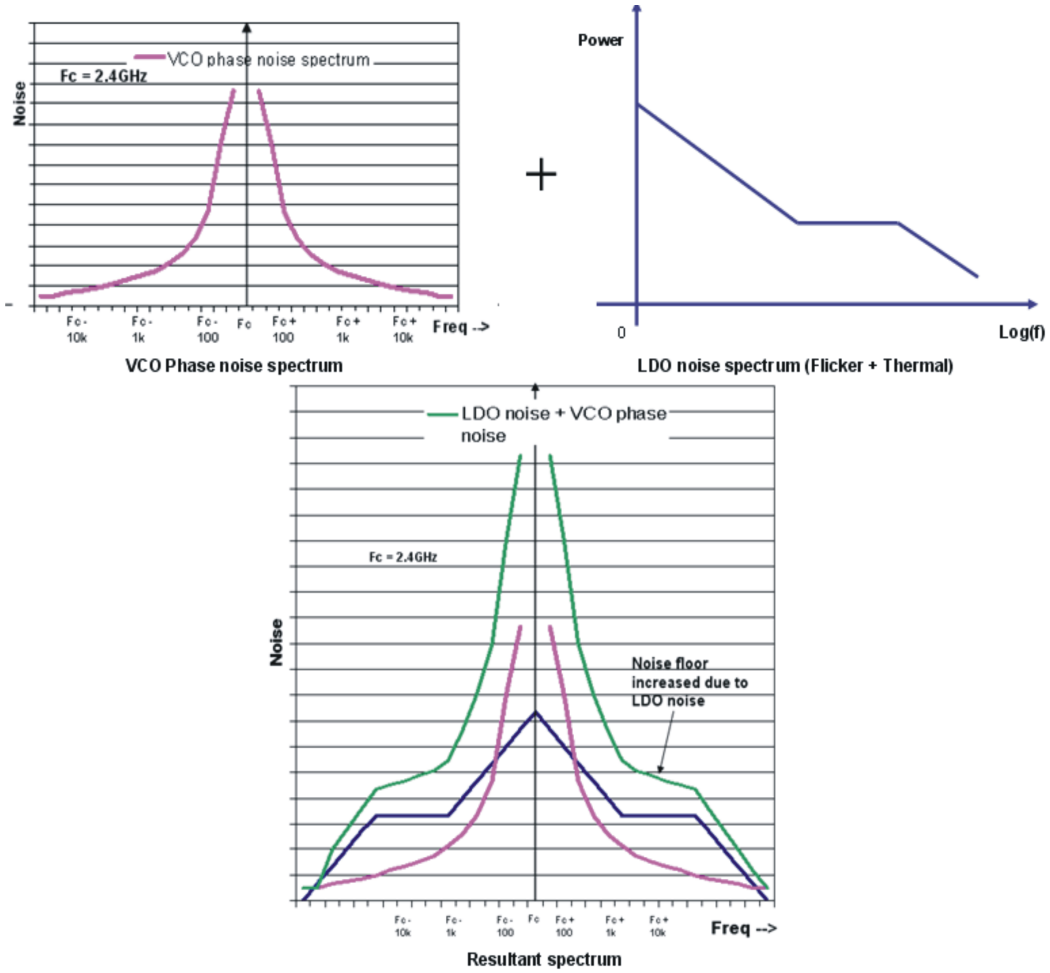

Figure 5. Increase in VCO Noise Floor Due to LDO Noise

So in this RF application the user should use Spectral Noise Density curve since the single noise number loses the frequency dependence and would not be an accurate representation of the final output.

2. Consider a system in which LDO is powering an ADC or DAC. Any sampled system causes the high frequency noise to fold to lower frequencies due to aliasing. For example, if the sampling frequency is 100kHz and the noise due to LDO is at 90kHz and 110kHz, 190kHz and 210kHz, etc., then all the noise will fold back to 10kHz which is the beat frequency. This will occur for any frequency of the output noise so that all of the LDO noise folds back to within the bandwidth of the sampling system. This is same as integrating all the noise from DC to bandwidth of the system and computing the total noise. This way, the performance of ADC/DAC suffers if the LDO total (integrated) noise is high. Figure 6 below shows how LDO noise aliasing takes place. First graph is for a system powered by ideal LDO, second is for a system powered by LDO with thermal noise that increases noise floor and third is for a system powered by LDO with noise at high frequency that aliases to lower frequency.

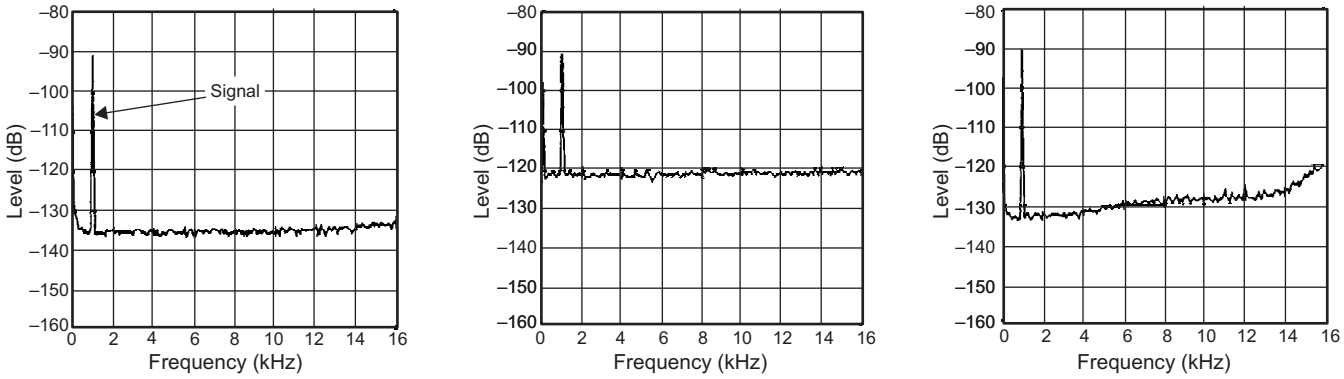

Figure 6. LDO Noise Aliasing

So in this application, the user can use Total (Integrated) output noise since all of the noise will be folded in frequency and integrated by the system.

5 How to Reduce the LDO Noise?

The primary noise source in the LDO is the band gap. The noise in LDO can be reduced using two methods. The following discussion explains both the methods.

One method to reduce the noise is by reducing the bandwidth of the LDO. This can be done by lowering the bandwidth of error amplifier inside the LDO. But if we reduce the bandwidth of error amplifier then it reduces the transient response of the LDO.

Another method is by using a low-pass filter (LPF). As we know, the most dominant source of noise in an LDO is the internal band gap. A LPF can be inserted between the band gap output and the input of the error amplifier. This reduced the band gap noise before it is gained up by the error amplifier. Typically this LPF is formed with a large internal resistor and an external capacitor. The cutoff frequency of this filter is set as low in frequency as possible to filter out nearly all of the noise coming from the band gap.

There is always the question “Why the huge power pass element (mostly FET), which takes up most of the total die area, is not a primary noise contributor?” the answer is the lack of gain. The primary noise source, the band gap, is connected to the input of the error amplifier and thus amplified by the gain of the error amplifier. As we know, the procedure to find the output noise is first refer each noise contributor to the op-amp input; so to find the noise from the pass FET you would first divide the noise contribution by the open-loop gain that exists between it and the error amplifier input. This gain is very large; therefore, the noise contribution from the pass FET is usually negligible.

To summarize, the LDO noise and PSRR both are important specifications to be taken into account when selecting the LDO. There are two ways the LDO noise is specified, and the user should look for the appropriate specification for their application.

6 Implications of the LDO Noise

Let us take an example of a DC-DC Converter with integrated LDOs (such as TPS57140-Q1).

The bandgap noise that is internal to the LDO regulator becomes a limiting factor in the rejection of high frequency components. One of the example where its bad affect can be seen is when a a fast-falling input transient is applied at the input of the DC/DC converter. During the fast input falling edge, if the slew rate of the input is higher than a particular value, the internal LDO regulator of the device resets because of the power-supply rejection-ratio (PSRR) limitation. The fast transition corresponds to higher frequencies. The bandgap noise that is internal to the LDO regulator becomes a limiting factor in the rejection of high frequency components. For example, using the TPS57140- Q1 design simulation and bench test measurement, the resulting slew-rate value measured is 1.2 V/μs. If the slew rate is higher than this value, the device gets disabled and regenerates a soft start. Higher ESR of the input capacitor negatively affects the slew rate of the input voltage and the duration of this rate because of high current transient across the ESR according to ESR × C × dV/dt. Therefore, the use of a low-ESR ceramic capacitor is recommended.

Refer to *Design Considerations for DC-DC Converters in Fast-Input Slew Rate Applications* (SLVA693) for more information

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2009) to A Revision	Page
• Added *Implications of the LDO Noise* section	6

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265