Application Report
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Using TLV320AIC3x Digital Audio Data Serial Interface With Time-Division Multiplexing Support

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ABSTRACT

This application report describes how to configure the time-division multiplexing mode in TLV320AIC3x codec devices and discusses the associated protocol timing diagram for the I²S and DSP modes of operation with various offset programmability. This document also explains how to interface and communicate multiple TLV320AIC3x devices using single audio data interface with the host/multimedia processor.

Contents

List of Figures

List of Tables

1 Introduction

In the TLV320AIC3x audio codec, audio data is transferred between the host/application processor and the TLV320AIC3x codec via the digital audio data serial interface. The data serial interface on this device is flexible, including left- or right-justified data options, support for I^2S or DSP protocols, programmable data length options, time-division multiplexing (TDM) mode for multichannel operation, flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The TLV320AIC3x supports all the features shown in Table 1 for configuring digital audio serial data interface, giving this codec the flexibility to interface with any host/application processor in a system.

Table 1. Digital Audio Serial Data interface Configuration Settings

S.No.	Programmable Feature Supported	Control Register
1	Bit Clock Direction (Input/Output) Control	Page00H/Reg08H Bit D7
2	Word Clock Direction (Input/Output) Control	Page00H/Reg08H Bit D6
3	Digital Audio Serial Data Interface Protocol(I^2S/LJF/RJF/DSP)	Page00H/Reg09H Bits D7–D6
4	Digital Audio Serial Data Word Length	Page00H/Reg09H Bits D5–D4
5	Offset Programmability (0 to 255 bit clock cycles)	Page00H/Reg0AH Bits D7–D0
6	3-stating DOUT line for the unused bit clock cycles.	Page00H/Reg08H Bit D5
7	If Bit/Word Clock is programmed as output, then generating them even CODEC is powered down.	Page00H/Reg08H Bit D4
8	If Bit Clock is programmed as output, then programming number of bit clock cycles/frame, which needs to be generated.	Page00H/Reg09H Bit D3
9	5-wire I^2S interface support for enabling different sample rates for the ADC and DAC.	Page00H/Reg62H Bits D7–D4

The following sections of this application report describe in detail how to configure the TDM mode and present the associated protocol timing diagrams for the I^2S and DSP modes of operation with various offset programmability. Also explained is how to use the 3-state mode in the DOUT line for the unused bit clock cycles and how to interface and communicate multiple TLV320AIC3x devices using a single audio data interface.

2 Programmable Offset Support

The TLV320AIC3x codec has a programmable offset feature which can be configured to any value from 0 to 255 using Page-00H/Reg-0AH, regardless of master/slave configurability of the bus clock line. But the programmed offset value should be ≤ (the number of bit clock cycles per frame – programmed word length for the data).

By changing the programmable offset, the bit clock cycle in each frame at which the data begins can be changed. The serial data output driver (DOUT) can also be programmed for a 3-state mode during all bit clock cycles other than cycles at which valid data is being put onto the bus. This allows other TLV320AIC3x codecs to be programmed with different offsets and to drive their data onto the same DOUT line, just in a different slot. For incoming data, the TLV320AIC3x simply ignores data on the bus except where it is expected, based on the programmed offset.

2.1 I²S Mode Protocol Timing With Different Offset Settings

Case 1: Number of bit clock cycles per channel is equal to the programmed word length (n) for the data. If TLV320AIC3x is programmed to generate the bit clock, then this case will arise if Page00H/Reg09H Bit D3 is programmed to 0 which is also named as continuous transfer mode in TLV320AIC3x product data sheets.

A: I^2S timing with offset = 0. This is similar to standard I^2S timing.

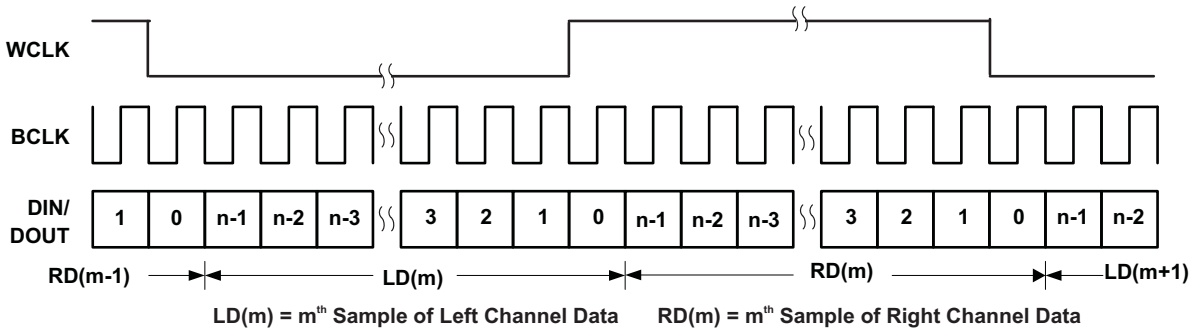

Figure 1. I²S Timing With Offset = 0

B: I²S timing with offset = 2.

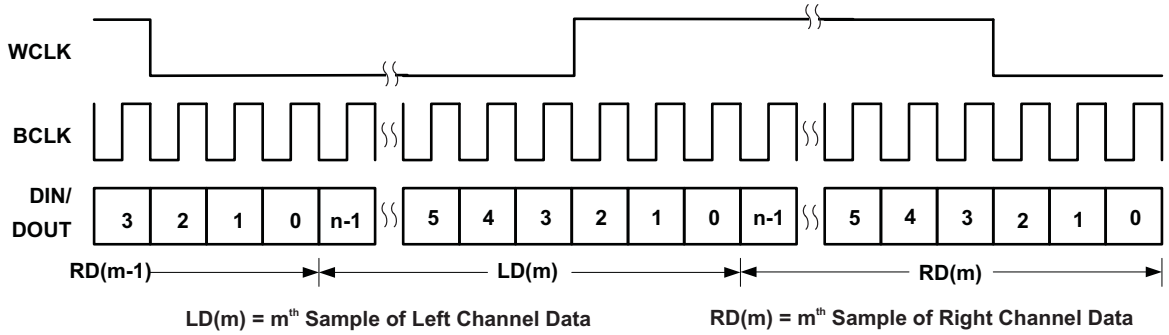

Figure 2. I²S Timing With Offset = 2

C: I²S timing with offset = n–1, where n is the programmed word length for the data.

Note : In this case, the I²S mode timing is equivalent to the left-justified timing with offset = 0.

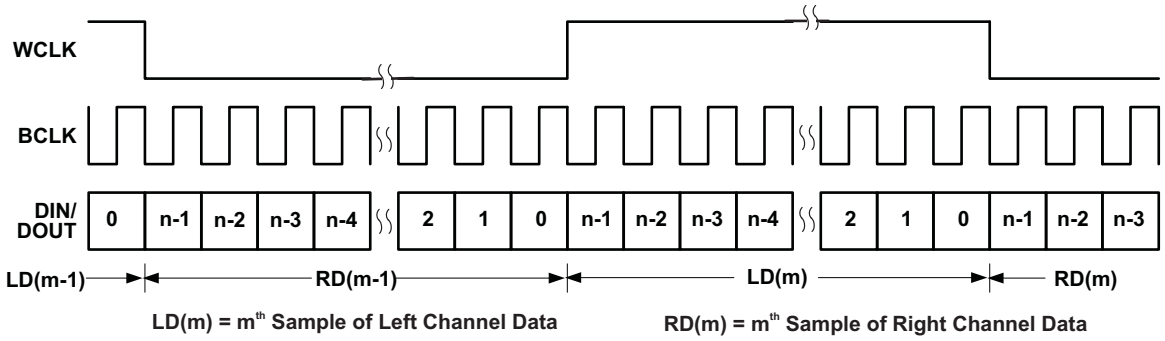

Figure 3. I²S Timing With Offset = n–1

D: I²S timing with offset = n, where n is the programmed word length for the data.

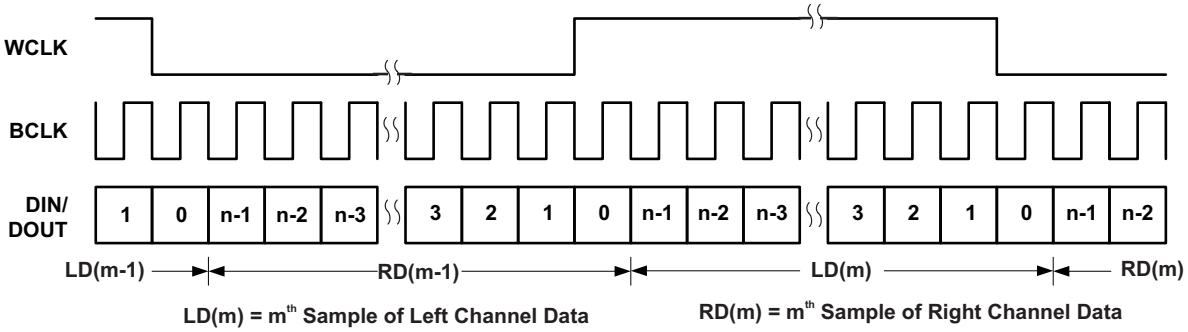

Figure 4. I²S Timing With Offset = n

Note : In this case, the I²S mode timing is equivalent to as if the I²S timing with offset = 0 and the word clock signal is inverted.

Case 2: Number of bit clock cycles per channel is greater than the programmed word length (n) for the data. If TLV320AIC3x is programmed to generate the bit clock then this case will arise if Page00H/Reg09H Bit D3 is programmed to 1 which is also named as 256-clock transfer mode in TLV320AIC3x product data sheet.

A: I²S timing with offset = 0. This is similar to standard I²S timing.

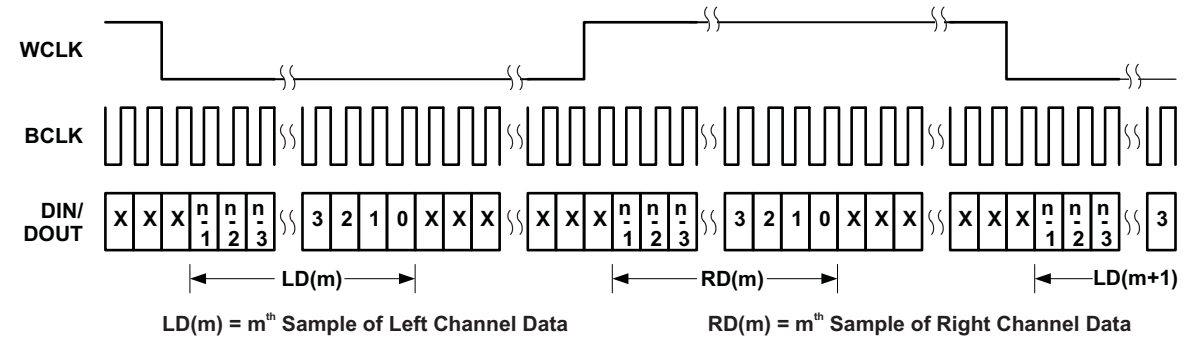

Figure 5. I²S Timing With Offset = 0 and Extra Bit Clock Cycles

B: I²S timing with offset = 2.

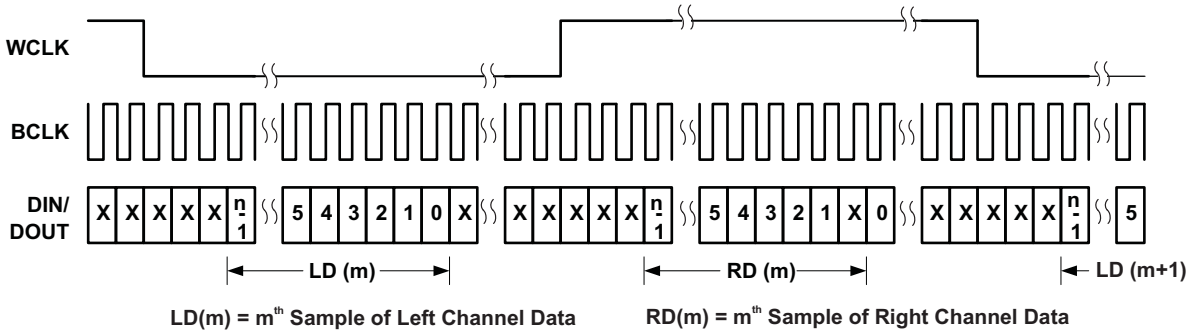

Figure 6. I²S Timing With Offset = 2 and Extra Bit Clock Cycles

2.2 DSP Mode Protocol Timing With Different Offset Settings

Case 1: Number of bit clock cycles per channel is equal to the programmed word length (n) for the data. If TLV320AIC3x is programmed to generate the bit clock then this case will arise if Page00H/Reg09H Bit D3 is programmed to 0 which is also named as continuous transfer mode in TLV320AIC3x product data sheet.

A: DSP mode timing with offset = 0. This is similar to standard DSP mode timing.

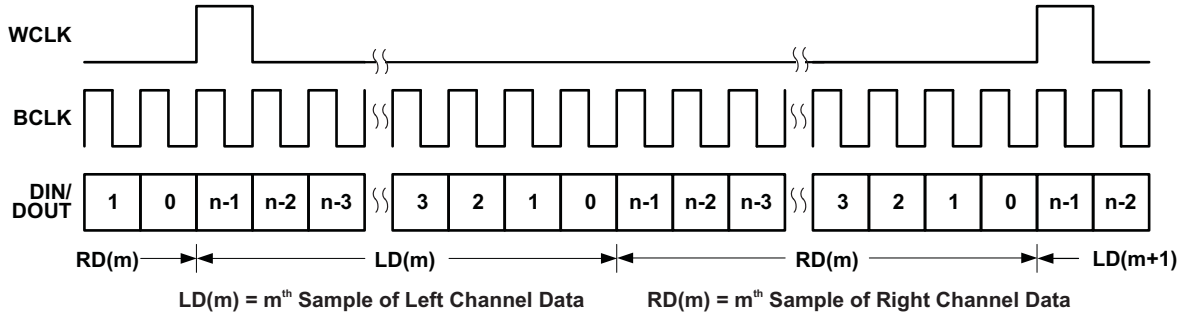

Figure 7. DSP Mode Timing With Offset = 0

B: DSP mode timing with offset = 2.

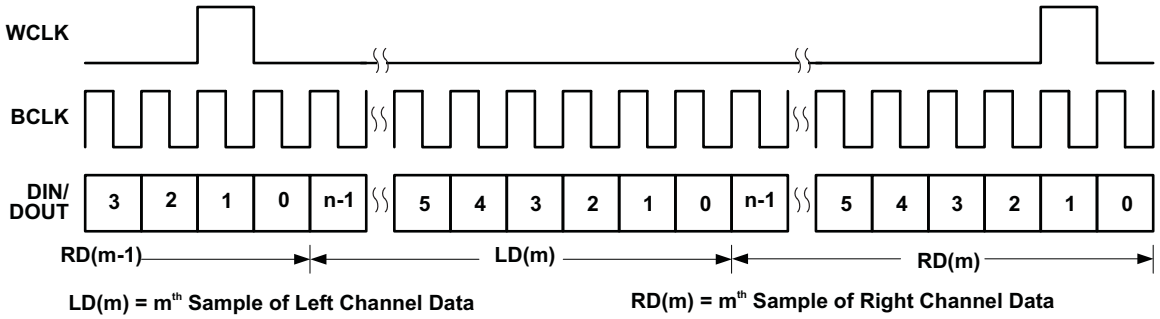

Figure 8. DSP Mode Timing With Offset = 2

C: DSP mode timing with offset = n–1, where n is the programmed word length for the data.

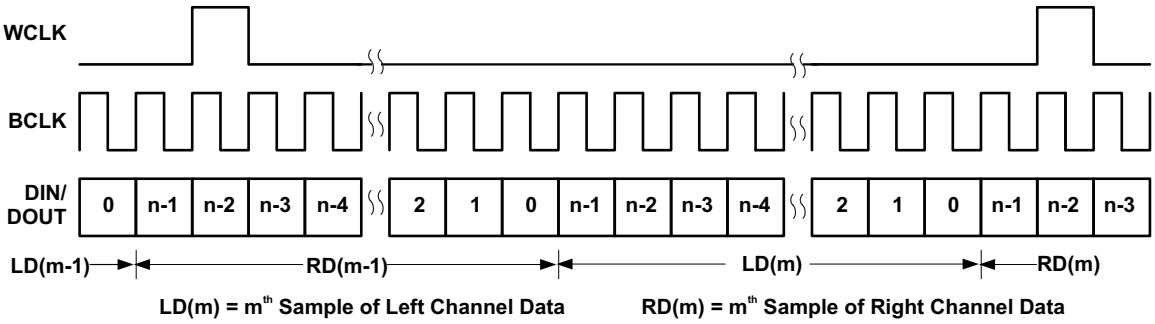

Figure 9. DSP Mode Timing With Offset = n–1

D: DSP mode timing with offset = n, where n is the programmed word length for the data.

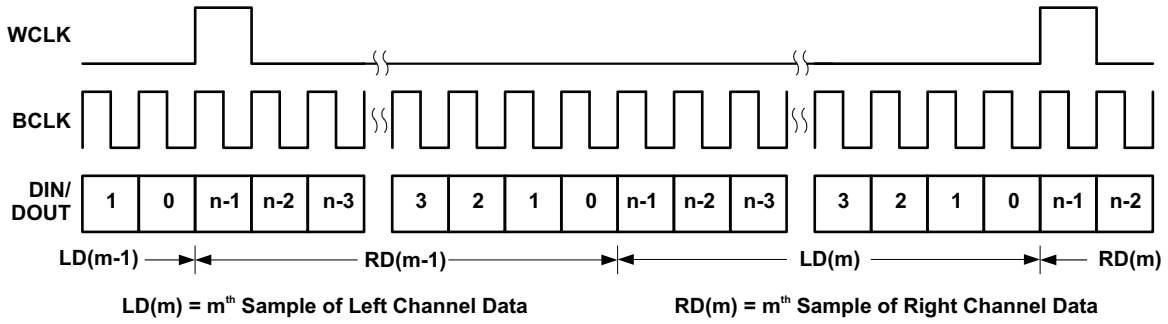

Figure 10. DSP Mode Timing With Offset = n

Case 2: Number of bit clock cycles per channel is greater than the programmed word length (n) for the data. If TLV320AIC3x is programmed to generate the bit clock, then this case arises if Page00H/Reg09H Bit D3 is programmed to a logic 1 which is also called a 256-clock transfer mode in TLV320AIC3x product data sheet.

A: DSP mode timing with offset = 0. This is similar to standard DSP mode timing.

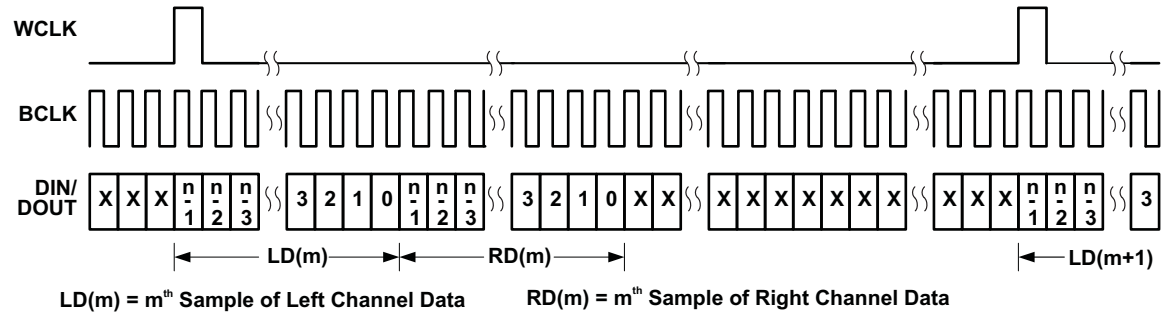

Figure 11. DSP Mode Timing With Offset = 0 and Extra Bit Clock Cycles

B: DSP mode timing with offset = 2.

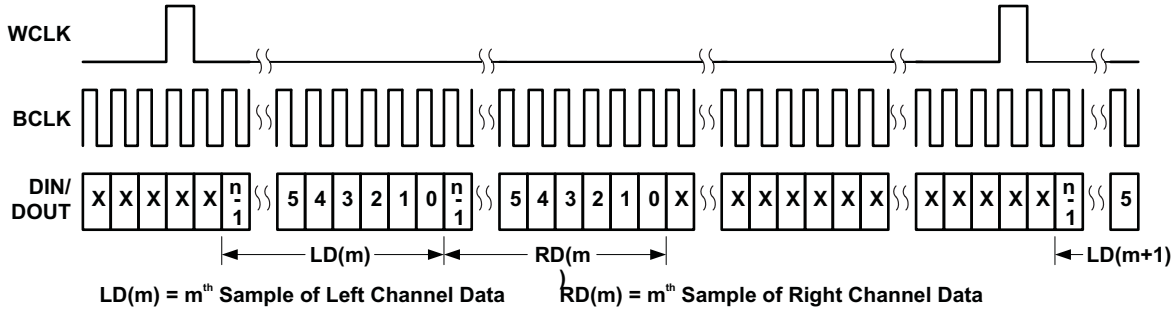

Figure 12. DSP Mode Timing With Offset = 2 and Extra Bit Clock Cycles

Also, if the programmed offset is not equal to zero, then in the case of I^2S mode or left-justified mode, the number of **bit clock cycles per channel** should be greater than or equal to the programmed word length for the data, whereas in DSP mode, the number of **bit clock cycles per frame** should be greater than or equal to two times the programmed word length for the data. This constraint is needed to satisfy the proper data transfer of both channels. Also, it is recommended that the right-justified mode not be used if the programmed offset is not equal to zero and if that is needed, then it can be simply achieved indirectly by using either I^2S or left-justified mode with the necessary offset programming.

3 Entering the DOUT Line in 3-State Mode for the Unused Bit Clock Cycles

Furthermore, with offset programmability, TLV320AIC3x also supports the 3-state mode for the serial data output driver (DOUT) during all bit clock cycles other than cycles at which valid data is being placed on the bus. For example, the previously mentioned Case 2 for I^2S and DSP modes has a lot of unused bit clock cycles where the DOUT lines are having invalid unknown data; so, by programming TLV320AIC3x control register Page-00H/Reg-08H bit D5 = 1 during these invalid unknown data slots, the TLV320AIC3x places the DOUT line in a 3-state mode as shown in Figure 13 and Figure 14.

A: I^2S timing with offset = 0 and also DOUT 3-state programmability is enabled.

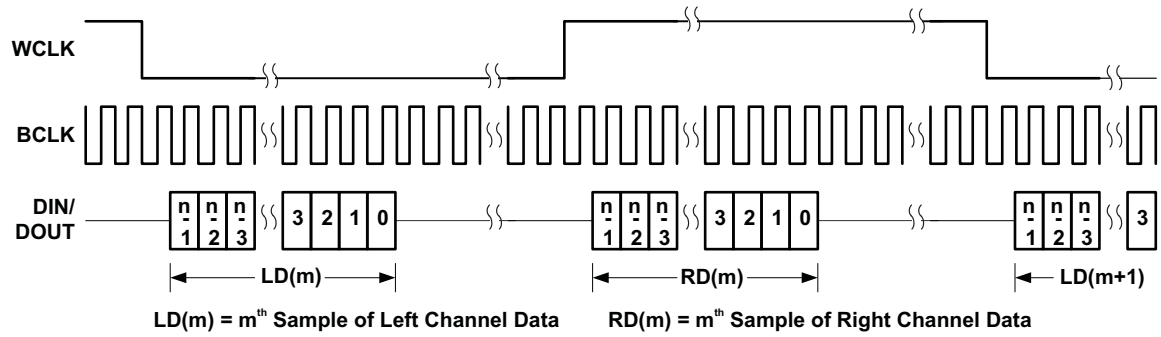

Figure 13. I^2S Timing With DOUT 3-State Programmability

B: DSP mode timing with offset = 2 and also DOUT 3-state programmability is enabled.

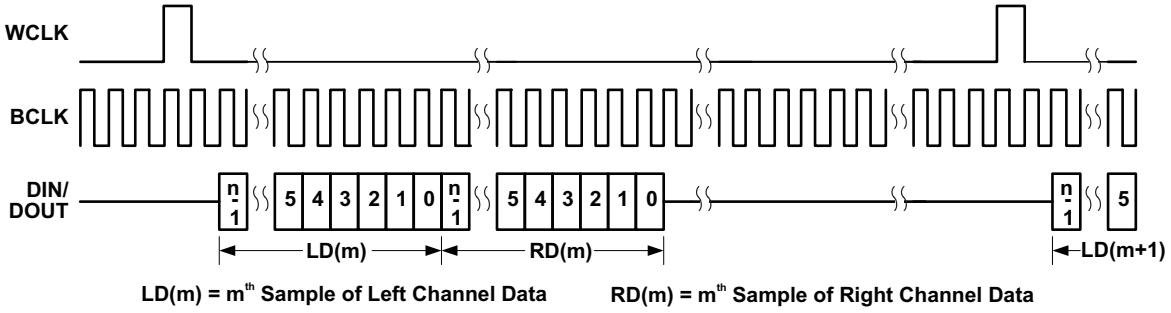

Figure 14. DSP Mode Timing With DOUT 3-State Programmability

Moreover, the on-chip bus keeper is integrated on the DOUT line which is always active by default. When the DOUT line is not being driven by any devices, then this active bus-keeper circuitry keeps the DOUT line at the logic level that was most recently driven. Thus, on-chip bus keepers reduce the static power dissipation caused by a floating/3-state mode DOUT line and also eliminate the need for external bias resistors on the DOUT line needed for pullup and pulldown.

4 Interfacing Multiple Codecs Using Single Digital Audio Serial Data Interface

Using the offset programmability and the DOUT line 3-state feature, the TLV320AIC3x enables the flexibility where multiple TLV320AIC3x devices can be interfaced together and can communicate to host/multimedia processor using a single digital audio serial interface. By changing the programmable offset, the bit clock in each frame where the data begins can be changed, and the serial data output driver (DOUT) also can be programmed to a 3-state mode during all bit clocks except when valid data is being put onto the bus. This allows other codecs to be programmed with different offsets and to drive their data onto the same DOUT line, just in a different slot. For incoming data, the codec simply ignores data on the bus except where it is expected based on the programmed offset.

Shown in Figure 15 is an application example in which OMAP5912 Multimedia Processor is transmitting/receiving the serial digital audio data with multiple TLV320AIC3x using single digital audio serial interface. For further details regarding interfacing TLV320AIC3x, see the OMAP5912 reference guide (SPRU762).

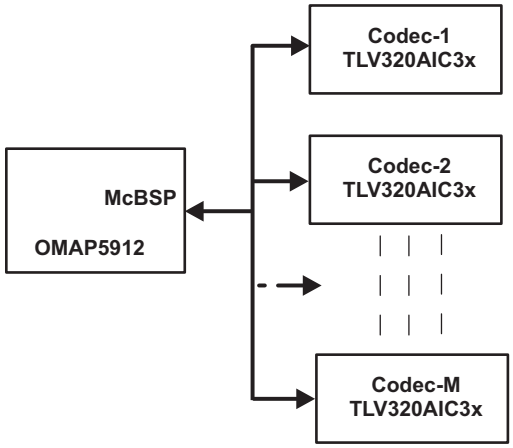

Figure 15. Interfacing Multiple TLV320AIC3x Devices Using Single I²S Interface

The digital audio serial interface timing diagram for the interface in Figure 15 is shown in Figure 16. In this particular configuration, TLV320AIC3x is programmed for I²S mode with n-bit word length. The offset programmed for the codec-1 is 0, for codec-2 it is n, and likewise, the offset programmed for the codec-M is (M-1) x n. Also, the DOUT line 3-state feature is enabled for all the CODEC.

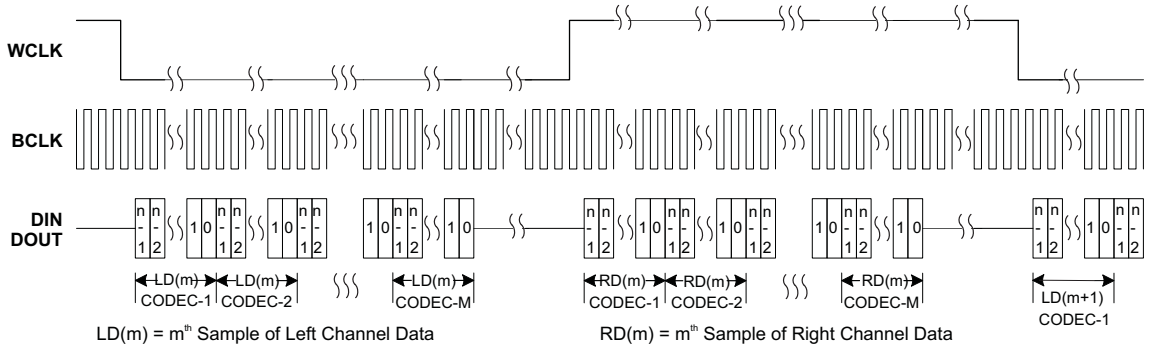

Figure 16. I²S Timing for Multiple TLV320AIC3x Devices Interfaced Together

5 References

1. *TLV320AIC33, Low Power Stereo Audio Codec for Portable Audio/Telephony* data sheet (SLAS480).
2. *OMAP5912 Multimedia Processor Multichannel Buffered Serial Ports (McBSPs) Reference Guide* (SPRU762).
3. *Using TDM Function to Interface Four TLV320AIC33 Codecs With a Single Host Processor* application report (SLAA301)
4. I²S Bus Specification (http://www.semiconductors.philips.com/acrobat_download/various/I2SBUS.pdf).

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