![Texas Instruments logo]

Evaluation Board for the TLC320AD545 DSP Analog Interface Circuit

Ziad Asghar   *Mixed Signal Products*

ABSTRACT

This application report discusses the design of the AD545EVM evaluation board and its use to demonstrate the performance of the TLC320AD545 (AD545) analog interface circuit. The TLC320AD545EVM interfaces to a 'C54x DSK+ board to allow the user to evaluate the performance of the device.

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1 Introduction

The TLC320AD545 provides high-resolution low-speed signal conversion from digital to analog (D/A) and from analog to digital (A/D) using oversampling sigma-delta technology. This device consists of two serial-synchronous conversion paths (one for each data direction), and includes an interpolation filter before the DAC and a decimation filter after the ADC. Other overhead functions provide on-chip timing and control. The sigma-delta architecture produces high-resolution analog-to-digital and digital-to-analog conversion at low system speeds and low cost.

The options and circuit configurations of this device can be programmed through the serial interface. The options include reset, power down, serial clock rate, gain control, and test mode. The TLC320AD545 is an analog interface circuit (AIC) with many features that make it suitable for DSP-based applications:

- Single 5-V/3.3-V supply

- 16-bit resolution sigma-delta ADC and DAC

- Hybrid operational amplifiers

- 8-Ω AT41 differential speaker driver with programmable-gain amplifier

- Flash write-enable circuit provides power to write the flash memory device

- Transformer reference (2.5-mA source and sink at 2.5 V for a 5-V supply. and 1.5 V for a 3.3-V supply) to allow single-ended driving

- 79-dB (min) signal-to-noise

- Inherent antialiasing filtering and sin(x)/x compensation

- High input impedance

- Low operating power (120 mW typical)

- Power-down mode (20 mW max)

- Available in 48-pin PT (TQFP) package operating from –40°C to 85°C

1.1 Scope of This Report

This application report discusses the design of the AD545EVM evaluation board and its use to demonstrate the performance of the TLC320AD545 (AD545) analog interface circuit.

The objective is to design a development board (the AD545EVM) which allows the users of the AD545 to determine its capabilities with minimum effort. The board can be directly connected to the low-cost TMS320C54x DSP starter kit (DSK+), or to any other system with a compatible synchronous serial interface. Directly compatible DSP devices include the TMS320C2x, 'C2xx, 'C3x, 'C5x, 'C54x, and 'C6xxx. An example program is provided for the DSK+ development system which allows the board to be used as a sine-wave generator, or to output to the DAC samples read out from the ADC. Signal processing functions such as filtering can easily be included in this echo mode.

1.2   Block Diagram of AD545EVM

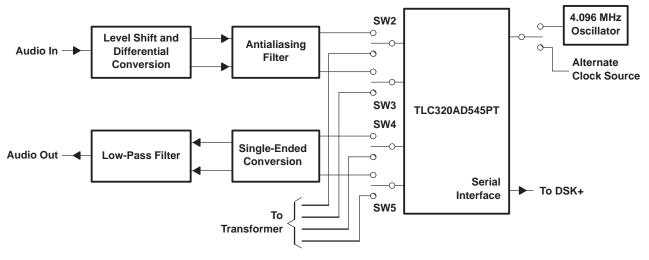Figure 1 shows the block diagram of the AD545EVM evaluation board.

Figure 1. AD545EVM Block Diagram

1.3   Special Considerations When Using Sigma-Delta Converters

Sigma-delta analog-to-digital converters typically consist of an analog modulator (second-order in the case of the AD545) followed by a digital-filter section. The modulator contains a 1-bit ADC (a comparator) that produces a 1-bit wide data stream which is applied to the input of the digital filter. The data stream is also applied to the input of a 1-bit DAC, the output of which is fed back to the input of the modulator. The 1-bit ADC is clocked much faster than the desired output sampling frequency FS (128 x FS for the AD545), and the large amount of quantization noise generated is uniformly spread over a wide range of frequencies. A noise-shaping filter within the analog modulator reduces the noise in the pass-band, increasing it elsewhere. A low-pass digital filter then removes the unwanted high-frequency quantization noise and the signal is resampled at the desired output frequency.

The sigma-delta DAC in the AD545 consists of a digital interpolating filter operating at 128 x FS, followed by a 1-bit DAC and a second-order modulator. The digital filter removes most of the image frequencies which would otherwise be present at the output of a conventional DAC. This makes a high-order analog low-pass reconstruction filter unnecessary. There is no need for separate sin(x)/x compensation, as this is inherent in the DAC architecture. Sigma-delta converters have several advantages and a few disadvantages relative to other types of ADCs, as indicated in the following summary.

Advantages:

*   Sigma-delta conversion is inherently linear because there is no reference resistor chain, as in the case of flash or successive-approximation converters. This results in extremely-low distortion.

*   Inherent monotonicity

- No missing codes

- Antialiasing filtering is inherent within sigma-delta converters. This greatly simplifies their application because only a simple external RC filter is required at the input of the ADC to achieve the necessary alias rejection.

- The digital filters, which form an integral part of the ADC and DAC, are usually of the finite impulse-response type offering a linear-phase characteristic with high stability.

- The cutoff frequency of the digital filters automatically tracks the sampling rate.

- DAC anti-image filtering is greatly simplified because an internal digital filter attenuates image frequencies. A simple analog filter is sufficient to remove HF noise.

- No need for sin(x)/x compensation

- The sigma-delta architecture is compatible with dense, low-cost, digital IC processes.

Disadvantages:

- The digital filters in sigma-delta converters introduce a time delay into the conversion process making them unsuitable for some control applications. The AD545 ADC has a 17-sample delay, and the DAC has an 18-sample delay.

- Audio-band converters are optimized for ac signals, and a small dc offset may be present.

- Spurious low-level tones can sometimes occur at very low input-signal levels, especially if clock signals at FS/2 are allowed to couple into the reference voltage pins. Such tones can be identified because their frequency is affected by small changes in dc offset.

1.4 AD545 Clock Rates, Bandwidth, and Voltage Reference

The AD545 works only in the master mode, and hence it provides the FS and SCLK signals to the DSP. The sampling rate FS of the AD545 is equal to MCLK/512. The SCLK rate is given by: SCLK = FS X 256 = MCLK/2. The 3-dB bandwidth of the ADC and DAC channels is 3.6 kHz at 8-kHz sampling rate. The bandwidth scales linearly with the sampling rate. The AD545 has two FS modes; either one of the modes can be selected using the switch labeled SW1.

The DT_REF pin produces a reference voltage at 2.5 V for a 5-V supply, and 1.5 V for a 3.3-V supply. The maximum source or sink current at this terminal is 2.5 mA.

2 AD545EVM Design and Construction

2.1 PCB Construction

The AD545EVM printed-circuit board is of a 4-layer construction with ground and power planes sandwiched between the top and bottom signal-carrying layers. This minimizes RF noise coupling into the system by providing very low impedance to power and ground, and by shielding signal tracks. The AD545 is available in a TQFP surface-mount package. This 48-pin package is very suitable for PCMCIA and other miniature applications.

The printed-circuit board is of the same size as the DSK+ board. The AD545EVM and the DSK+ can be stacked one above the other using interboard links. Either board can be on top, but placing the AD545EVM on top gives better access to the EVM test points.

A separate connector labeled SERIAL has been provided for interfacing to systems other than the DSK+. This brings out the SCLK, FS, DIN, and DOUT signals. Each signal is interleaved with a ground conductor in the ribbon cable, allowing a longer cable length without crosstalk. Nevertheless, this cable should be as short as reasonably possible, since ringing in the unterminated cable may become excessive for cable lengths greater than about one meter. To minimize RF emissions, the cable should be shielded and the shield connected to the ground plane at the ground point provided adjacent to pins 1 and 2 of the connector. This connector should not be used simultaneously with the connections around the edge of the AD545EVM board, which are specifically intended for the DSK+.

The ground plane of the AD545EVM is channeled to prevent digital-noise currents from inducing noise voltages in the analog ground of the device. The DSK+ has ground and power pins along both edges of the board, making the use of split-ground planes ineffective. Instead, channeling is used on the ground plane to separate the analog and digital grounds and to reduce the common impedance.

2.2   Power Supply

The AD545EVM board is designed to use a single positive-power supply. The board can run at either +5 V or +3.3 V. These are the two voltage levels at which the AD545 operates. All other components can also function at these voltage levels. See the analog input and output stage description for further details. When the AD545EVM is connected to the DSK+, it can not be operated with a 3.3-V supply because the two boards share their digital grounds and the DSK+ operates at 5 V.

The AD545EVM uses the power from the connector labeled PSU PWR, and then splits it into an analog supply (PAVDD) and a digital supply (DVDD). The power plane is split to keep the digital and analog supplies separate.

2.3   System Clock

When the AD545EVM is used in stand-alone mode, a crystal oscillator module must be fitted to the socket provided. A frequency of 4.096 MHz is suggested, as this will allow a standard sampling frequency of 8 kHz. In stand-alone mode, the AD545EVM can be clocked at frequencies up to 5.632 MHz. The AD545EVM is provided with a 4.096-MHz oscillator. To provide this clock to the AD545, the jumper labeled clock B should be closed.

Alternatively, the DSK+ and AD545EVM clocks can be separated by opening the jumper labeled Clock A. This prevents the clock from being transmitted between the boards. This mode allows the AD545 and the DSP to use separate clocks. It is important to ensure that only one oscillator is used in the system (except as described above); otherwise, the results may be unpredictable. No damage will be caused, however, as current limiting resistors are provided on the output of each oscillator.

A third option is to run the AD545 using the CLKOUT from the DSP. This can be accomplished by closing the jumper labeled Clock C. Since the AD545 allows a maximum MCLK rate of 5.632 MHz, the only option is to set pins CLKMD1, CLKMD2 and CLKMD3 so that the 10-MHz clock provided with the DSP is divided by two (see the following note). This mode could not be checked in laboratory tests because the HPI port used to interface the DSP to the PC on the DSK+ cannot function at such a low frequency. Hence, this option can be used in the stand-alone mode to use an alternate clock source. See Table A–2.

NOTE: CLKMD1, CLKMD2, and CLKMD3 can be accessed through pins 17, 18, and 16, respectively, on the connector labeled JP4. The default positions of the CLKMD pins on the DSK+ are 110, corresponding to CLKMD1, CLKMD2, and CLKMD3. This means that the DSP runs at four times the clock provided on the CLKIN pin. Manipulating these pins allows the user to run the DSP using a slow clock by multiplying it by a suitable factor. This should be done with caution because CLKMD3 is connected to ground via a 0-ohm resistor, and pulling it high could short the DSK+, unless resistor (R37) on the DSK+ is removed. See the TMS320C542 data sheet for more details.

2.4   Serial Port Interfacing

The AD545EVM has been designed to interface to the same synchronous serial port used by the AC01 on the DSK+ system. This is achieved by sharing the serial clock, frame sync, and data signals, and by powering down the AC01. Connecting the AD545 EVM to the DSK+ powers down the AC01 on the DSK+. The additional connectors labeled *Serial* can be used to interface the AD545 to another type of DSP system.

2.5   Transformer Interface

In a typical modem design, the analog-interface circuit interfaces to a transformer via a hybrid. A hybrid is used to implement a 4-wire to 2-wire conversion. The AD545 provides built-in operational amplifiers to implement the hybrid. The AD545EVM board allows the user to input an analog signal, or to interface the AD545 to a transformer by using switches SW2, SW3, SW4, and SW5. Putting the switches in the TXFM position connects the input and output of the AD545 to the transformer. If the switches are left in the *input* or *output* position, they allow the user to apply an analog signal to the AD545 and to read out the analog signal from the output.

The AD545EVM board can also be used in conjunction with a transformerless data access arrangement (DAA), such as the ones provided by CPClare Corporation and Krypton Isolation Incorporated. Depending on whether the hybrid operational amplifiers are needed or not, the transformer interface may be used or the input or output jacks may be used.

NOTE: SW2 and SW3 must be configured as a pair. Similarly, SW4 and SW5 must be configured as a pair.

2.6   Operational Amplifier Selection

The design of the input stage uses operational amplifiers in the inverting configuration. This has the advantage of keeping both inputs at the reference voltage, thus preventing problems with input common-mode range.

Miniature systems often require that analog and digital circuits be in close proximity to each other. This can lead to problems where radio-frequency interference from clock signals or DSP bus lines is demodulated by operational amplifiers, leading to an increased dc offset. If the RF is modulated, that modulation may appear at the operational amplifier output. CMOS and BiFET operational amplifiers can be more resistant to demodulating RF than bipolar devices. Take particular care to keep digital and analog signals away from each other, and be generous with power-supply decoupling and filtering. Power planes greatly reduce system noise.

A Texas Instruments TLC2272 device was selected for this application; this is a LinCMOS dual operational amplifier designed for single-supply operation. It has full rail-to-rail output swing and low distortion. However, the distortion increases when driving loads of about 2 kΩ or less.

2.7 Analog Input Stage

The AD545 uses differential inputs biased at 2.5 V. The maximum code is generated with 1.5 V_{PP} on both differential inputs. The input stage provides the necessary level-shifting and single-ended-to-differential conversion. The input stage is designed to require no negative supply. This limits the maximum input voltage below 1.5 V_{PP} at the *input* jack. If the AD545 is to be tested at 1.5 V_{PP} on both differential inputs, then its input pins can be accessed through the connector labeled ANALOG.
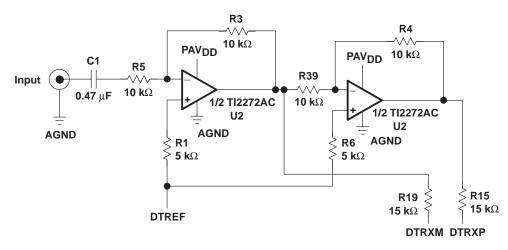

Figure 2. Analog Input Stage to the AD545

The two operational amplifiers are used in the inverting configuration and are biased at 2.5 V for a 5-V supply, and at 1.5 V for a 3.3-V supply by using the DT_REF pin of the AD545.

Sigma-delta converters have the advantage of providing antialiasing filtering as an integral part of their operation. However, this filtering has *holes* at multiples of the oversampling frequency. The AD545 is a 128-times oversampling converter; so, for a 10-kHz sampling rate, the first *hole* will be centered at 1.28 MHz and will be 10-kHz wide. It is important to ensure that no energy of this frequency is present across the codec inputs. A simple single-pole RC filter is sufficient. This filter is implemented using a capacitor (C10) and a resistor (R38) between DTRXM and DTRX_FB.

2.8 Analog Output Stage

The AD545 uses a pair of differential voltage outputs. The output stage converts the differential signals to a single-ended output, and attenuates noise outside the pass-band. This filter is not a conventional reconstruction filter, since the AD545 has an integral low-pass reconstruction filter. This filter is unnecessary in many applications, since it only removes out-of-band noise.
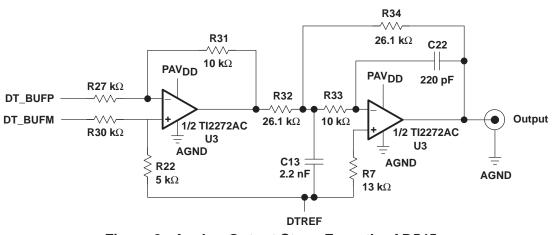
Figure 3. Analog Output Stage From the AD545

The output stage is also designed to eliminate the need for a negative supply for the operational amplifiers. If higher output-voltage levels are to be observed, the AD545 outputs (DT_BUFP and DT_BUFM) can be accessed from the connector labeled ANALOG.

3   Configuring the AD545EVM

Configuring the AD545EVM involves coupling it to the synchronous serial port of a digital-signal processing system. Two configurations are supported. The first is to couple the AD545EVM to a DSK+ development system by means of four connectors, directly linking the circuit boards together. The DSK+ consists of a TMS320C542 16-bit fixed-point digital-signal processor, combined with a 14-bit analog-interface circuit and PC printer-port-compatible data interface. This allows the downloading and debugging of C or assembler programs from a DOS or Windows™ environment. Many example programs are supplied with the DSK+ which can readily be adapted to use with the AD545EVM. The second configuration is the stand-alone mode, where a shielded ribbon cable up to approximately one meter in length connects the AD545EVM to a separate DSP system.

Power to the AD545 EVM is provided through the connectors labeled PSU PWR. The positive supply should be connected to pin 2 of this connector, and ground should be connected to pin1.

3.1   Stand-Alone Mode

To use the AD545 EVM in the stand-alone mode, connect the jumper labeled CLOCK-B to allow the AD545 to use the 4.096-MHz oscillator provided with the board. Switches SW2 and SW3 should be moved (as a pair) to the *input* position to enable a signal to be provided to the AD545 directly. Similarly, the switches labeled SW4 and SW5 should be moved (as a pair) to the *output* position to access the analog output of the AD545 or the transformer interface. The AD545 registers can not be programmed in stand-alone mode, since they are software controlled via the serial interface. The FS, SCLK and MCLK signals can be checked in this configuration. A simple digital loopback is asserted by connecting pins 7 and 9 on the connector labeled *Serial*. This connects the codec's DIN and DOUT together. A certain DOUT may cause the codec to generate a secondary communication FS. With DIN and DOUT connected, FS may also show the secondary FS.

Windows is a trademark of Microsoft Corp.

3.2 Connecting the AD545EVM to the DSK+

Couple the two circuit boards together using the four interboard connectors (JP1, JP3, JP4, and JP5). See *Appendix A* for full details. Power to the AD545EVM is provided through the connector labeled PSU PWR. Inputs and outputs are provided on 3.5-mm stereo jack sockets. Attaching the AD545EVM to the DSK+ automatically powers down the AC01 on the DSK+. It is advisable to have the AD545EVM on top to allow access to any signals. The clocks can be provided according to the previous discussion. This setup allows the user to fully program the device and test its programmability. Note that the SELFTEST program does not function properly now because the AC01 on the DSK+ is powered down.

A sample program is provided with this application report. Type in and assemble a program such as the sine-wave generator listed below, or modify an appropriate example program such as OSCOPE supplied with the DSK+.

3.3 Programming the AD545 Registers

Register 0 is a dummy register, equivalent in principle to a NOP instruction. Writing to it does nothing. Register 1 controls reset, power-down status, digital and analog loopback, and monitor-amplifier signal source, and gain. Register 2 allows control of the analog input and output PGA gain. Register 2 also monitors speaker gain and the ADC overflow indicator.

3.4 Sine-Wave Generator and Loopback Program

The following code is for a sine-wave generator and loopback program that demonstrates how to program the DSK+ to drive the AD545EVM. The sine-wave is generated by means of a cyclically-indexed lookup table. The sine table delivers an output waveform at –3 dB relative to clipping, to allow direct comparison with the levels used in the AD545 data book.

This AD545SIN.ASM program generates a sine wave when the assembler variable *makesine* is set to 1. Otherwise the program reads data from the ADC and copies it to the DAC. Filtering code can be inserted if desired. When *makesine* is set to 1, the registers are programmed so that the AD545 converts the digital data generated by the DSP into analog. Then analog loopback is asserted and the signal at the output of the PGA is sent to the speaker. This fully demonstrates the AD545 operation. When *makesine* is set to 0, the 4 lines that program the AD545 should be changed to comments by placing semicolons at the beginning of the lines, and then the program should be assembled. This configuration requires the use of the registers default values. The program must be edited using a text editor (such as *MSDOS Edit*) and assembled as follows:

    DSKPLASM AD545SIN

This generates a binary object file called AD545SIN.OBJ, which is loaded into the DSK+.

```
        .title "Sine-wave generator for AD545-EVM and C54x DSK+"
        .width  80
        .length 55
; Adapted from DSK+ example programs by Ziad Asghar
;                                       September 1999
        .mmregs
```

```
        .setsect ".text",0x1800,0     ; these assembler directives specify
        .setsect ".data",0x0200,1     ; the absolute addresses of different
        .setsect "vectors",0x0180,0   ; sections of the assembly code

makesine        .set 1   ; Set it to one to generate a sine wave and to check
                         ; the working of the speaker, and set it to 0 for the
                         ; DSP to send back the digital data that it receives
                         ; from the codec
sinestepsize    .set 1
sinetablesize   .set 8 ; for 1kHz at 8 ksps


; The vectors in this table can be configured for processing external and
; internal software interrupts. The DSKplus debugger uses four interrupt
; vectors. These are RESET, TRAP2, INT2, and HPIINT.
;   *  DO NOT MODIFY THESE FOUR VECTORS IF YOU PLAN TO USE THE DEBUGGER  *
;
; All other vector locations are free to use. When programming always be sure
; the HPIINT bit is unmasked (IMR=200h) to allow the communications kernel and
; host PC interact. INT2 should normally be masked (IMR(bit 2) = 0) so that
; the DSP will not interrupt itself during a HINT. HINT is tied to INT2
; externally.

        .sect "vectors"
reset   goto  #80h             ;00; RESET  * DO NOT MODIFY IF USING DEBUGGER *
        nop
        nop
nmi     return_enable          ;04; non-maskable external interrupt
        nop
        nop
        nop
trap2   goto  #88h             ;08; trap2  * DO NOT MODIFY IF USING DEBUGGER *
        nop
        nop
        .space 52*16           ;0C-3F: vectors for software interrupts 18-30
int0    return_enable          ;40; external interrupt int0
        nop
        nop
        nop
int1    return_enable          ;44; external interrupt int1
        nop
        nop
        nop
int2    return_enable          ;48; external interrupt int2
        nop
        nop
        nop
tint    return_enable          ;4C; internal timer interrupt
        nop
        nop
        nop
brint   return_enable          ;50; BSP receive interrupt
        nop
        nop
        nop
```

```
bxint   return_enable          ;54; BSP transmit interrupt
        nop
        nop
        nop
trint   dgoto receive          ;58; TDM receive interrupt
        nop
        nop
txint   return_enable          ;5C; TDM transmit interrupt
        nop
        nop
        nop
int3    return_enable          ;60; external interrupt int3
        nop
        nop
        nop

hpiint  goto  #0e4h            ;64; HPIint * DO NOT MODIFY IF USING DEBUGGER *
        nop
        nop
        .space  24*16      ;68-7F; reserved area
        .data
sineindex   .word   0      ; index to sine-wave table
sinevalue   .word   0      ; workspace for sine-wave generation
initwork    .word   0      ; workspace for initialization
        .text
start:  intm = 1           ; disable all interrupts
        pmst = #01a0h      ; Interrupt pointer maps vectors to address 180h
        sp = #0ffah        ; stack pointer located in Communications Kernel
        imr = #240h        ; unmask TDM RINT and HPIINT(host port interface)
        OVM = 0            ; OVM = 0 (do not clip overflow)
        ASM = #0           ; ASM = 0 (shift=0)
        DP = #0
INIT:

; initialize serial port
        tcr = #10h         ; stop timer
        imr = #240h        ; unmask RXINT and HPIINT
        tspc = #0008h      ; stop TDM serial port
        tdxr = #0h         ; send 0 as first xmit word
        tspc = #00c8h      ; reset and start TDM serial port

; Initialize ad545 registers
; Include the next four lines in the code when "makesine" is set to 1. For
; "makesine" set to 0 the codec uses the default register values.
        a = #0000000100011011b    ; register 1
        call ad545init            ; Analog loopback asserted, Data-In PGA
                                  ; selected for monitor amp input and
                                  ; Monitor amp PGA gain set to 6 dB
        a = #0000001000000010b    ; register 2
        call ad545init            ; 8 ohm speaker driver gain set to 0 dB
            intm = 0              ; enable all interrupts

WAIT        idle(1)              ; idle waiting for interrupts
```

```
            nop
            goto   WAIT
    ;--------------------------------------------------------------------------
    ; ad545 init routines here
    ad545init
            ifr = #080h                 ; clear flag from IFR
        tdxr = #01h                     ; request secondary when AD545 starts
            call waitfortdx             ; wait for primary to xmit
            tdxr = a                    ; send register value to serial port
            ifr = #080h                 ; clear flag from IFR
            call waitfortdx             ; wait for secondary to xmit
            tdxr = #0h                  ; send neutral state in case last init
            ifr = #080h                 ; clear flag from IFR
            call waitfortdx             ; wait for neutral state to xmit
            return                      ; return from subroutine
    waitfortdx                          ; a robust way of waiting for a tdm port
            b = mmr(ifr)                ; transmission to complete
            b &= #10000000b
            nop
            nop
            if(BEQ) goto waitfortdx
            return
    ;--------------------------------------------------------------------------
    receive
                                 ; save context if necessary

            B = mmr(TRCV)    ; always read serial port to avoid buffer overflow
                                 ; which would stop interrupts from being generated
        B &= #1111111111111110b
        .if makesine = 0   ; don't make a sinewave - just echo data from adc
                                 ; to dac
                                 ; put code for filtering etc here
        .else              ; make a sinewave
            AR1 = #sineindex
            AR2 = #sinevalue
            A  = *AR1
            A += #sinestepsize
            B  = A
            A -= #sinetablesize
            nop                         ; two nops to allow for pipeline delay
            nop
            if (ALT) execute(1)     ; check whether index points outside table
            A = B

            *AR1 = A

        A += #sinetable8_3dB
            *AR2 = prog(A)              ; get sinewave value from table in program
                                        ; memory
            B = *AR2                    ; (could use sine table in rom for this)
            .endif
            mmr(TDXR) = B

                                        ; restore context if necessary
```

```
     return_enable                      ; return to waiting loop
;-------------------------------------------------------------------------
transmit:                              ; Transmit and receive interrupts are
                                       ; inherently synchronized, so there is no
                                       ; point in using both return_enable
;-------------------------------------------------------------------------
sinetable8_3dB                         ; -3dB re clipping, 1kHz @ 8 ksps
                                       ;  8 samples/cycle
 .word 0, 16384, 23170, 16384, 0, -16384, -23170, -16384
 .end
```

4 References

1. *TLC320AD545C/I Data Manual, Single Channel Data/Fax Codec*. literature number SLAS206A.
2. *TMS320C54x, TMS320LC54x, TMS320VC54x Fixed-Point Digital Signal Processors*, literature number SPRS039B.
3. *Evaluation Board for the TLC320AD50C DSP Analog Interface Circuit*, literature number SLAAE15.

Appendix A

A.1 Installing the AD545EVM

Table A–1 shows the functions of the switches.

Table A–1. Switch Positions

SWITCH	POSITION 1	POSITION 2
SW1	*fslow* (See AD545 data sheet)	*fshigh* (See AD545 data sheet)
SW2	*Input*. Input of the AD545 (DTRXM and DTRXP) connected to the 3.5-mm stereo jack labeled INPUT.	*TXFM*. Input of the AD545 (DTRXM and DTRXP) connected to the transformer interface via the hybrid operational amplifiers.
SW3		
SW4	*Output*. Output of the AD545 (DT_BUFP and DT_BUFM) connected to the 3.5-mm stereo jack labeled OUTPUT.	*TXFM*. Output of the AD545 (DT_BUFP and DT_BUFM) connected to the transformer interface via the hybrid operational amplifiers.
SW5		

Table A–2 shows the functions of the jumpers.

Table A–2. Jumper Positions

JUMPER	OPEN	CLOSED
CLOCK A	Clock on the AD545EVM and CLKIN on the DSP not connected	Clock on the AD545EVM and CLKIN on the DSP connected
CLOCK B	AD545 not running on 4.096-MHz oscillator on AD545EVM	AD545 running on the 4.096 MHz oscillator on AD545EVM
CLOCK C	AD545 not running on CLKOUT on the DSP	AD545 running on CLKOUT from DSP

NOTE: Certain issues arise when trying to run the AD545 using DSPs CLOCKOUT because the maximum acceptable MCLK might be exceeded. CLKMD pins on the DSP configure the C542s hardware PLL to divide CLKIN by two, as discussed in the *System Clock* section. Problems with the HPI interface can occur. In stand-alone mode, this jumper can be used to run the AD545 on an off-board clock. Jumpers CLOCK B and CLOCK C must not be closed at the same time.

The connectors labeled SERIAL and ANALOG interface the AD545EVM to systems other than the DSK+. The pinouts are shown in Table A–3.

Table A–3. ANALOG and SERIAL Connectors

PIN	ANALOG	SERIAL
1	DTRX_FB	DT_MCLK
2	DTRXM	DGRND
3	DTRXP	DT_SCLK
4	DT_REF	DGRND
5	DTTX_OUTP	DT_FS
6	DTTX_INM	DGRND
7	DTTX_INP	DT_DOUT
8	DTTX_OUTM	DGRND
9	DT_BUFP	DT_DIN
10	DT_BUFM	DGRND
11	TXFM_M	
12	TXFM_P	

A.2 Parts List

The parts list is shown in Table A–4 below.

Table A–4. Parts List

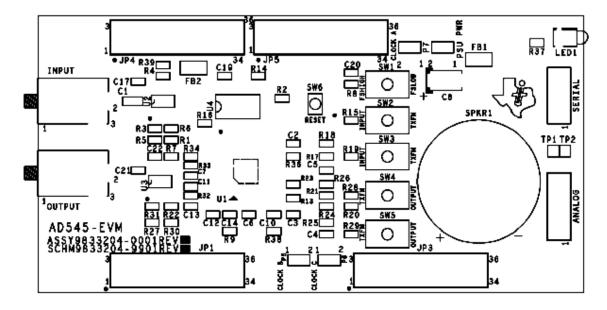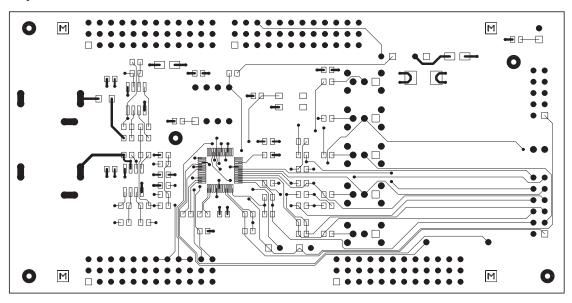| SILK NAME	COMPONENT	SILK NAME	COMPONENT
U1	TLC320AD545PT	R36	0 Ω
LED1	Dialight 551-0207 Green LED	R37	560 Ω
U2	TLC2272ACD	R38	15 kΩ
U3	TLC2272ACD	R39	10 kΩ
U4	Fox JITO-2-BC5AE 4.096	C1	0.47 μF 16 V Panasonic ECW-U1C474JB9
R1	4.99 kΩ (all resistors 1 %)	C3	470 pF COG/NPO 0603
R2	10 kΩ	C4	470 pF COG/NPO 0603
R3	10 kΩ	C5	470 pF COG/NPO 0603
R4	10 kΩ	C8	100 μF 10 V size D tantalum
R5	10 kΩ	C10	470 pF COG/NPO 0603
R6	4.99 kΩ	C11	0.1 μF X7R 0805
R7	13 kΩ	C12	0.1 μF X7R 0805
R8	10 kΩ	C13	2.2 nF COG/NPO 0805
R13	15 kΩ	C14	0.1 μF X7R 0805
R14	47 Ω	C17	0.1 μF X7R 0805
R15	15 kΩ	C19	0.1 μF X7R 0805
R16	2.21 kΩ	C20	0.1 μF X7R 0805
R17	10 kΩ	C21	0.1 μF X7R 0805
R18	20 kΩ	C22	220 pF COG/NPO 0603
R19	15 kΩ	FB1	100 mH FBEAD
R20	10 kΩ	FB2	100 mH FBEAD
R21	20 kΩ	Input	Vimex SCJ-0352B stereo jack socket
R22	4.99 kΩ	Output	Vimex SCJ-0352B stereo jack socket
R23	280 Ω	Clock A	Right-angle header
R24	280 Ω	Clock B	Right-angle header
R25	20 kΩ	Clock C	Right-angle header
R26	20 kΩ	SW1	C&K GS01MV3KE slide switch
R27	10 kΩ	SW2	C&K GS01MV3KE slide switch
R28	23.2 kΩ	SW3	C&K GS01MV3KE slide switch
R29	23.2 kΩ	SW4	C&K GS01MV3KE slide switch
R30	10 kΩ	SW5	C&K GS01MV3KE slide switch
R32	26.1 kΩ	SW6	Digi-Key 7914G-000ETR-ND push-button switch
R33	10 kΩ	Spkr	International S110RMSS
R34	26.1 kΩ		

A.3 Circuit Diagrams

A.4 PCB Diagrams

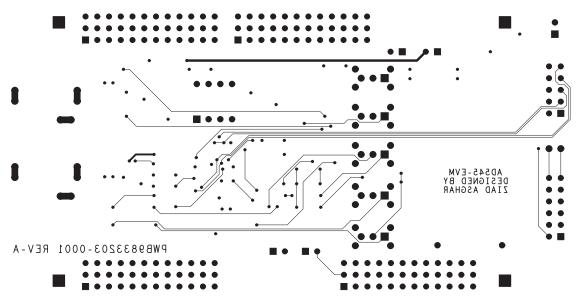### A.4.1 Top Side Silkscreen

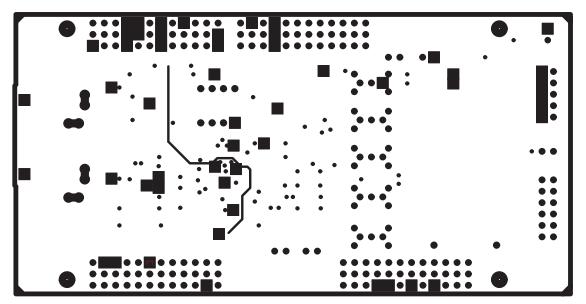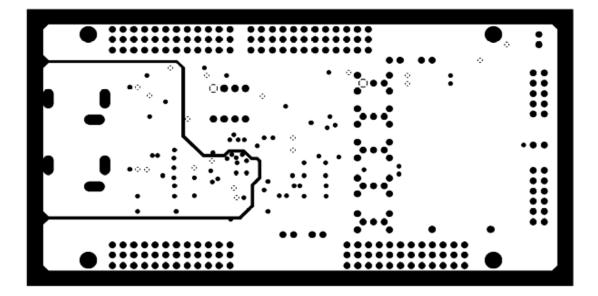### A.4.2 Top Side Tracks

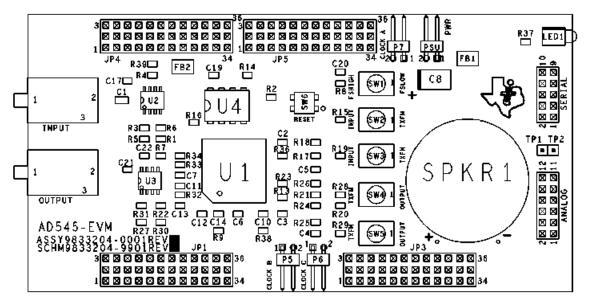### A.4.3 Bottom SIde Tracks

A.4.4 Ground Plane

A.4.5 Power Plane

A.4.6 Component Positions

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