# TLC320AD58C

## Sigma-Delta Stereo Analog-to-Digital Converter

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## Introduction

The TLC320AD58C is a sigma-delta stereo analog-to-digital converter (ADC) that provides 18-bit resolution with a signal-to-noise ratio (EIAJ) of 100 dB and a dynamic range of 95 dB. The device consists of two synchronous conversion paths including a digital decimation filter following the 64× oversampling sigma-delta modulator.

The TLC320AD58C device is available in a 28-pin DWM surface-mount package. This device uses the One Micron Advanced LinEPIC1Z™ Process. The functional block diagram for the TLC320AD58C is shown in Figure 1.

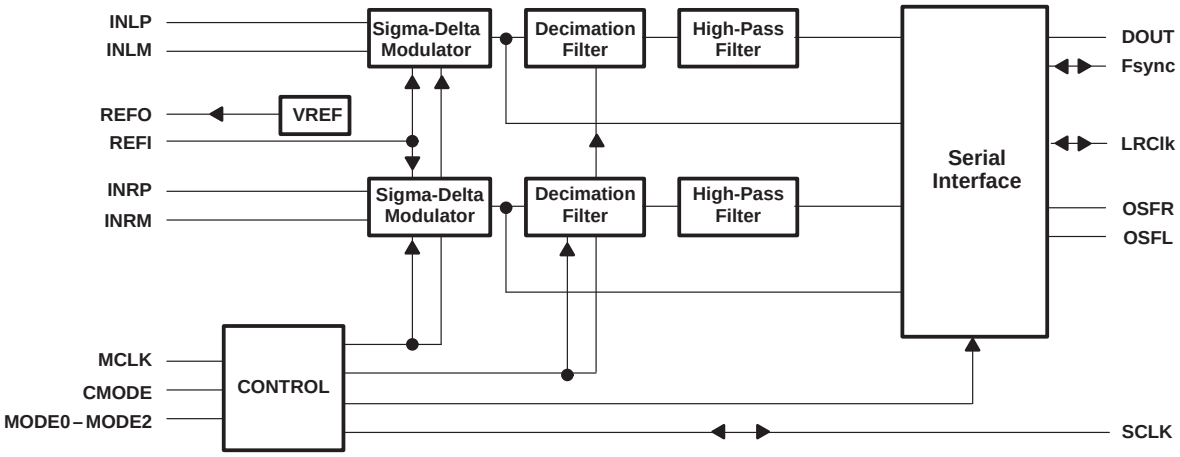


**Figure 1. TLC320AD58C Functional Block Diagram**

## Differential Input

The TLC320AD58C has a differential input scheme in order to provide common-mode noise rejection and to increase the dynamic range of the inputs. Figure 2 shows the analog input signals used in a differential configuration to achieve a differential swing of 6.4 V with a swing on each input line of 3.2 V.

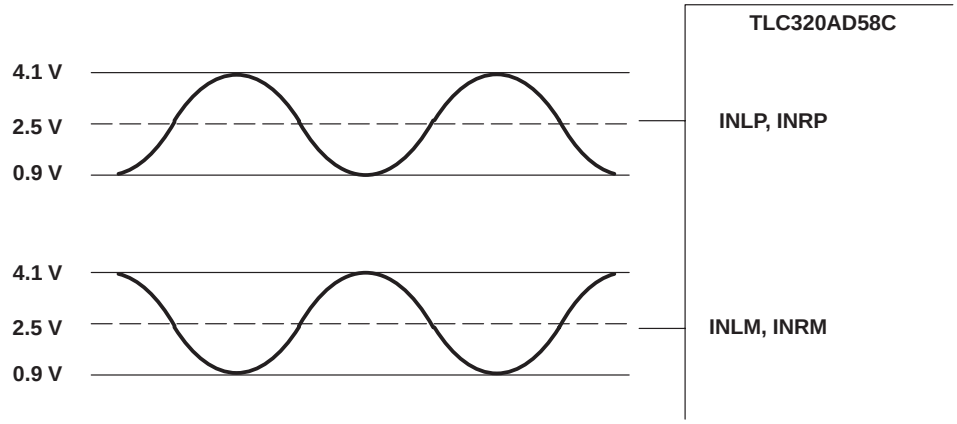


**Figure 2. Differential Analog-Input Configuration**

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The TLC320AD58C is a stereo ADC which means that it has separate channels for left and right data. The separate channels apply from the input, through the modulator and filtering, and to separate digital outputs. The signal applied to the inputs [INL(R)P and INL(R)M] must be differential to preserve the device specifications. When the analog input is single-ended, which is often the case, it must first pass through a single-ended-to-differential converter. The Texas Instruments TL32088 analog front end IC is recommended for this purpose. The TL32088 was designed to be a companion to the TLC320AD58C.

Regardless of whether the input must be converted to differential, it must first pass through an antialiasing filter. Aliasing occurs when a high-frequency signal is translated to a lower frequency by sampling a signal at less than twice its maximum frequency. Those frequencies that are greater than half the sampling rate are translated down to lower frequencies by the sampling process and appear as frequencies in the signal band.

Sampling a frequency causes a copy of the input spectrum to appear at multiples of the sampling frequency. When the copy overlays the original input spectrum at half the sampling frequency, then the amplitude component of the band that overlaps is added to the noise floor degrading the performance. The solution to this problem is to filter out all of the frequencies that are greater than half the sampling frequency. An effective way to do this is with a brick-wall filter, but this is expensive and difficult to design.

Fortunately, due to the 64× oversampling of the TLC320AD58C, the sampling frequency divided by two is sufficiently far enough away from the signal band. Only a single-pole resistor-capacitor (RC) low-pass filter is required to achieve the necessary attenuation of the unwanted frequencies. The suggested starting value for the pole is 318 kHz. This value can be adjusted to optimize performance.

When possible, care should be taken to ensure that the input signal applied to the ADC is within the dynamic range. When the dynamic range is exceeded, data out (DOUT) outputs the digital code for the appropriate extreme until the input amplitude returns within the dynamic range. After two consecutive conversions exceeding full scale, the overscale flag (OSFL/R) for the left or right channel is set high for 4096 LRClk cycles. Each overscale flag can trigger an LED to serve as an indicator that the dynamic range has been exceeded. When an LED is used, the current should be limited by a 2-kΩ resistor in series with the LED.

## Serial Port Interface

Data shifts out on DOUT serially in a 2s-complement data word. The left and right channel inputs are sampled and converted simultaneously, but the channel outputs are sent out in two separate time packets through the serial port. The serial port interface has five master modes and three slave modes each with different readout formats. The mode is selected by setting the MODE0-2 bits (terminals 8, 13, and 22). As a slave, the TLC320AD58C receives LRClk, Fsync, and SCLK as inputs. The conversion cycle for slave mode is synchronized to the rising edge of LRClk, and the data is synchronized to the falling edge of SCLK. SCLK must meet the setup requirements specified in the recommended operating conditions in the TLC320AD58C data manual. Synchronization of the slave modes is accomplished by pulling the $\overline{\text{DigPD}}$ signal (terminal 10) low after toggling it high.

In master mode, the TLC320AD58C generates LRClk, Fsync, and SCLK from MCLK. These signals are provided for synchronizing the serial port of a digital signal processor (DSP) or other electronics to valid data. Fsync designates the valid data from the ADC in master mode. LRClk is generated internally from MCLK. The frequency of this signal is fixed at the sampling frequency $F_S$. During the high period of LRClk, the left channel data shifts to the output. The right channel data is shifted out serially during the low period of LRClk. The conversion cycle is also synchronized to the rising edge of LRClk for master mode. The eight modes are discussed in the following paragraphs. Refer to Figure 3(a) through Figure 3(h) for the timing diagrams.

**Mode 000:** The device is in slave mode with the MSB of the data sent out first. The data can be sent out as either 16 bits or 18 bits. The standard output format is 16 bits, but for higher resolution, an 18-bit output can be used in a 16-bit system with an external dithering filter scheme to reduce the word width to 16 bits. The number of bits of resolution is determined by the number of SCLK cycles provided while LRClk is high (or low). In this mode, Fsync (terminal 17) is tied high.

**Mode 001:** The device is in slave mode with the data shifted out LSB first. This mode is for 18-bit data only and requires 64 SCLK periods for every LRClk period. In this mode, Fsync is tied high.

**Mode 010:** The device is in slave mode with the data shifted out MSB first. The data can be shifted out of the serial port as either 16 bits or 18 bits. This mode requires 64 SCLK periods for every LRClk period.

**Mode 011:** The device is in master mode with the data shifted out MSB first. This mode is for 16-bit data only. The rising edge of Fsync designates the beginning of a valid data transfer and remains high throughout the transfer of all 16 bits of valid data. Fsync then goes low. In this way, Fsync provides boundaries for the valid data. There is a delay of one SCLK cycle after LRClk goes high before the rising edge of Fsync occurs. In this mode, there must be 64 SCLK cycles for every LRClk cycle.

**Mode 100:** The device is in master mode with the data shifted out MSB first. This mode is for 18-bit data only. Fsync also designates the valid data in this mode, but it is designated by a single pulse prior to the valid data. The falling edge of this pulse designates the beginning of valid data. In this mode, there must be 64 SCLK cycles for every LRClk cycle.

**Mode 101:** This mode is identical to mode 100 except that the data is shifted out LSB first. This mode is an 18-bit only master mode.

**Mode 110:** (DSP Continuous Mode) The device is in master mode with the data shifted out MSB first. This mode is for 16-bit data only. Fsync designates the valid data from the converter. In this mode, there must be 32 SCLK cycles for every LRClk cycle (half of the SCLK frequency used in the other modes).

**Mode 111:** (DSP Continuous Mode) This mode is identical to mode 110 except that the data is shifted out LSB first. This mode is a 16-bit master mode.

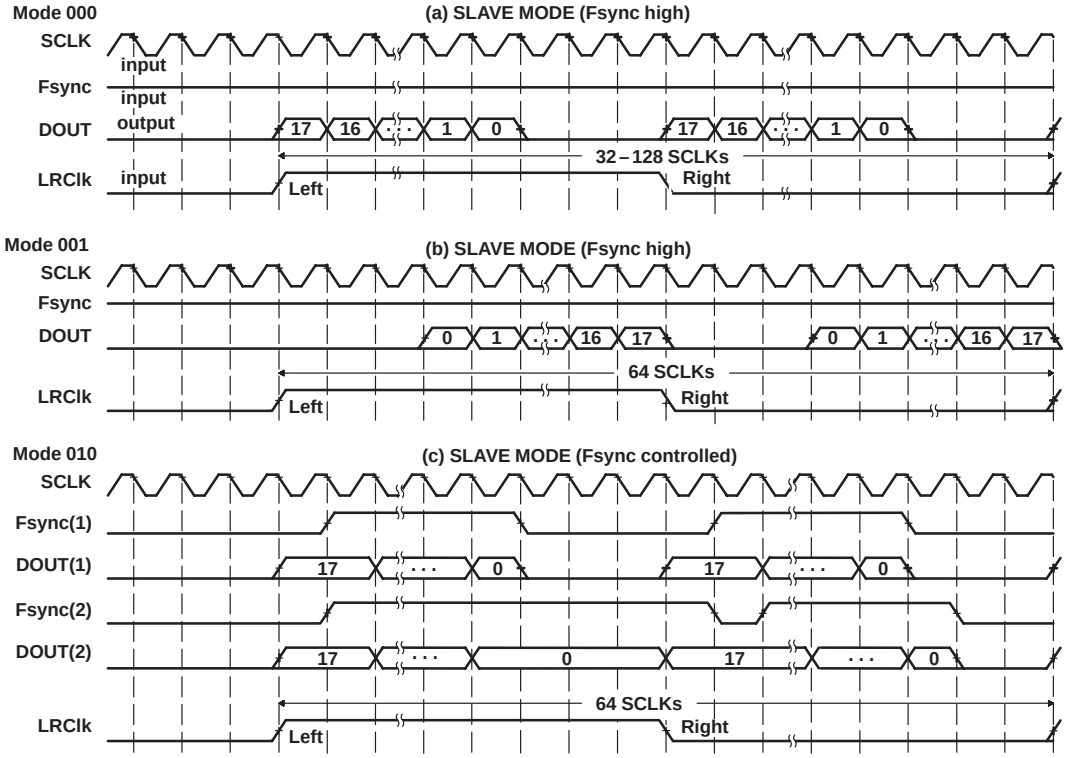


**Figure 3. Serial Port Timing Diagrams**

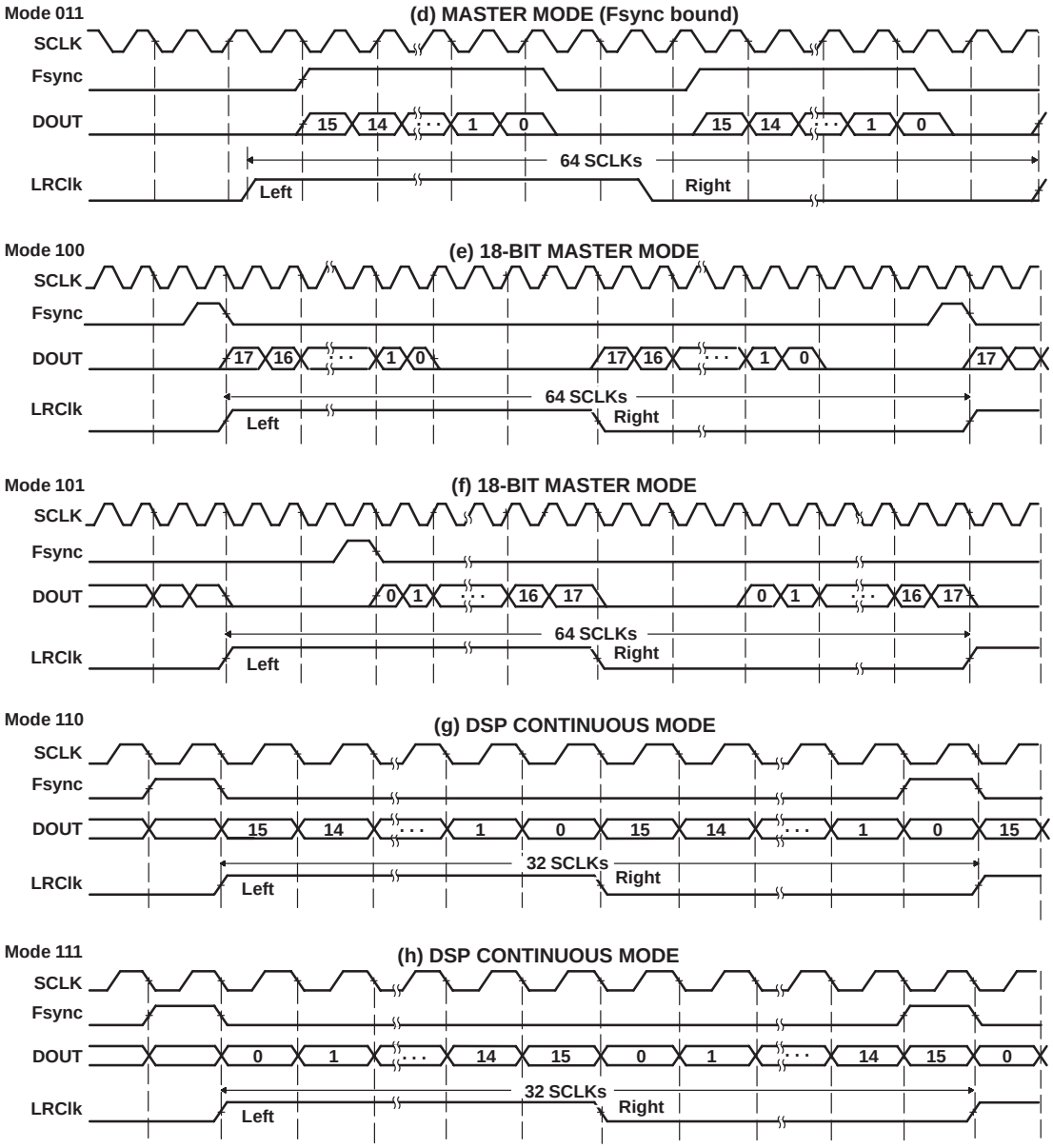


**Figure 3. Serial Port Timing Diagrams (Continued)**

## Master Clock Circuit

The clock circuit generates and distributes necessary clocks throughout the design. MCLK is the external master clock input whether the device is being used in master or slave mode. CMODE (terminal 12) selects the ratio of MCLK to the sample rate LRClk. When CMODE is low, the sample rate of the data paths is set as LRClk = MCLK/256. When CMODE is high, the sample rate of the data paths is set as LRClk = MCLK/384. The state of this bit does not affect the oversampling ratio which is always set at 64×. When in master mode, SCLK is derived from MCLK to provide the clocking of the serial communications between the sigma-delta-audio ADC and a DSP or control logic. In all modes except modes 110 and 111, this is equivalent to a clock running at 64× LRClk. In modes 110 and 111, this is equivalent to a clock running at 32× LRClk. When the device is in slave mode, SCLK is an external input along with LRClk and Fsync.

## Power Down

The power-down state is comprised of separate analog and digital power-down modes. The digital power-down mode shuts down the digital filters and clock generation (for master mode). All digital outputs are set to an unasserted state. When the digital power-down terminal ($\overline{\text{DigPD}}$) is pulled low, normal operation of the device is initiated. In slave mode, the conversion process must be synchronized to an input on the LRClk terminal as well as the SCLK terminal. Therefore, the conversion process is not initiated until the first rising edge of SCLK and the first rising edge of LRClk are detected after $\overline{\text{DigPD}}$ is pulled low. This synchronizes the conversion cycle. All conversions are performed at a fixed LRClk rate after the initial synchronization. After the digital power-down terminal ($\overline{\text{DigPD}}$) is brought low, the output of the digital filters remains invalid for 50 LRClk cycles. In master mode, LRClk is an output. The conversion process is initiated based on internal timing.

The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid, which renders the outputs of the digital filters invalid. When the analog power-down terminal ($\overline{\text{AnaPD}}$) is brought low, the modulators are brought back online, and the outputs of the digital filters require 50 LRClk cycles for valid results. The power-down state typically drops the current to 0.5% of operating current in the analog power-down mode and to 0.2% of operating current in the digital power-down mode.

The conversion process is not initiated until the first rising edge of SCLK and the first rising edge of LRClk are detected after $\overline{\text{DigPD}}$ is pulled low. This synchronizes the conversion cycle. All conversions are performed at a fixed LRClk rate after the initial synchronization. In this way, the $\overline{\text{DigPD}}$ terminal can perform the reset function.

## Test Mode

When the TEST terminal (terminal 11) is pulled high, a test mode is selected that routes the high-speed one-bit modulator result to the serial port output. When in test mode, the SCLK output frequency is equal to the data out frequency and LRClk is an input. When LRClk is held high, the left channel modulator output is routed to the serial port output. When LRClk is held low, the right channel modulator output is routed to the serial port output. This feature can be incorporated into a built-in self test. This feature also allows the output of either modulator to be sent to an external decimator filter that allows a different sample rate or a different digital decimation-filter transfer function. In this mode, however, only one channel of data (left or right) can be sent to the serial port output. For normal operation the TEST terminal should always be held low.

## High-Pass Filter

The TLC320AD58C has a separate high-pass filter in the conversion path for each channel. The purpose of the high-pass filter is to remove dc from the input. The cutoff frequency for the high-pass filter is approximately 2 Hz.

## Power Supply Decoupling

One source of high frequencies that can interfere with the operation of the TLC320AD58C is the power supplies. Oversampling sigma-delta converters are clocked at very high frequencies. This high-frequency clocking produces high-frequency current spikes and glitches on the power supply lines. If not attenuated, these power supply disturbances degrade the converter's performance. When a high frequency near the input sample rate is injected into the power supplies, it increases the noise floor and, therefore, decreases the effective resolution of the ADC. The injected noise is not a pure sine wave; harmonics are present. Thus, the shape of the resulting interference is not a tone but a collection of tones. These undesirable tones show up directly in the audio output. The analog and digital power supplies ($AV_{DD}$ and $DV_{DD}$) used by the device should be carefully bypassed to the correct ground plane. A suitable solution for high-quality audio is to use a 47-µF aluminum electrolytic capacitor (Nichicon Muse part number UFX1A470MDJ) in parallel with a 0.1-µF metal film capacitor (Wima MKS2 series) for filtering higher frequency components. As with all converters, lower cost filtering components can be used but with some sacrifice in performance. The most important parameter to consider in choosing a capacitor is its equivalent series resistance (ESR). For the best performance, it is important to use the lowest ESR part that meets the design's cost and size requirements.

The power-supply bypass capacitors must be placed as close as possible to the converter's power supply terminals (terminals 4 and 18). There are two important reasons for positioning the bypass capacitors as close as possible to the

power supply terminals. First of all, a converter's power-supply rejection-ratio (PSRR) decreases at higher clock frequencies. For all integrated circuits, the power supply inputs should always be viewed as signal inputs. The internal circuit treats any ac signal appearing on the power supply voltage as another input signal. However, not all ac signal frequencies are acted upon in the same manner. All ICs have an inherent PSRR that indicates the ability of the device to attenuate ac signals. Thus, high frequency noise present on the power supply terminals due to the clocks used for oversampling and conversion is not well rejected by the converter alone. The bypass capacitors also supply the high frequency component of supply current used by the converter.

The second important reason for positioning the bypass capacitors as close as possible to the supply terminals is that the inductance of the bypass-capacitor leads at high clocking frequencies reduces their bypassing efficiency. Therefore, the leads must be as short as possible. Bond wires, package leads, board traces, and capacitor leads can total up to an inductance of approximately 10 to 20 nH and an impedance on the order of 3 to 5 Ω. This may not seem significant; however, the device is converting signals at the level of 20 to 80 mV per bit.

As the distance from the capacitor to the converter's power-supply terminal increases, the attenuation efficiency of the bypass capacitor decreases. For this reason, the use of sockets and other mounting schemes that lift the part off the board can degrade noise reduction performance.

## Voltage Reference

The voltage reference input is often the most sensitive analog terminal on an ADC. The voltage reference has a multiplicative relationship to the output. Ideally, the voltage reference is a pure dc signal, but in practice, the voltage reference has an ac component. All ac components on the voltage reference are multiplied by the input signal yielding sum and difference frequency components in the output due to the modulation inherent in sigma-delta converters. This results in an elevation of the noise floor when not adequately decoupled. The TLC320AD58C generates an internal voltage reference, REFO (terminal 26). This is normally connected to the voltage reference input, REFI (terminal 3). The option does exist to input a separate voltage reference at terminal 3. When an external reference is used, the absolute accuracy as well as stability over time and temperature should be checked. This reference should be at 3.2 V. Whether the internal reference or an external reference is used, bypass capacitors should be connected between the reference input terminal and analog ground. Suitable choices for the bypass capacitors are a 220-μF aluminum electrolytic capacitor (Nichicon Muse part number UFX1A221MEJ) in parallel with a 0.1-μF metal film capacitor (Wima MKS2 series). It is critical to position these capacitors as close to the terminal as possible. The smaller value capacitor should be placed closer to the chip. It is also important in designing the circuit to keep all dynamic signals, both analog and digital, away from this terminal.

## Other Design Considerations

The most fundamental rule in audio design is to use separate analog and digital ground planes. All analog components and associated circuits should be placed directly over the analog ground plane while the digital components and clock traces should be restricted to the digital ground plane. When the digital traces are run over the analog ground plane, capacitive coupling of the fast edges of the high-speed logic signals can occur. Ground planes provide a convenient way to distribute a low-impedance low-inductance ground reference over a wide area, but they are not incorruptible. A similar argument applies to analog traces over the digital ground plane. It takes only a small amount of coupling to transfer tens of millivolts of a signal from the digital ground plane onto the sensitive analog traces. One of the worst conditions is to overlap the analog and digital ground planes because the intersecting area could be large and thus create significant capacitance. The converter should be placed across the gap between the planes since it connects to both analog and digital grounds. Normally, ground planes are not used; all of the ground connections are returned to one single star-ground point at the power supply, voltage regulator, or power connector. In the same way, there should be only one connection between the analog and digital ground planes at the star point in order to avoid ground loops.

Power planes can be used; however, they are not always necessary. It is often good design practice to provide separate power supply traces from the regulator or power supply to each of the critical analog components rather than daisy chain the supply. When there are any ripple or high-frequency glitches from transient currents, power planes can easily couple these into the analog traces. When they are used, the analog supply plane should be placed entirely under the analog ground plane. Power planes can add crosstalk and interaction within the analog section. The power plane forms a common capacitor plate between any two analog traces. While this coupling also occurs on the ground planes, the ground plane is a much lower impedance than the power plane.

Trace lengths connecting the analog inputs from the edge connectors should be as short and direct as possible. Longer etch runs have a higher impedance which increases their susceptibility to noise. Input amplifiers can be rotated in 90-degree increments to the best orientation to keep the etch runs short. High-impedance lengths, such as summing junctions of operational amplifiers, should be as short as possible.

Only metal film resistors should be used in the analog signal path. Carbon resistors can add noise and distortion from voltage coefficient effects. Only polystyrene, dipped mica, or NPO ceramic capacitors should be used in the analog signal path as well. Capacitors made with Z5U or X7R materials can have a high degree of dielectric absorption which causes nonlinearity and distortion.

## Schematics

Schematics for the TLC320AD58C are shown in Figure 4, Figure 5, and Figure 6.

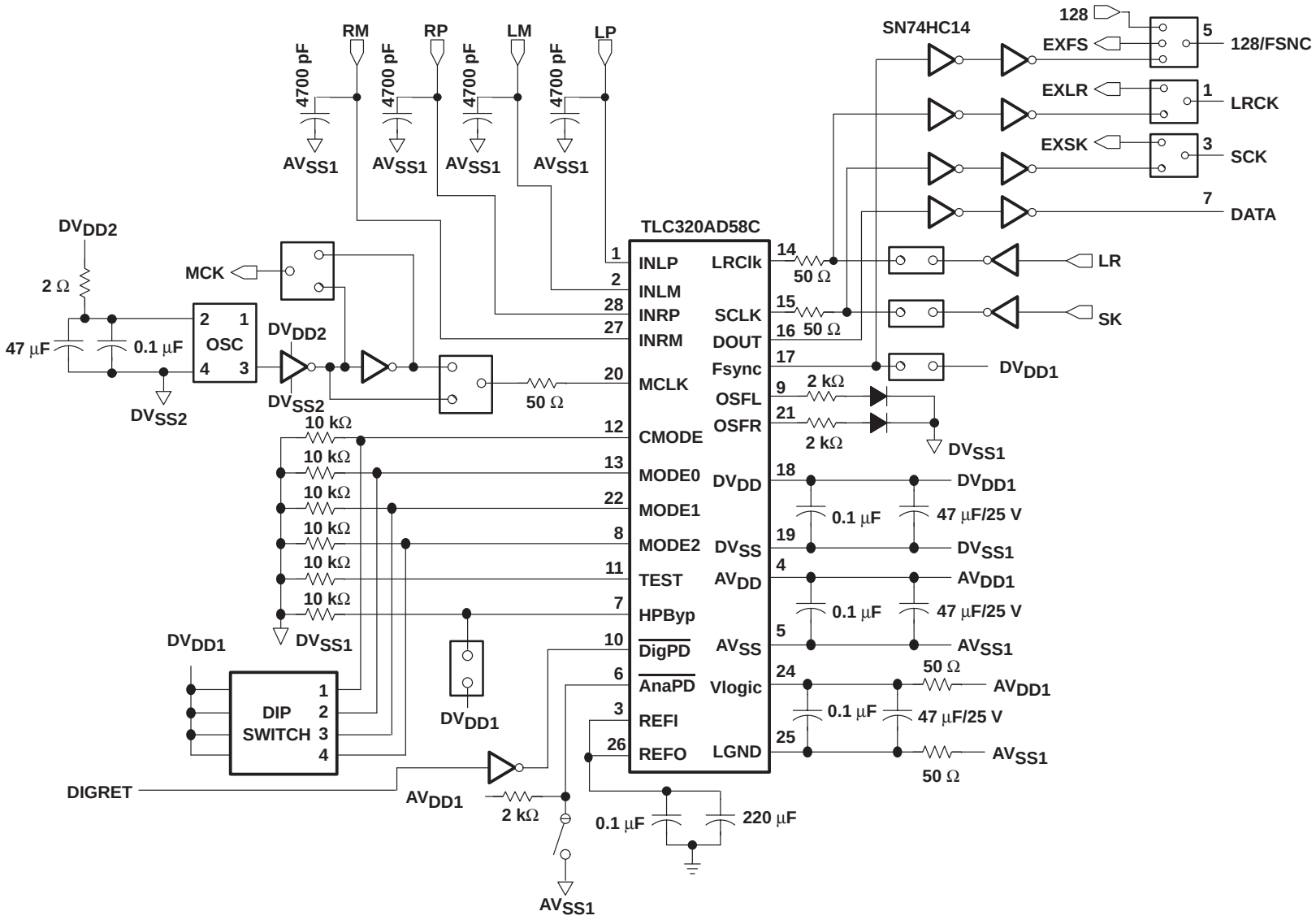


**Figure 4. TLC320AD58C Configuration Schematic**

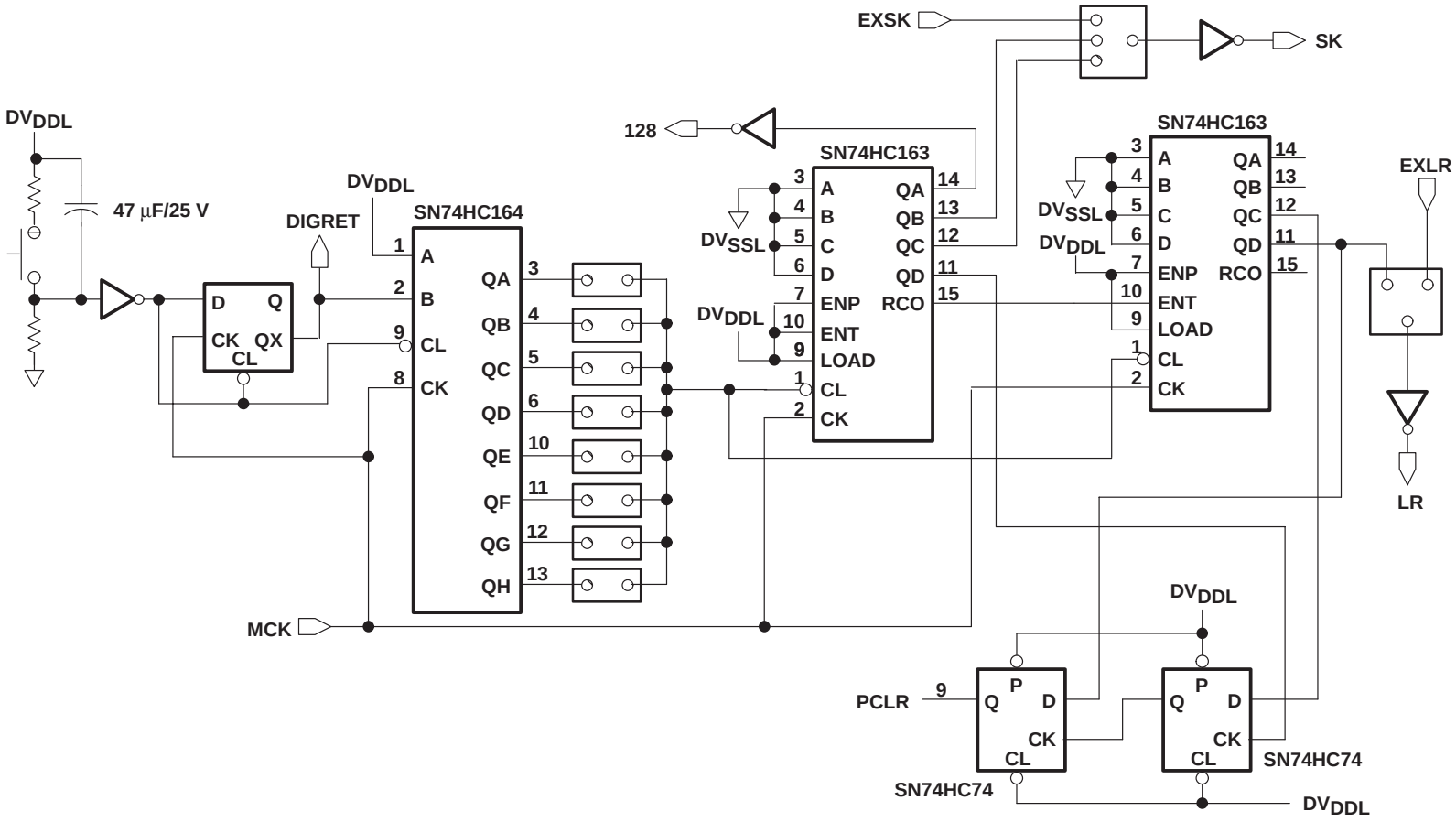


**Figure 5. TLC320AD58C External Digital-Timing and Control-Signal Generation Schematic**

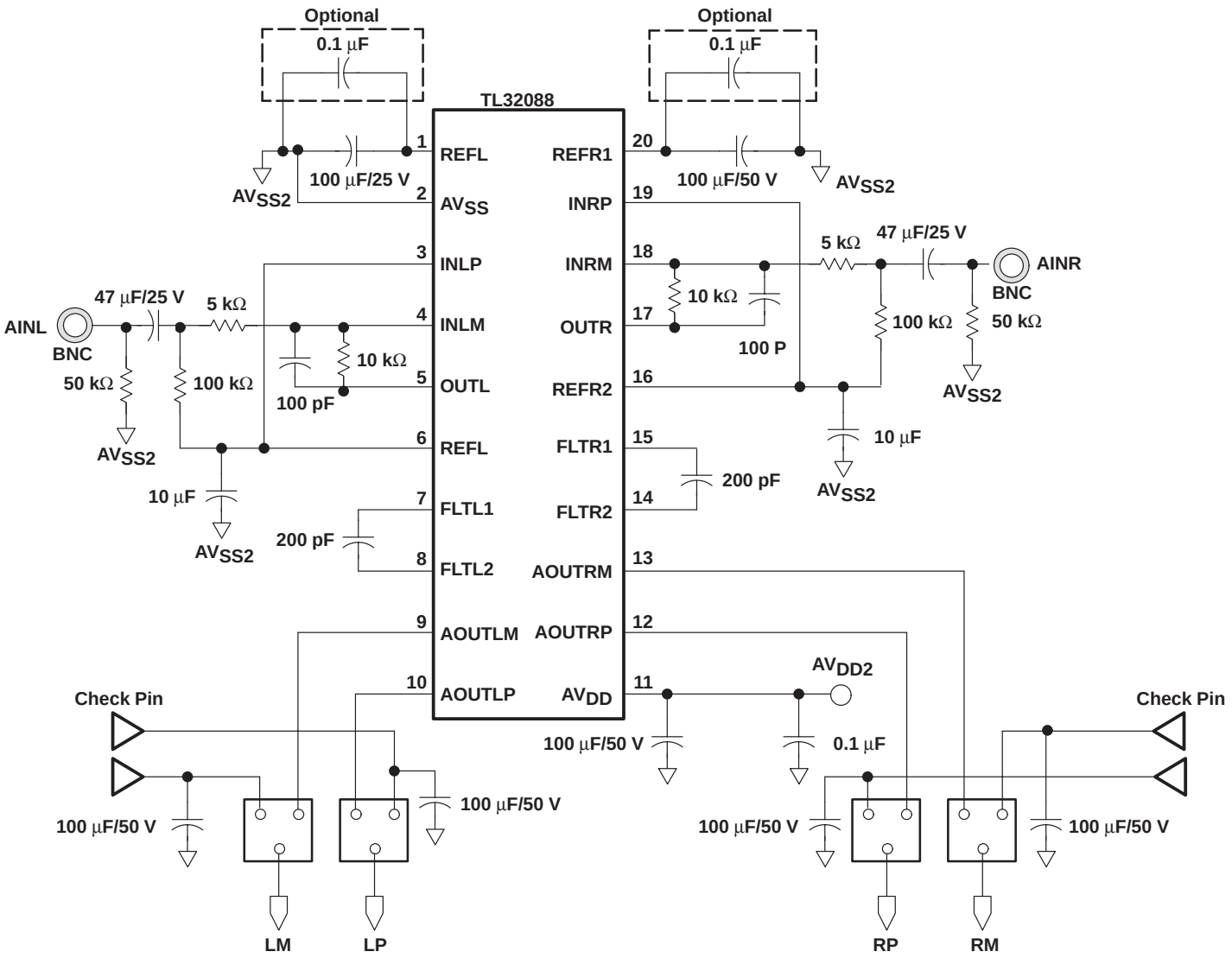


**Figure 6. TLC320AD58C External Analog Input Buffer Schematic**

## Characteristic Curves

The characteristic curves for the TLC320AD58C are shown in Figure 7, Figure 8, and Figure 9.

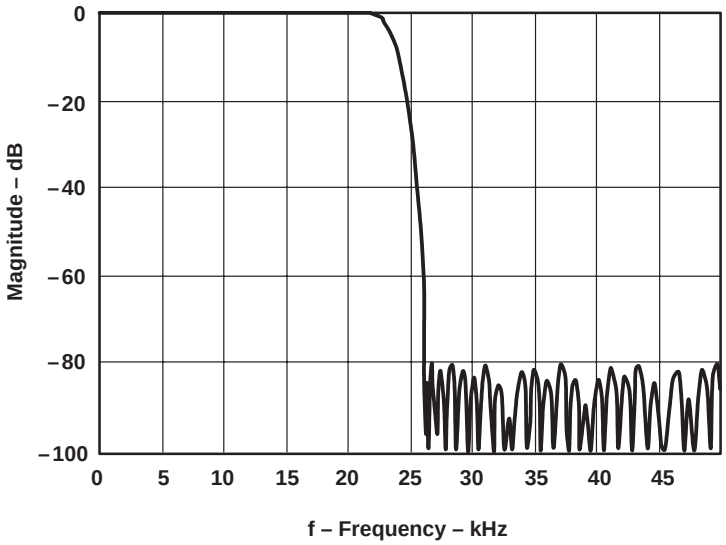


**Figure 7. TLC320AD58C Decimation Filter Response**

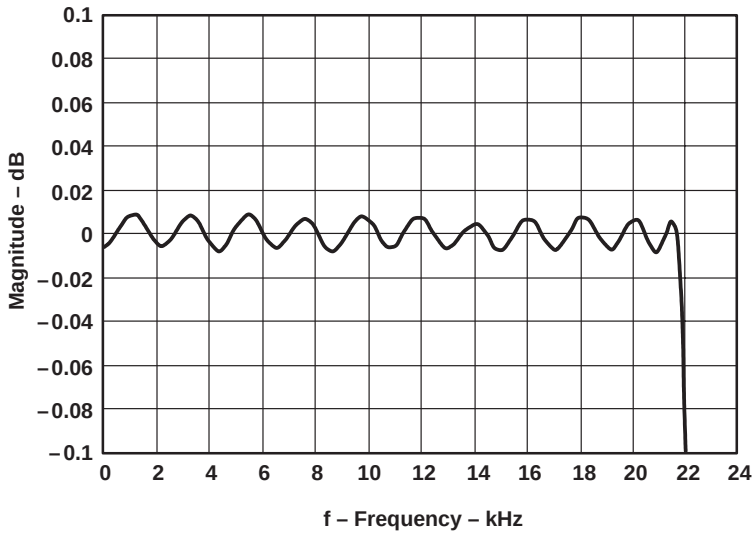


**Figure 8. TLC320AD58C Decimation Filter Ripple**

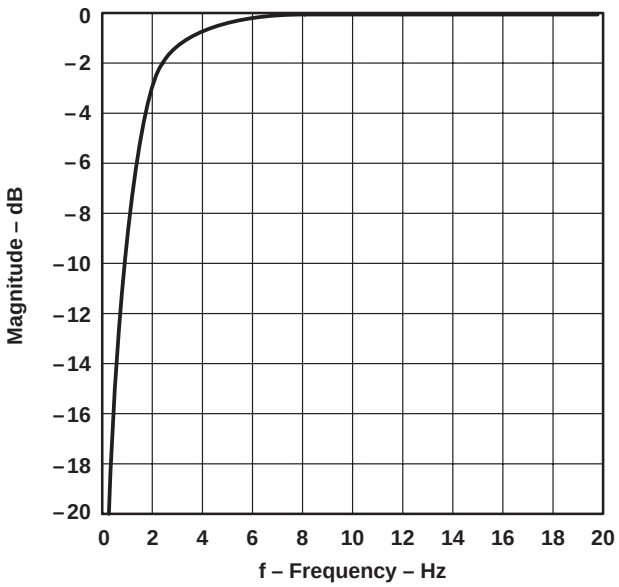


**Figure 9. TLC320AD58C High-Pass Filter Response**