Design Considerations of SN74V293 FIFO in a MicroSTAR BGA™ Package

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ABSTRACT

Texas Instruments' near-chip-scale MicroSTAR BGA™ package is gaining in popularity for applications where board space and/or weight are significant design factors. However, no less-significant design factors are those associated with electronic coupling between signal paths when leading-edge high-speed digital signals are closely spaced.

With a few simple routing and trace-location considerations, not only can the MicroSTAR BGA be used at speed without signal degradation, the short MicroSTAR BGA signal paths with optimized internal routing offer some electrical advantages as well.

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Introduction

Addressing the thrust in electronic packaging for lighter, smaller, and faster, Texas Instruments now offers the new SN74V293 series 9–18 × 9–18 selectable 65-Kbyte FIFO in a near-chip-scale ball grid array (BGA) package. Where board space is at a premium, this package offers significant space-saving advantages, as well as the well-known BGA ease of handling and board mounting (see Figure 1).
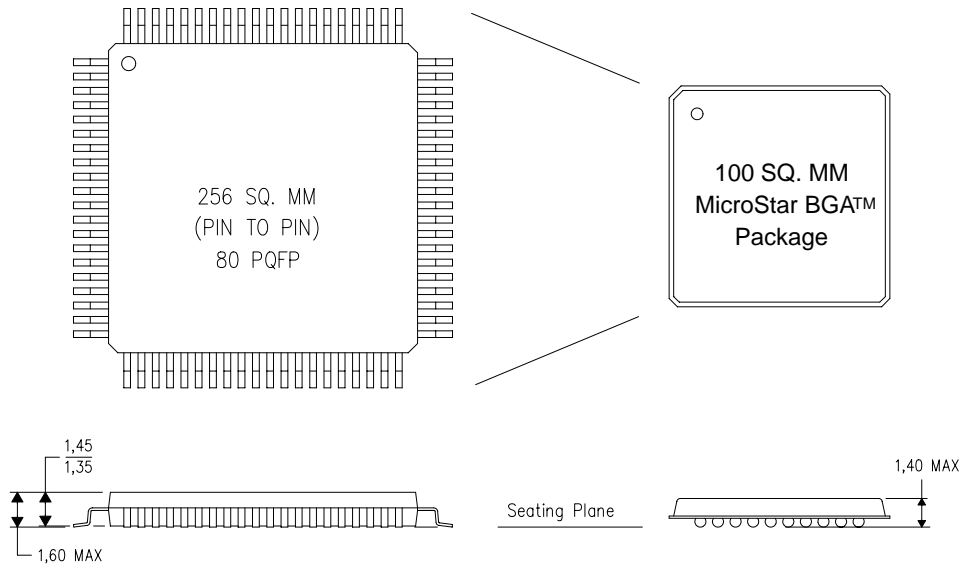
**Figure 1. MicroSTAR BGA™ Package Area Requirements
of the Two Available SN74V293 Packages**

Due to the compact pin pattern on the MicroSTAR BGA package, in addition to the high clock rate of the SN74V293 series, special trace design and routing must be complemented to avoid negating the advantageous electrical properties of this package.

Design Considerations

Several factors should be taken into account when designing a printed circuit board (PCB) for high-frequency FIFOs in MicroSTAR BGA packages. Some of the factors are:

- Electromagnetic interference (EMI)
- Electromagnetic coupling (EMC)
- Reflections and connections impedances
- Switching-related noise

To reduce EMI and EMC effects, using short microstrip lines and interlayer connections and providing stable characteristic impedance for connections is recommended.

For example, a simple microstrip line on an FR-4 PCB has the impedance shown in equation 1.

$$Z = \left(\frac{87}{\sqrt{e + 1.41}} \right) \ln \left(\frac{5.98\ H}{0.8\ W + t} \right) = 106.3\ \Omega^{\dagger} \tag{1}$$

Where:
    e = 4.65 dielectric constant of the PCB material at F >100 MHz
    H = 0.5-mm thickness of the PCB material[†]
    W = 0.100-mm BGA maximum conductor thickness
    t = 0.07-mm thickness of the conductor

High-frequency circuits with a characteristic impedance of 75 Ω or more demonstrate lower power consumption compared to common 50-Ω systems, but dc performance is slightly lower.

With CMOS devices connected to the FIFO, dc performance is not an important factor, but propagation delay is. In the previous case, the line propagation delay is calculated as:

$$t_{pd} = 1.017 \sqrt{0.475e + 0.67} = 1.72\ \text{ns/f or } 0.14\ \text{ns/in.} \tag{2}$$

For example, for an unterminated 2-in. microstrip line, FIFO output rise time (0.1 to 0.9 level) should be more than:

$$t_r\ \text{min} = 2t_{pd} \times \text{length} = 2 \times 0.14 \times 2 = 0.56\ \text{ns} \tag{3}$$

At 166 MHz and V_{CC} = 3.3 V, the SN74V293 FIFO has 0.9 t_r – 0.1 t_r = 1.15 ns, even with C_L = 5 pF.

Thus, this connection would be an appropriate approach. However, introduction of load capacitance decreases impedance and increases propagation delay, which requires shortened connections to maintain a good reflection noise margin in the PCB design.

EMI and EMC performance could be improved significantly using multilayer board design and shorter interconnects.

[†]IPC-D-317A, *Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques*, January 1995.

Simultaneous-switching noise is an important factor that should be considered during package-pinout and PCB design. This noise is caused by capacitive coupling between device pins, as well as by the inductance of the package. The equivalent schematic for two adjacent outputs is shown in Figure 2.
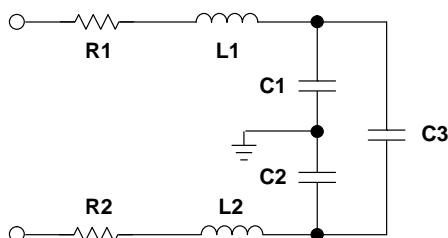
Figure 2. Equivalent Schematic of Noise-Generating Components

Values of components in Figure 2 are:

R1 = R2 = 0.066 Ω
L1 = L2 = 2.257 nH
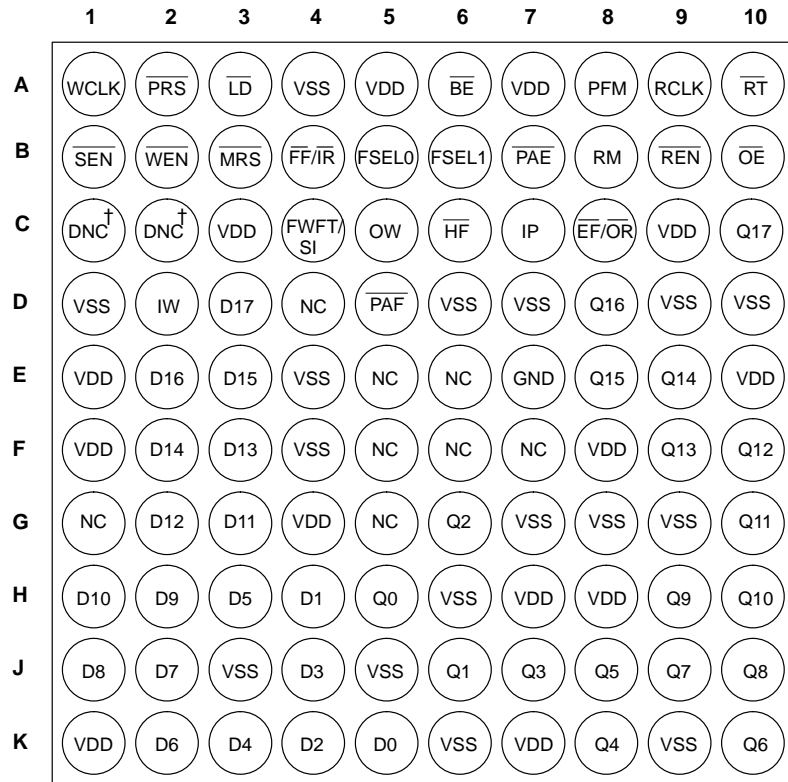C1= C2 = 0.264-pF average BGA package resistance, inductance, capacitance
C3 = 0.25-pF parasitic-coupling capacitance

Capacitive coupling between adjacent package pins is a very important factor. If inputs or outputs are switching at high frequencies, the noise through the interpin coupling can be sufficient to disturb the edges of the signal.

With a BGA package, it is very important to place pins so that capacitive-coupling noise is minimized. Isolating inputs and outputs from each other using power or ground pins as much as possible is recommended.

All inputs and outputs of the SN74V293 BGA package are grouped together and are sufficiently isolated with GND pins (see Figure 3). Also, sensitive pins, such as WCLK, RCLK, WEN, REN, MRS, PRS, are located in rows A and B of the package, providing lower noise interference and better PCB layout.

	1	2	3	4	5	6	7	8	9	10
A	WCLK	$\overline{\text{PRS}}$	$\overline{\text{LD}}$	VSS	VDD	$\overline{\text{BE}}$	VDD	PFM	RCLK	$\overline{\text{RT}}$
B	$\overline{\text{SEN}}$	$\overline{\text{WEN}}$	$\overline{\text{MRS}}$	$\overline{\text{FF}}/\overline{\text{IR}}$	FSEL0	FSEL1	$\overline{\text{PAE}}$	RM	$\overline{\text{REN}}$	$\overline{\text{OE}}$
C	DNC†	DNC†	VDD	FWFT/SI	OW	$\overline{\text{HF}}$	IP	$\overline{\text{EF}}/\overline{\text{OR}}$	VDD	Q17
D	VSS	IW	D17	NC	$\overline{\text{PAF}}$	VSS	VSS	Q16	VSS	VSS
E	VDD	D16	D15	VSS	NC	NC	GND	Q15	Q14	VDD
F	VDD	D14	D13	VSS	NC	NC	NC	VDD	Q13	Q12
G	NC	D12	D11	VDD	NC	Q2	VSS	VSS	VSS	Q11
H	D10	D9	D5	D1	Q0	VSS	VDD	VDD	Q9	Q10
J	D8	D7	VSS	D3	VSS	Q1	Q3	Q5	Q7	Q8
K	VDD	D6	D4	D2	D0	VSS	VDD	Q4	VSS	Q6

† DNC = Do not connect

Figure 3. SN74V293BGA MicroSTAR BGA™ Package Pinout (Top View)

Consider the operation of two adjacent outputs of SN74V293BGA (Q8 and Q10 for example). A simplified connection, including package parameters, is shown in Figure 4.
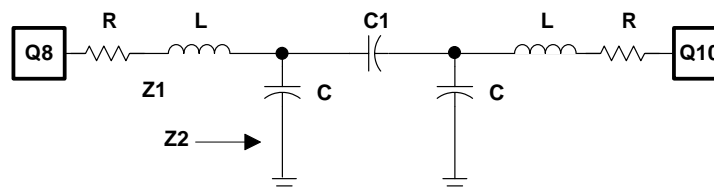
Figure 4. Schematic of Q8 and Q10 Connections, Including Package Components

The transfer function to the load capacitance (including package capacitance) is:
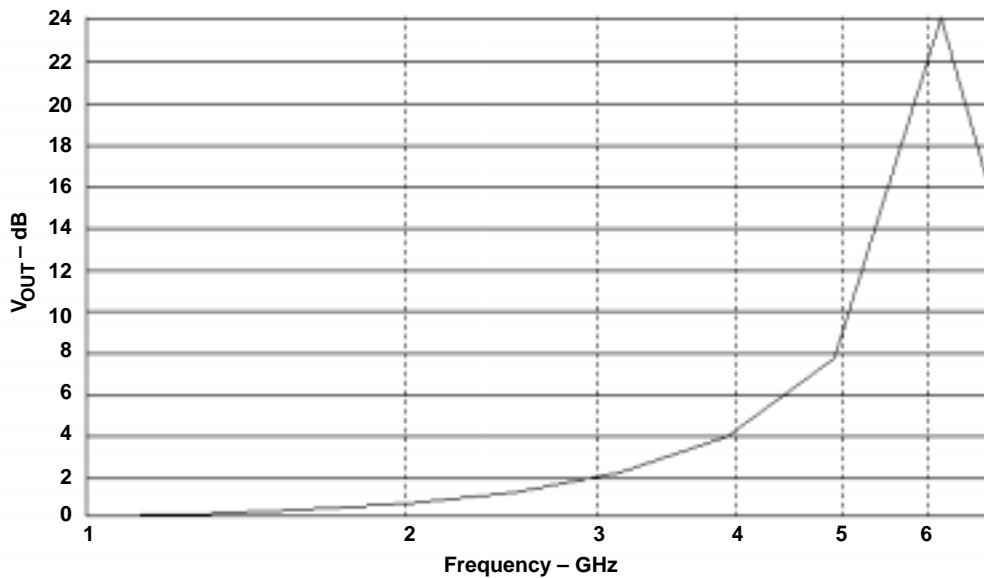
$$Z_2/(Z_1 + Z_2)$$

Where:

$Z_1 = R + sL$
C_1 = coupling between package pins

$$Z_2 = \cfrac{1}{sC + \cfrac{1}{\frac{1}{sC_1} + \cfrac{1}{sC + \frac{1}{sL + R}}}} = \frac{s^2(C + C_1)L + R(C + C_1)s + 1}{s^3C(C + 2C_1)L + RC(C + 2C_1)s^2 + (C + C_1)s} \tag{4}$$

Figure 5 shows the Bode-plot SPICE frequency response at C_1, indicating resonance at 6.3 GHz.

**Figure 5. Bode Plot of Coupling Resonance Between Typical Package Pins**

The bandwidth at 3 dB is approximately 3.3 GHz, from which it can be concluded that the BGA package allows the device to operate with t_r = 0.35/BW = 100 ps. This is much faster than timing requirements for such a high-speed device as the SN74V293BGA.

Figure 6 shows the output waveform of Q8 and Q10 when Q8 and Q10 transition from high to low simultaneously (100% in phase). The influence of package-related parameters is minimal, even at high operating frequencies.
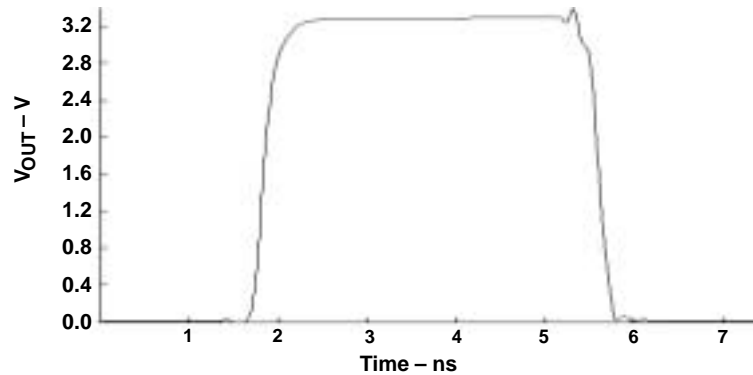
Figure 6. Waveform of SN74V293 Adjacent Outputs Switched High to Low Simultaneously

Figure 7 shows the output waveform at Q8 when Q8 and Q10 switch 180 degrees out of phase. Even if outputs are 180 degrees out of phase, when one output switches to high and the other switches to low, no significant package-related distortions are apparent.
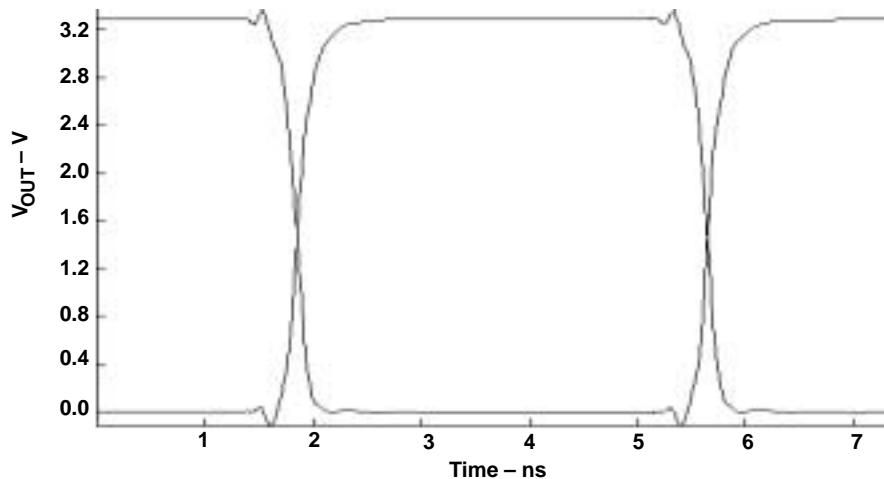
Figure 7. Waveform of SN74V293 Adjacent Outputs Switched High to Low and Low to High

Package capacitive coupling is minimal in both cases and does not affect waveforms significantly, even at high operating frequencies. The distortions of output signals are outside the signals active transition range and are acceptable, even in very noise-sensitive systems.

Conclusion

Texas Instruments MicroSTAR BGA package provides a cost-effective, low-noise, high-pin-density solution for FIFOs capable of operating at frequencies above 150 MHz. Influence of package parasitic parameters is negligible, and an appropriate device design and pinout provide an adequate V_{CC}-to-GND pin isolation for even better performance.

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