Metastability Performance of Clocked FIFOs

First-In, First-Out Technology

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Introduction

This report is intended to help the user understand more clearly the issues relating to the metastable performance of Texas Instruments (TI) clocked FIFOs in asynchronous-system applications. It discusses basic metastable-operation theory, shows the equations used to calculate metastable failure rates for one and two stages of synchronization, and describes the approach TI has used for synchronizing the status flags on its series of clocked FIFOs. Additionally, a test setup for measuring the failure rate of a device to determine its metastability parameters is shown and results are given for both an advanced BiCMOS (ABT) FIFO and an advanced CMOS (ACT) FIFO. Using these parameters, calculations of MTBF under varying conditions are performed.

Metastability

Metastability in digital systems occurs when two asynchronous signals combine in such a way that their resulting output goes to an indeterminate state. A common example is the case of data violating the setup and hold specifications of a latch or a flip-flop. In a synchronous system, the data always has a fixed relationship with respect to the clock. When that relationship obeys the setup and hold requirements for the device, the output goes to a valid state within its specified propagation delay time. However, in an asynchronous system, the relationship between data and clock is not fixed; therefore, occasional violations of setup and hold times can occur. When this happens, the output may go to an intermediate level between its two valid states and remain there for an indefinite amount of time before resolving itself or it may simply be delayed before making a normal transition[1]. In either case, a metastable event has occurred.

Metastable events can occur in a system without causing a problem, so it is necessary to define what constitutes a failure before attempting to calculate a failure rate. For a simple CMOS latch, as shown in Figure 1, valid data must be present on the input for a specified period of time before the clock signal arrives (setup time) and must remain valid for a specified period of time after the clock transition (hold time) to assure that the output functions predictably. This leaves a small window of time with respect to the clock (t_0) during which the data is not allowed to change. If a data edge occurs within this aperture, the output may go to an intermediate level and remain there for an indefinite amount of time before resolving itself either high or low, as illustrated in Figure 2. This metastable event can cause a failure only if the output has not resolved itself by the time that it must be valid for use (for example, as an input to another stage); therefore, the amount of resolve time allowed a device plays a large role in calculating its failure rate.

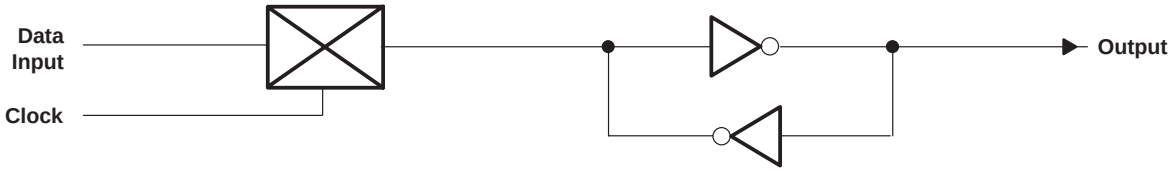

Figure 1. A Simple CMOS Latch

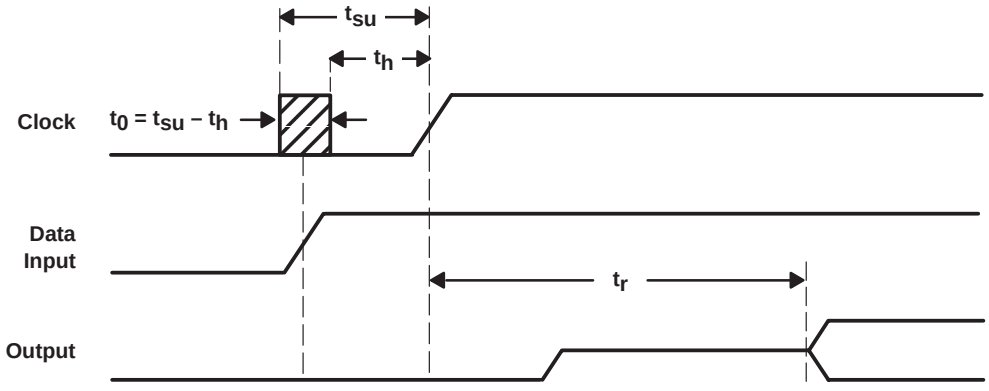

Figure 2. Output at Intermediate Level Due to Data Edge Within t_0 Aperture

The probability of a metastable state persisting longer than a time, t_r, decreases exponentially as t_r increases[2]. This relationship can be characterized by equation 1:

$$f_{(r)} = e^{(-t_r/\tau)} \quad (1)$$

where the function f(r) is the probability of nonresolution as a function of resolve time allowed, t_r, and the circuit time constant τ (which has also been shown to be inversely proportional to the gain-bandwidth product of the circuit)[3,4].

For a single-stage synchronizer with a given clock frequency and an asynchronous data edge that has a uniform probability density within the clock period, the rate of generation of metastable events can be calculated by taking the ratio of the setup and hold time window previously described to the time between clock edges and multiplying by the data edge frequency. This generation rate of metastable events coupled with the probability of nonresolution of an event as a function of the time allowed for resolution gives the failure rate for that set of conditions. The inverse of the failure rate is the mean time between failure (MTBF) of the device and is calculated with the formula shown in equation 2:

$$\frac{1}{\text{failure rate}} = \text{MTBF}_1 = \frac{e^{(t_r/\tau)}}{t_0\ f_c\ f_d} \quad (2)$$

Where:

t_r = resolve time allowed in excess of the normal propagation delay time of the device
t = metastability time constant for a flip-flop
t_0 = a constant related to the width of the time window or aperture wherein a data edge triggers a metastable event
f_c = clock frequency
f_d = asynchronous data edge frequency

The parameters t_0 and t are constants that are related to the electrical characteristics of the device in question. The simplest way to determine their values is to measure the failure rate of the device under specified conditions and solve for them directly. If the failure rate of a device is measured at different resolve times and plotted, the result is an exponentially decaying curve. When plotted on a semilogarithmic scale, this becomes a straight line the slope of which is equal to τ; therefore, two data points on the line are sufficient to calculate the value of τ using equation 3:

$$\tau = \frac{t_{r2} - t_{r1}}{\ln(N1/N2)} \quad (3)$$

Where:

t_{r1} = resolve time 1
t_{r2} = resolve time 2
N1 = number of failures relative to t_{r1}
N2 = number of failures relative to t_{r2}

After determining the value for τ, t_0 may be solved for directly.

The formula for calculating the MTBF of a two-stage synchronizer, equation 4, is merely an extension of equation 2:

$$\text{MTBF}_2 = \frac{e^{(t_{r1}/\tau)}}{t_0\ f_c\ f_d} \times e^{(t_{r2}/\tau)} \quad (4)$$

Where:

t_{r1} = resolve time allowed for the first stage of the synchronizer
t_{r2} = resolve time allowed in excess of the normal propagation delay
f_c, f_d, t, and t_0 are as previously defined, with t and t_0 assumed to be the same for both stages.

The first term calculates the MTBF of the first stage of the synchronizer, which in effect becomes the generation rate of metastable events for the next stage. The second term then calculates the probability that the metastable event will be resolved based on the value of t_{r2}, the resolve time allowed external to the synchronizer. The product of the two terms gives the overall MTBF for the two-stage synchronizer.

TI Clocked FIFOs

The TI clocked FIFOs are designed to reduce the occurrence of metastable errors due to asynchronous operation. This is achieved through the use of two- and three-stage synchronizing circuits that generate the status-flag outputs input ready (IR) and output ready (OR). In a typical application, words may be written to and then read from the FIFO at varying rates independent of one another, resulting in asynchronous flag-signal generation (internally) at the boundary conditions of full and empty; for example, the operation when the FIFO is at the full boundary condition with writes taking place faster than and asynchronous to reads. The IR flag is low, signifying that the FIFO is full and can accept no more words. When a read occurs, the FIFO is no longer completely full. This causes an internal flag signal to go high, allowing another write to take place. Since the exit from the full state happens asynchronously to the write clock (WRTCLK) of the FIFO, this flag is not useful as a system write-enable signal. The solution is to synchronize this internal flag to the write clock through two D-type flip-flop stages and output this synchronized signal as the IR flag (see Figure 3). The OR status flag is generated in a similar manner at the empty boundary condition and is synchronized to the read clock through a three-stage synchronizing circuit.

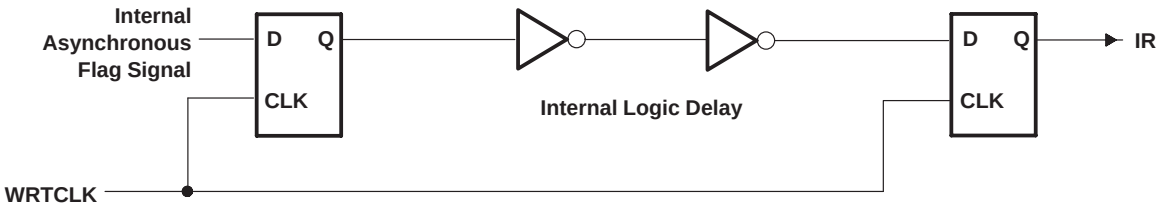

Figure 3. IR-Flag Synchronizer

The remainder of this report pertains to the metastability performance of the two-stage IR synchronizer, which is the limiting case of the two in terms of MTBF characteristics. The internal flag signal that goes high on a read and low on a write is synchronized to the write clock through two D-type flip-flop stages. Since this results in the IR flag status of the FIFO being delayed for two clock cycles, a predictive circuit is used to clock the status into the synchronizer at (full minus two) words so that the action of the IR flag going low coincides with the actual full status of the FIFO. However, once the FIFO is full and IR is low, a read that causes the internal flag to go high is not reflected in the status of the IR flag until two write clocks occur.

With the FIFO full and the IR flag low, a read causes the internal flag signal to go high. This signal is clocked into the first stage of the two-stage synchronizer on the next write clock. Because these two signals are asynchronous to one another, the potential for the output of the first stage of the synchronizer to go to a metastable state exists. If this condition persists until the next write clock rising edge, a metastable condition could be generated in the second stage and reflected on the IR flag output. This metastable condition manifests itself as a delay in propagation time and is considered a failure only if it exceeds the maximum delay allowed in a design.

The effectiveness of the two-stage synchronizer becomes apparent when attempting to generate failures at a rate high enough to count in a reasonable period of time. A metastable event generated in the first stage must persist until the next write clock, i.e., when that data is transferred to the second stage. The resolve time for the first stage is governed by the frequency or period of the write clock. At slower frequencies, the failure rate of the first stage is very low, resulting in a low metastable generation rate to the second stage. The second stage of the synchronizer further reduces the probability of a metastable failure based on the resolve time allowed at the output. The overall failure rate of the device may be affected by increasing the initial asynchronous data generation rate (adding jitter to the data centered about the setup and hold window), by decreasing the resolve time of the first stage (increasing the write clock frequency), and by reducing the external resolve time at the output.

Test Setup for Measuring FIFO Flag Metastability

The failure rate of a device is measured on a test fixture as shown in Figure 4. The input waveforms used on this setup are also shown in Figure 4. Rising data is jittered asynchronously about the setup and hold aperture of the device under test (DUT) in a ±400-ps window with respect to the device clock (CLK). The output of the DUT is then clocked into two separate flip-flops, FF1 and FF2, by two different clock signals, CLK1 and CLK2. The resolve time, t_r, is set by the relationship between CLK1 and CLK and is measured as the delta between the normal output transition time and the rising edge of CLK1 minus the setup time required for FF1. CLK2 occurs long enough after CLK1 to allow sufficient time for the DUT to have resolved itself to a valid state. The outputs of FF1 and FF2 are compared by the exclusive OR gate, the output state of which is latched into FF3 by CLK3. When a metastable failure occurs, the output of the exclusive OR gate goes high caused by FF1 and FF2 having opposite data due to the DUT not having resolved itself by time t_r. On the next cycle, low data is clocked into the DUT and FF1 and FF2 in order to reset the status latch, FF3. Failures are counted for different resolve times, and τ is then calculated using equation 3.

Using the test setup in Figure 4, failure rates are measured for both an SN74ABT7819, $512 \times 18 \times 2$ clocked FIFO, and an SN74ACT7807, $2K \times 9$ clocked FIFO. The device is initially written full to set IR low at the boundary condition. A read clock is generated to send the internal flag high, and a jitter signal is superimposed on it to sweep asynchronously with respect to the write clock in an 800-ps-wide envelope and centered such that the IR flag goes high alternately on the second and third write clocks. The nominal write-clock frequency of the test setup is 40 MHz, but to increase the failure rate to an observable level, a pulse is injected into the write-clock stream just after the read clock occurs such that the first and second write clocks (the ones that clock the status through the synchronizer) are only 5.24 ns apart. This increases the effective write clock frequency to 191 MHz, reducing the resolve time allowed in the first stage and increasing the failure rate.

This test setup and these actions together create the necessary conditions to generate a metastable occurrence on the IR output that is seen after the second write clock and manifests itself as a delay in propagation time. In this instance, the write clock is the synchronizing clock and the read clock generates the asynchronous internal data signal. CLK1 is adjusted to vary the external resolve time, t_{r2}, and the resulting failure rates are recorded (see Table 1).

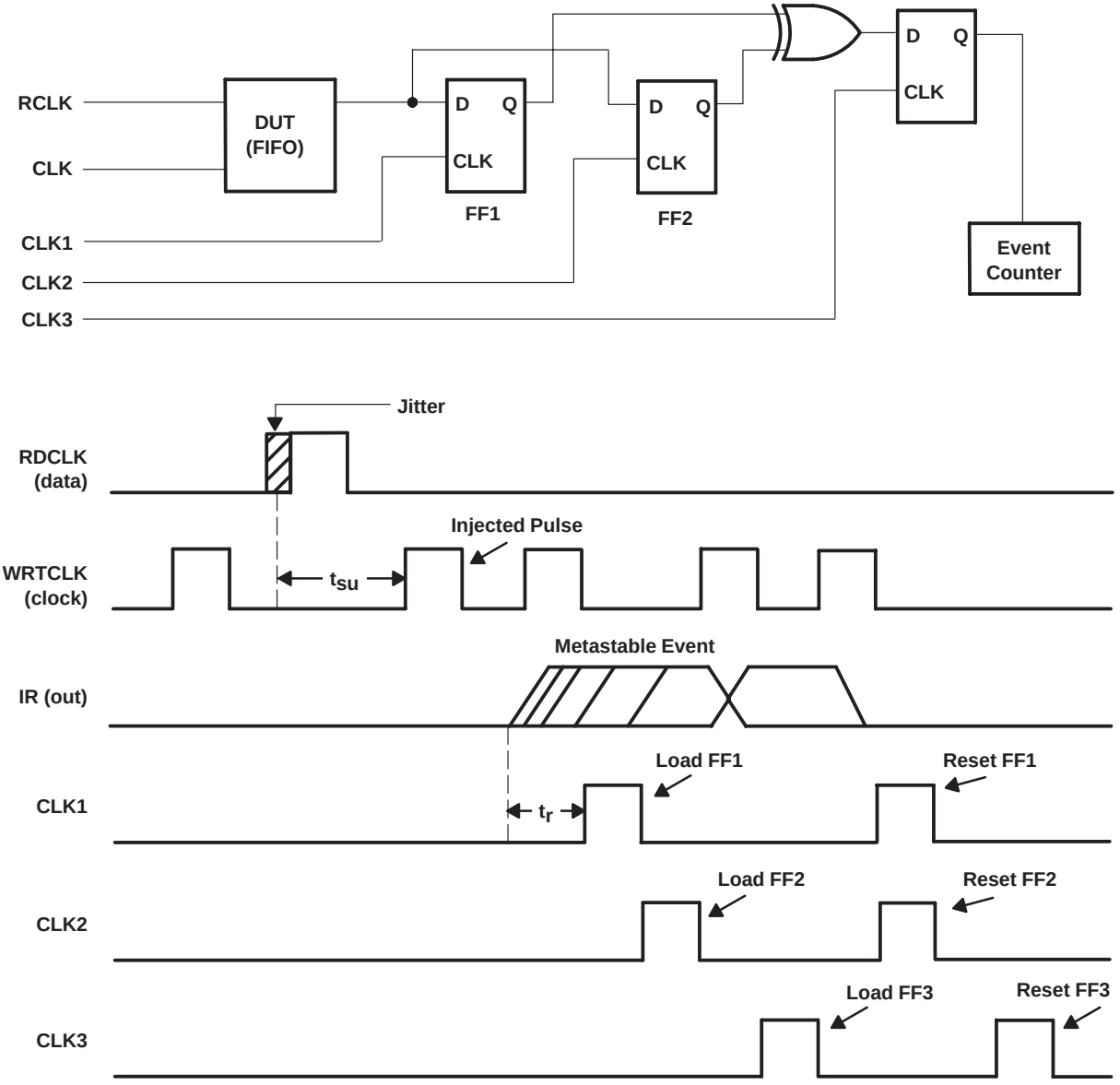

Figure 4. Metastable Event Counter and Input Waveforms

Test Results

Table 1. SN74ABT7819 Failure Rates†

RESOLVE TIME, t_{r2} (ns)	NUMBER OF FAILURES/HOUR	NUMBER OF FAILURES/SECOND	MTBF (seconds)
0.27	890	0.2472	4.04
0.39	609	0.1692	5.91
0.53	396	0.1101	9.08

† V_{CC} = 4.5 V, T_A = 25°C

After measuring the metastable performance of the SN74ABT7819, some assumptions must be made to calculate the parameters τ and t_0. Because the individual flip-flops comprising the two-stage synchronizer cannot be measured separately, it is first assumed that the values for τ and t_0 are the same for both. This is a safe assumption, as these constants are driven by the process technology and because the schematics are identical. The other assumption made involves determining the resolve time allowed in the first stage of the synchronizer. The clock period is set at 5.24 ns, but the delay through the flip-flop and the setup time to the next stage must be subtracted from the clock period to arrive at the true resolve time (t_{r1}). These values could not be measured directly and were, therefore, estimated from SPICE analysis to be 1.3 ns.

Using equation 4 and the measured failure rates to calculate τ results in a value of 0.33 ns for the conditions given. The following values from the test setup must be used to solve for t_0:

Where:

t_{r1} = 3.94 ns (5.24-ns clock period – 1.3-ns setup and delay time)
t_{r2} = 0.27 ns (set externally at IR output by CLK1)
f_c = 40 MHz
f_d = 125 MHz (4-MHz input adjusted by 25/0.8 jitter ratio)
$MTBF^2$ = 4.04 s

Substituting these values into equation 4 and solving for t_0 yields a value of 16.9 ps.

Table 2 summarizes the results for the SN74ABT7819 and SN74ACT7807 clocked FIFOs. An internal setup and delay time of 1.8 ns was assumed for the SN74ACT7807.

Table 2. Values of τ and t_0 for SN74ABT7819 and SN74ACT7807

T_A	V_{CC}	SN74ABT7819		SN74ACT7807	
		τ (ns)	t_0 (ps)	τ (ns)	t_0 (ps)
25°C	4.5 V	0.33	16.9	0.50	1.13
	5 V	0.30	7	0.40	2.05
	5.5 V	0.23	28.8	0.30	9.40

These numbers indicate the performance of only a few devices and are not intended to represent a fully characterized parameter. However, they should be valid for the purpose of relative performance comparisons, and the values do fall within the expected range given the circuit configuration and process technology in which the devices are fabricated.

MTBF Comparisons

With the constants τ and t_0 now known, calculations of the MTBF of the device under different operating conditions may be performed. First, however, consider an example of the metastability performance of a single-stage synchronizer using equation 1 and the circuit constants τ and t_0 from Table 2. Assume an application running with a 33-MHz write clock, an 8-MHz read clock, a 9-ns maximum propagation delay time for the IR path, and a 5-ns setup time for IR to the next device. Therefore:

t_r = 16 ns (30-ns clock period – 9-ns propagation delay – 5-ns t_{su})
f_c = 33 MHz
f_d = 8 MHz

Using equation 2 to calculate the MTBF gives 2.55 y 10^{17} seconds or a little bit more than 8 billion years.

The reliability of a one-stage synchronizer degrades as operating frequency increases. With a 50-MHz write clock, a 12-MHz read clock, a 9-ns maximum delay, and a 5-ns setup time:

t_r = 6 ns (20-ns clock period – 9-ns propagation delay – 5-ns t_{su})
f_c = 50 MHz
f_d = 12 MHz

Substituting these values into equation 2 yields an MTBF of about 2 hours. This performance is unacceptable, even with a device fabricated in the 0.8-mm BiCMOS process, which is more resistant to metastability than other processes.

The benefits of two-stage synchronization become evident with the next example. Using the conditions stated in the last example:

t_{r1} = 18.7 ns (20-ns clock period – 1.3-ns setup and delay time)
t_{r2} = 6 ns (20-ns clock period – 9-ns propagation delay – 5-ns t_{su})
f_c = 50 MHz
f_d = 12 MHz

Using equation 4 to calculate the MTBF gives 3.16 y 10^{28} seconds or 1.00 y 10^{21} years.

Table 3 gives a performance summary of both one- and two-stage synchronizing solutions under different conditions.

Table 3. MTBF Comparisons†

CONDITIONS	ACT 1 STAGE	ABT 1 STAGE	ACT 2 STAGE	ABT 2 STAGE
f_c = 33 MHz, f_d = 8 MHz	8400 years	8.1×10^9 years	2.62×10^{28} years	4.77×10^{47} years
f_c = 40 MHz, f_d = 10 MHz	92 days	1400 years	3.56×10^{19} years	2.18×10^{34} years
f_c = 50 MHz, f_d = 12 MHz		2 hours	4.90×10^{10} years	1.00×10^{21} years
f_c = 67 MHz, f_d = 16 MHz			417 years	1.28×10^9 years
f_c = 80 MHz, f_d = 20 MHz				2900 years

† Assumptions for the MTBF comparisons:
– The values for t_0 and τ are those given previously for both the ABT and ACT devices with V_{CC}= 4.5 V, T_A = 25°C.
– Flag propagation delay time (IR or OR) is assumed to be 9 ns.
– Setup times to the next device are 5 ns (up to 50-MHz operation), 4 ns (up to 67-MHz operation), and 3 ns (up to 80-MHz operation).

Conclusion

Metastability failures must be accounted for in the design of asynchronous digital circuits. These failures become increasingly prevalent at higher operating frequencies. When higher frequencies are used, extreme care must be taken to ensure that system reliability is not adversely affected due to inadequate synchronization methods.

Clocked FIFOs from TI provide a solution to this problem by synchronizing the boundary flags with at least two flip-flop stages to improve the metastable MTBF over one-stage synchronization. This architecture allows designers to utilize the high-throughput performance of the memory without endangering the reliability of their end products.

References

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