Design-For-Test Analysis of a Buffered SDRAM DIMM

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TEXAS INSTRUMENTS

Contents

Title *Page*

Abstract **1**

1 Introduction **1**

2 Module Construction **1**

3 Module Function **2**

4 Taxonomy of Defects **3**

5 Fault Models **6**

6 Test Methodologies **6**

7 Card-Edge Test (Module Without DFT) **6**

8 Module DFT **7**

9 In-Circuit Test **7**

10 Boundary-Scan Test **9**

10.1 Boundary Scan at Register and Clock Driver 9
10.2 Boundary Scan at Register Only 9
10.3 Boundary Scan at SDRAM ICs 9
10.4 Boundary Scan at Buffer 9
10.5 Boundary Scan: Beyond Manufacturing Test 9

11 Comparative Study **10**

12 Conclusion **10**

References **11**

List of Tables

Table *Title* *Page*

1 Summary of Module Construction 2
2 Node/Solder-Joint Matrix With Card-Edge and In-Circuit Test Fault Classification 4
3 Defined Solder-Joint Fault Model 6
4 Card-Edge Test Fault Classification 7
5 In-Circuit Test Accessibility Classification 8
6 In-Circuit Test Fault Classification 8
7 Comparison of Test Methodologies 10

Abstract

This paper presents a design-for-test (DFT) analysis of a buffered synchronous dynamic random-access memory (SDRAM) dual in-line memory module (DIMM). The analysis is restricted to board-level manufacturing faults. The test problem is described, alternate test methods are suggested, and a comparative study is presented contrasting a DFT approach – including boundary-scan test – versus a non-DFT approach.

Keywords: boundary scan, design-for-test, DFT, DIMM, DRAM, IEEE Std 1149.1, in-circuit, JTAG, memory, module, SDRAM, test.

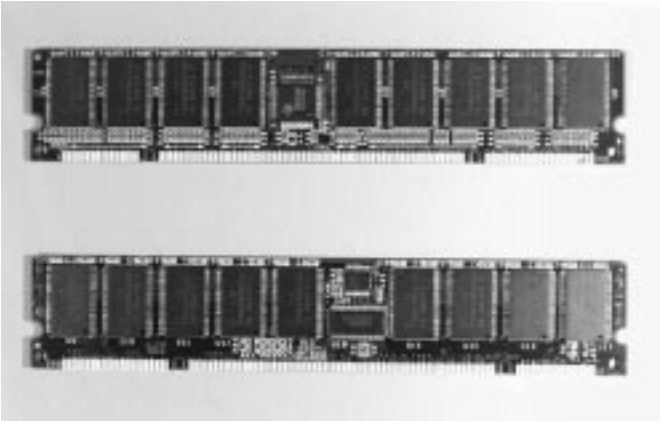

Figure 1. Subject Module (1/2X)

1. Introduction

The high quality of electronic systems being demanded by business and private consumers today is driving the growing importance that manufacturers are placing on testing as a whole. Ever-increasing miniaturization and complexity of very-large-scale integration (VLSI) integrated circuits (ICs) and systems are, in turn, leading to escalating difficulties faced by board/module manufacturers in using conventional test methods for their testing needs. The advent of new assembly technologies like fine-pitch surface-mount technology (SMT), multichip modules (MCMs), tape-automated bonding (TAB), and chip-on-board (COB) have complicated matters further.

Due to such advances, not only has it become difficult to gain physical access to probe printed-wiring-board (PWB) traces, but it has also become impractical to continue with conventional test development. With increased IC and module complexity, the high costs involved with developing test programs are recurring, as standard test programs that could be reused several times in the past, now need to be generated with a specific application in mind, due to the application-specific nature of ICs. Therefore, to maintain quality of products and increase competitive advantage while remaining economically viable, new and evolving system-level test methodologies aimed at improving overall testability must be adopted. This paper will demonstrate the applicability of such methods to a buffered SDRAM DIMM.

2. Module Construction

The analysis to be presented in this paper is based on a 200-pin, 2-bank x 2M x 72, buffered SDRAM DIMM designed at Texas Instruments (TI) according to JEDEC Standard 21-C. Figure 1 shows the subject module at half-size magnification. As shown, the module is a double-sided assembly that uses a high degree of miniaturization for both components and assembly.

The fundamental elements of the buffered SDRAM DIMM are a laminate substrate with dual-in-line edge contacts, a high-speed buffered register IC, a phase-locked-loop (PLL) clock distribution IC, several SDRAM ICs, as well as several capacitor and resistor components. Table 1 provides a summary of the module construction. As can be ascertained from this summary, all components, including passives as well as ICs, are of the fine-pitch surface-mount type.

Table 1. Summary of Module Construction

PWB							
Finished size: 1.15 in. x 6.05 in. x 0.05 in; finished cost: $10							
Substrate: glass-base epoxy resin, flame retardant (FR4) – 6 layers; edge: 200 pin, gold plate							
Wiring: copper/entek plus, size 4 mil, pitch 10 mil; vias: size 12 mil, pitch 50 mil							
ICs	**DESCRIPTION**	**NO.**	**PART NO.**	**COST $**		**PACKAGE**	**LEAD PITCH**
				UNIT	**EXT'ED**		
SDRAM	2M × 8	18	TMS626802	30.00	540.00	44-pin TSOP	0.80 mm
Buffered register	20 bit	1	ALVCH162721	5.00	5.00	56-pin TSSOP	0.50 mm
Clock driver	1-to-12 PLL	1	CDC2586	6.00	6.00	52-pin TQFP	0.65 mm
PD buffer	8 bit	1	LVC244	1.00	1.00	20-pin TSSOP	0.65 mm
PASSIVES		**NO.**		**COST $**		**PACKAGE**	**PITCH**
				UNIT	**EXT'ED**		
Shunt/tie-off resistors (0, 10)		8, 72		0.01	0.80	0603	50 mil
Bypass capacitors (0.001, 0.1)		24, 24		0.03	1.44	0603	50 mil

In the dual-bank architecture of the subject module, nine SDRAM ICs are placed on each side of the PWB. The clock driver and related passives are placed on one side of the board, while the register and buffer, along with associated passives, are placed on the other side of the board.

As noted in the construction summary, the PWB was constructed in six layers. The two outer layers were used for the data I/O and address/control buses. One inner layer was used for the clock signal routing, while another was used for routing register outputs to receiving SDRAMs on the back side. Finally, the remaining two layers were used for power (Vcc) and ground planes.

3. Module Function

The function of the subject SDRAM DIMM is shown in the block diagram of Figure 2. All address (12) and control (8) lines to the SDRAM devices are buffered and retimed through the 20-bit register. Data in/out signals are driven directly to/from the card edge via 10-ohm series damping resistors. External damping resistors are avoided on the address, clocks, and controls through the use of ICs that integrate such resistors. The single clock driver supplies buffered, phase-controlled clock signals to the register, as well as all SDRAM devices. The octal buffer sources the buffered presence-detect outputs, which provide configuration information about the DIMM. The output enable for this buffer is controlled by the presence-detect enable (PDE) signal.

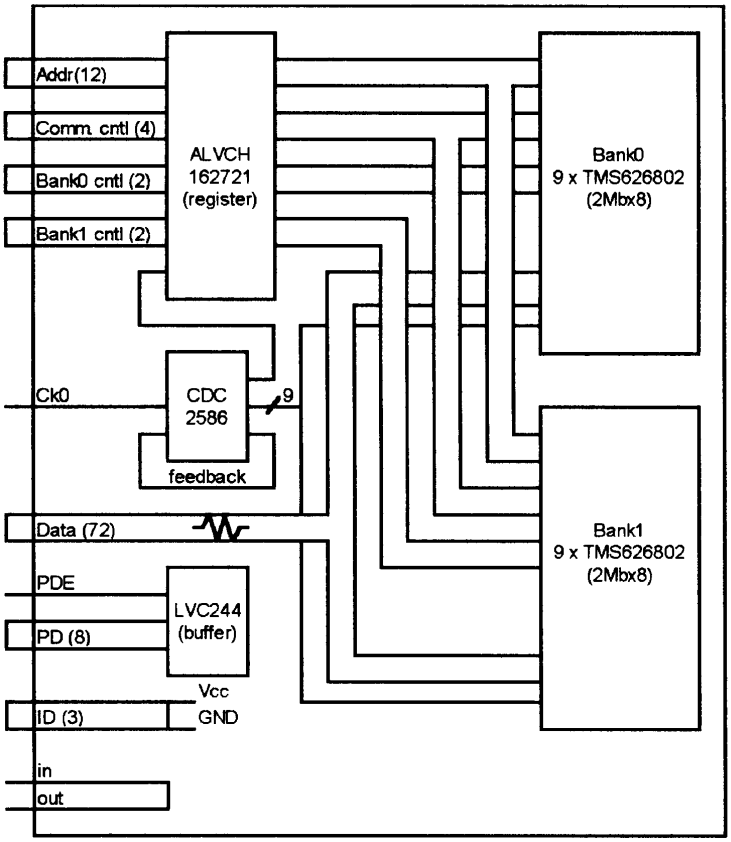

Figure 2. Module Block Diagram

4. Taxonomy of Defects

The causes for defects in a module can broadly be classified into process defects and random point defects. Process defects can result from high or abnormal variation in processing, such as in solder paste thickness, wiper pitch, etc., while point defects may result from particulate or other contamination.

Some defects that occur during the assembly process are commonly caused by manufacturing errors, such as the use of wrong components or missing components. Defects introduced during module assembly can also result from manufacturing processes, such as incorrect or insufficient paste, incorrect component placement, cold solder, solder splashes, contamination, or process damage. These may also be caused by use of defective or faulty components in the form of broken or improper leads, mislabeled parts or wrong values, or cracked components.

Regardless of their root cause, such defects can result in improper operation/function of the assembly. Therefore, testing is necessary to verify proper module function, to identify defects in faulty assemblies for rework and repair, as well as to eliminate sources of defects in the process.

A specific manifestation of a defect in an assembly is referred to as an assembly fault. These can be broadly grouped into gross and marginal classes. Marginal assembly faults are parametric in nature and deal with electrical characteristics of circuits like threshold, bias, and leakage currents and voltages. Delay faults can be classified as such. Gross assembly faults can be divided into interconnect faults, which include shorts and opens, and placement faults, which are caused by wrong component orientation or wrong part in socket.

Table 2. Node/Solder-Joint Matrix With Card-Edge and In-Circuit Test Fault Classification

SIGNAL NODES	NO.	ASSOCIATED SOLDER JOINTS	NO.	DESCRIPTION	CLASSIFICATION OF SOLDER JOINT FAULTS					ICT ACCESSIBILITY
					CARD-EDGE (NO DFT)				ICT	
					ss/ L	ss/ H	so/ L†	so/ H†	so‡	
Edge → Reg(addr)	12	Reg-I(addr)	12	Module Address Inputs	fA	fA	fA	fA	iB	a
Edge → Reg(cas)	1	Reg-I(cas)	1	Module Column-Address Strobe Input	fX	fX	fX	fX	iB	a
Edge → Reg(cke)	2	Reg-I(cke)	2	Module Clock Enable Inputs 1 per bank	fX’	fQ	fX’	fQ	iB	a
Edge → Reg(dqm)	1	Reg-I(dqm)	1	Module Data/ Output Mask Enable Input	fR	fX	fR	fX	iB	a
Edge → Reg(ras)	1	Reg-I(ras)	1	Module Row-Address Strobe Input	fX	fX	fX	fX	iB	a
Edge → Reg(s)	2	Reg-I(s)	2	Module Chip Select Inputs 1 per bank	fX’	fX’	fX’	fX’	iB	a
Edge → Reg(w)	1	Reg-I(w)	1	Module Write Enable Input	fX	fX	fX	fX	iB	a
Edge → CDC(clk)	1	CDC-I(clkin)	1	Module System Clock Input	fX	fX	fX	fX	iC	a
Edge → Buf(pde)	1	Buf-I(pde)	2	Module Presence Detect Enable Input	fS	fS	fS	fS	iS	a
Edge → Shunt(id)	3	Shunt-head(id) Shunt-tail(id)	3	Module Identification Output	fT	fT	fT	fT	iT	a x
Edge ↔ Shunt(in/out)	2	Shunt-head(in/out) Shunt-tail(in/out)	1	Module Physical Presence Detect Input/Output	fU	fU	fU	fU	iT	a
Edge ↔ SDRAM(dq):	72	Resistor-head	72	Module Data Input/Data Output All SDRAM I/Os are driven through 10-ohm resistors to/from card edge	fV	fV	fV	fV	iV	a
Edge ↔ Resistor	72	Resistor-tail	72		fV	fV	fV	fV	iV	d
Resistor ↔ SDRAM(dq)	72	SDRAM-I/O(dq)	144		fV	fV	fV	fV	iV	
Edge	8	Buf-O(pd)	4	Module Logical Presence	fW	fW	fW	fW	iB	a
				Detect Outputs	fW’	fW’	fW’	fW’		
Reg → SDRAM(addr)	12	Reg-O(addr)	12	SDRAM Address	fA	fA	fA	fA	iB	b
		SDRAM-I(addr)	216				fA’	fA’	iA’	
Reg → SDRAM(cas)	1	Reg-O(cas)	1	SDRAM Column-Address Strobe	fX	fX	fX	fX	iB	b
		SDRAM-I(cas)	18				fX’’’	fX’’’	iX’’’	
Reg → SDRAM(cke)	2	Reg-O(cke)	2	SDRAM Clock Enable 1 per bank	fX’	fQ	fX’	fQ	iB	b
		SDRAM-I(cke)	18				fX’’’	fQ’	iX’’’	
Reg → SDRAM(dqm)	1	Reg-O(dqm)	1	SDRAM Data/Output Mask Enable	fR	fX	fR	fX	iB	b
		SDRAM-I(dqm)	18				fR’	fX’’’	iX’’’	
Reg → SDRAM(ras)	1	Reg-O(ras)	1	SDRAM Row-Address Strobe	fX	fX	fX	fX	iB	b
		SDRAM-I(ras)	18				fX’’’	fX’’’	iX’’’	
Reg → SDRAM(s)	2	Reg-O(s)	2	SDRAM Chip Select 1 per bank	fX’	fX’	fX’	fX’	iB	b
		SDRAM-I(s)	18				fX’’’	fX’’’	iX’’’	
Reg → SDRAM(w)	1	Reg-O(w)	1	SDRAM Write Enable	fX	fX	fX	fX	iB	b
		SDRAM-I(w)	18				fX’’’	fX’’’	iX’’’	

n/c = not considered; n/f = no fault
† noise injected onto open inputs may cause intermittent/unexpected results
‡ assuming 100% node coverage

Table 2. Node/Solder-Joint Matrix With Card-Edge and In-Circuit Test Fault Classification (Continued)

SIGNAL NODES	NO.	ASSOCIATED SOLDER JOINTS	NO.	DESCRIPTION	CLASSIFICATION OF SOLDER JOINT FAULTS					ICT ACCESSIBILITY
					CARD-EDGE (NO DFT)				ICT	
					ss/ L	ss/ H	so/ L†	so/ H†	so‡	
CDC → SDRAM(clk)	9	CDC-O(clk)	9	SDRAM System Clock	fX''	fX''	fX''	fX''	iC'	b/c
		SDRAM-I(clk)	18				fX'''	fX'''	iX'''	
CDC → Reg(clk)	1	CDC-O(clk)	1	Register System Clock	fX	fX	fX	fX	iC'	b
		Reg-I(clk)							iD	
CDC → CDC(fb)	1	CDC-O(fb)	1	CDC External Feedback	fX	fX	fX	fX	iC'	b
		CDC-I(fb)							iC	
Buf ← Shunt(pd-I)	4	Buf-I(pd)	4	Buffer Input (Presence Detect) Tie-offs	fW	fW	fW	fW	iB'	d
		Shunt-head(pd)							iT	
		Shunt-tail(pd)							iT	x
		OTHER SOLDER JOINTS								
		Reg-I(clken)	1	Reg Clock Enable (to be low)	n/f	fX	n/f	fX	iD	x
		Reg-I(NC)	1	Reg No-Connect (to be low)	n/f	n/f	n/f	n/f	n/f	x
		Reg-I(oe)	1	Reg Output Enable (to be low)	n/f	fX	n/f	fX	iS	x
		CDC-I(clr)	1	CDC Clear (to be low)	n/f	n/f	n/f†	n/f†	n/f†	x
		CDC-I(NC)	1	CDC No-Connect (to be low)	n/f	n/f	n/f	n/f	n/f	x
		CDC-I(oe)	1	CDC Output Enable (to be low)	n/f	fX	n/f	fX	iS	x
		CDC-I(sel)	2	CDC Select (to be low)	n/f	fY	n/f	fY	iY	x
		CDC-I(test)	1	CDC Test (to be low)	n/f	fZ	n/f	fZ	iZ	x
		SDRAM-I(NC)	90	SDRAM No-Connect (to be low)	n/f	n/f	n/f	n/f	n/f	x
		Buf-I(pd)	4	Buf Input (Presence Detect -- to be low)	n/f	fW'	n/f	fW'	iB	x
		Reg-Power	12	Register Vcc/GND	n/c	n/c	n/c	n/c	n/c	x
		CDC-Power	32	CDC Vcc/GND	n/c	n/c	n/c	n/c	n/c	x
		SDRAM-Power	216	SDRAM Vcc/GND	n/c	n/c	n/c	n/c	n/c	x
		Buf-Power	2	Buffer Vcc/GND	n/c	n/c	n/c	n/c	n/c	x
		Cap-head	48	Bypass Capacitors	n/c	n/c	n/c	n/c	n/c	x
		Cap-tail								
TOTAL SIGNAL NODES	**214**	**TOTAL SOLDER JOINTS**	**1175**							

n/c = not considered; n/f = no fault
† noise injected onto open inputs may cause intermittent/unexpected results
‡ assuming 100% node coverage

Because of its construction, the module typically is subject to such manufacturing defects and consequent assembly faults. As the majority of defects in fine-pitch surface-mount assemblies, especially those associated with process rather than human error, directly affect solder joints, the analysis presented in this paper addresses that issue. Columns 1 to 5 of Table 2 enumerate the signal nodes, their associated solder joints, and other solder joints (those associated with Vcc/GND nodes) in the module.

5. Fault Models

For faults to be modeled or simulated – for coverage and diagnostic analysis among other purposes – they must be represented mathematically by abstraction through a logical model. Such logical models are called fault models. They constitute a basic set of assumptions that represent such faults. By such abstraction, the problem of modeling physical faults is reduced to a logical level that can represent the effects of physical faults on the behavior of the system. The process of fault analysis is also simplified by converting faults across several technologies into logical fault models that are independent of process.

A fault model used pervasively in many sorts of test and DFT analysis is the single-stuck-at model, in which a single defective node is presumed to behave as if it were constantly held to a static low or high level. For our analysis, this model will be extended to comprehend faults resulting from defects in solder joints.

Each solder joint can be faulty, either due to an open condition or a short condition. Thus, the single-stuck-at model is modified to cover both cases, resulting in the fault model detailed in Table 3.

Table 3. Defined Solder-Joint Fault Model

NOTATION	FAULT NAME	DESCRIPTION
ss/L	Solder-short/low	Entire associated node stuck low
ss/H	Solder-short/high	Entire associated node stuck high
so/L	Solder-open/low	Pin is stuck low, independent of associated node
so/H	Solder-open/high	Pin is stuck high, independent of associated node

6. Test Methodologies

Two categories of test are typically considered for manufacturing use:

1. Dynamic functional tests: tests defined in association with a functional and/or performance fault model. These test for faults, such as delay faults, that are associated with the performance of the system and are intended to demonstrate the suitability of the finished module to its intended function.
2. Static structural tests: tests defined in association with a structural fault model. These methods test for gross interconnectivity issues. In-circuit test (ICT) is an example of a static structural test method. The solder-open/short faults of Table 3 would be susceptible to such methods.

While the need for dynamic functional test is taken as a given, such analysis is beyond the scope of this paper. Such testing may in fact be required to detect certain classes of solder-open faults, such as those associated with bypass capacitors. However, the capability of such testing to diagnose or even detect structural defects is generally suspect. Therefore, the remaining analysis will focus exclusively on structural test goals.

7. Card-Edge Test (Module Without DFT)

As the subject module was designed solely for the purpose of demonstrating electrical performance characteristics of a buffered SDRAM DIMM, it was designed without any consideration for testability. Without such DFT, observability and controllability are limited to the primary (card edge) input/outputs (I/Os) of the module. This implies that for faults to be detected, such faults must be sensitized from the card-edge inputs and propagated through the entire module to the card-edge outputs. Diagnosis (isolation and location) of faults poses even greater difficulties, as many faults will produce the same syndrome at the primary I/Os.

The various fault syndromes resulting from modeled faults at each class of module solder joint are classified in columns 6–9 of Table 2 and defined in Table 4. The latter table also details the number of patterns and/or read/write cycles to be applied, along with a brief description of algorithms and consequent diagnostic resolution.

As shown in this analysis, many solder-joint faults produce common syndromes resulting in poor diagnostic resolution for structural faults when only card-edge access is provided.

Table 4. Card-Edge Test Fault Classification

FAULT CLASS	DESCRIPTION	NUMBER PATTERNS FOR DETECTION/ISOLATION; (ALGORITHM)	DIAGNOSTIC RESOLUTION	
			NO. COMPONENTS	NO. SOLDER JOINTS
fA	All-chip addressing fault	2 *((N+1)w + (N+1)r) = 26w + 26r; (write to all-0 addr and to all addr with only 1 logic-1 bit – read same; repeat for all-1 addr and all addr with only 1 logic-0 bit)	19	20
fA'	Single-chip addressing fault	"	1	1
fQ	Bank access-hold fault	1wb + 1rb; (CKE low during read burst for access hold)	10	11
fQ'	Single-chip access-hold fault	"	1	1
fR	All-chip access-mask fault	1wb + 1rb; (DQM high during read/write burst for data mask)	19	20
fR'	Single-chip access-mask fault	"	1	1
fS	Presence detect enable/disable fault	2; (PDE low/high)	1	1
fT	Identification output fault	1; (static output)	1	2
fU	IN/OUT fault	4; (IN low/high, OUT low/high)	1	2
fV	Dual-chip data fault	2 * 2*72(1w + 1r) = 288w + 288r; (walking-1 each bank, walking-0 each bank)	3	4
fV'	Single-chip data fault	"	1	1
fW	Presence detect output fault(1)	1; (static output)	2	4
fW'	Presence detect output fault(2)	1; (static output)	1	1
fX	All-chip gross access fault	1w + 1r; (any valid write /read access with any addr/data)	20	69
fX'	Bank gross access fault	"	10	22
fX''	Dual-chip gross access fault	"	2	3
fX'''	Single-chip gross access fault	"	1	7
fY	Clock multiply fault	2*(1wb + 1rb); (1 wb/rb to bank0, 1 wb/rb to bank1)	1	1
fZ	Clock PLL-bypass fault	1w + 1r; (at freq. which will not result in phase-lock)	1	1

8. Module DFT

Design-for-test techniques are generally based on providing greater access to the module under test for the purpose of improving the degree to which the module function can be observed and controlled. Another way of looking at DFT is that it seeks to partition the larger module function into smaller functions that are easier to test. Several techniques for this are in common use today. The two that are considered in this paper are in-circuit test (ICT) and boundary scan.

9. In-Circuit Test

ICT is based on providing physical access to probe as many module nodes as possible and on *ad-hoc* circuit techniques that allow internal nodes to be safely controlled (as well as observed) by an external tester. The resulting test fixture is commonly called a "bed of nails" (or in the case of double-sided assembly such as the subject module, a "clam shell") and the required tester consists of a large number of high-drive parallel test channels.

Generally, on fine-pitch SMT assemblies such as the subject module, provision for ICT requires placement of "test points" on which ICT probes may land. In some cases, the vias that are anyway present to route signals from outer layers to other layers may provide such test points. In other cases, vias must be added to bring signals to be accessed up from inner layer to outer layer.

Such placement of test points requires use of module “real estate” that may not be available. Generally, the finest available ICT probes (50-mil pitch) require test pads of 25 mils minimum width.

While modifications to the module layout have not been specifically implemented, the module layout has been analyzed for placement of physical test points. The results by node are presented in column 11 of Table 2 according to the accessibility classes defined in Table 5.

Table 5. In-Circuit Test Accessibility Classification

ACCESSIBILITY CLASS	DESCRIPTION
a	Accessible from module edge
b	Test points easily provided
c	Test points provided with difficulty
d	Test points difficult/impossible to provide
x	Accessible from module edge (Vcc/GND)

With test points provided at all internal nodes, the module is quite controllable at the IC level. Since all ICs on the module provide means for placing their outputs at high impedance, the tester can safely disable any ICs that are not under test. The only provision that would be required for this is to add pull-down resistors at register and clock driver output-enable pins versus the direct tie to GND that is specified for the original module.

Based on the presumed insertion of test points at all internal nodes except those in accessibility class d (quantity 31), full coverage and diagnostic of solder shorts are provided. The nodes excluded are indirectly accessible via shunt or resistor, and so their exclusion may somewhat reduce fault diagnostic, but not coverage. In case of solder opens, the consequent fault syndromes resulting at each class of module solder joint are classified in column 10 of Table 2 and are defined in Table 6. The latter table also indicates the consequent diagnostic resolution.

Table 6. In-Circuit Test Fault Classification

FAULT CLASS	DESCRIPTION	DIAGNOSTIC RESOLUTION	
		NO. COMPONENTS	NO. SOLDER JOINTS
iA’	Single-Chip Addressing Fault	1	1
iB	Buffer Data Fault	1	2
iB’	Buffer Data Fault (no access)	2	3
iC	Gross Clock Output Fault	1	2
iC’	Single Clock Output Fault	1	1
iD	Register Clock Fault	1	2
iS	Output Enable Fault	1	1
iT	Shunt/Resistor Fault	1	2
iV	Memory Data Fault	2	3
iX”’	Single-Chip Gross Access Fault	1	7
iY	Clock Multiply Fault	1	1
iZ	Clock PLL-Bypass Fault	1	1

As shown, the diagnostic resolution is remarkably improved (versus card-edge test), such that all single solder-stuck faults are generally diagnosable to the component and often to the pin level. Such a diagnostic provides the information necessary to improve process and repair failed boards for subsequent shipment.

10. Boundary-Scan Test

Like ICT, boundary-scan test (BST), as standardized in IEEE Std 1149.1 (JTAG), is based on providing test access to as many module internal nodes as possible. Unlike ICT, boundary scan provides access by integrating digital test cells behind the pins of compliant ICs. Access to such boundary-scan cells for control and observation of the module is provided by a 4-wire test access port (TAP) at each compliant IC. Thus, the complex and expensive fixturing and automated test equipment (ATE) required for ICT is avoided.

10.1 Boundary Scan at Register and Clock Driver

Of the 31 internal nodes that are presumed to be ICT accessible, 21 are associated with the register (ALVCH162721) while 10 are associated with the clock driver (CDC2586). Therefore, if the register and clock driver were replaced with suitably equivalent ICs with boundary scan, all ICT-covered nodes would be boundary-scan accessible, and thus, ICT could be eliminated without any consequent loss of fault coverage or diagnostic.

Such equivalents or near equivalents to the ALVCH162721 are, or will be, available soon (such as LVTH182504A and/or ALVCH182504, at an estimated additional cost of $5). Unfortunately, the authors are unaware of any clock drivers available or planned with boundary scan. If these were available (at an estimated additional cost of $3), then boundary scan would displace ICT, while requiring off-edge physical access only to the four TAP signals and using much less expensive ATE – all at an additional component cost that is barely 1% of the total cost of module materials.

10.2 Boundary Scan at Register Only

Even with boundary scan available only in the register, controllability and observability of the SDRAM ICs is provided, with the exception of the clock signals. Observability of one output of the clock driver is also provided. Therefore, if access to the TEST input of the CDC2586 were provided, the low-cost boundary-scan tester could source the module CLKIN signal so that it would be coordinated with boundary-scan operations to perform read/write cycles to the SDRAM array. By doing so, all interconnects to the SDRAMs can be tested with the same fault coverage and diagnostic capability provided by ICT. Access to only five off-edge signals is required (four TAP signals, plus the CDC2586 TEST input).

10.3 Boundary Scan at SDRAM ICs

Boundary scan in the SDRAMs would greatly impact the overall controllability/observability of the module such that diagnostic resolution would be improved over that provided by ICT. For example, where faults of class iX''' (single-chip gross access fault) occur in ICT, the boundary-scan facility on the SDRAM would be able to distinguish which of seven pins on the device were open.

At this time, the authors are unaware of any available or planned offerings of SDRAMs with boundary scan. However, due to the large ratio of die size to I/O pins of such ICs, it is estimated that the silicon overhead for providing boundary-scan should be less than 5%. It is hoped that memory IC vendors will realize the benefit of scan-test techniques, not only for board/manufacturing test, but also to access built-in test capabilities of such ICs.

10.4 Boundary Scan at Buffer

As it has a very simple function on the module (drive static outputs), the octal buffer is the last device to warrant consideration for boundary scan. Still, the additional cost (estimated at $2) required to procure equivalent buffers with boundary scan would be minimal.

10.5 Boundary Scan: Beyond Manufacturing Test

A real advantage that boundary scan holds over any other manufacturing test or DFT approach is that it is built into the ICs and, thus, the module, and so is available for use when ATE is not. For example, it can be used for module test during burn-in or under other conditions where the module is not accessible by ATE. Additionally, if appropriate system-level access to boundary scan is provided, it can be used for in-system test, diagnostics, configuration, programming, emulation, etc.

11. Comparative Study

Several metrics have been used to grade the different structural test methodologies outlined. A tabulation of the performance of the various test methodologies versus these metrics is given in Table 7.

Table 7. Comparison of Test Methodologies

METRIC	CARD-EDGE	ICT	BST
Fault coverage	95%+	95%+	95%+
Fault diagnostic	4 sol. joints	2 sol. joints	2 sol. joints
Vector development	100 per-hr	30 per-hr	15 per-hr
Test pattern size	1 Mb	100 kb	20 kb
Test time	0.1 s	0.1 s	0.1 s
Tester cost	$200k	$400k	$40k

Fault coverage is the estimated percentage of faults that will be detected. Since the subject module is fairly simple structurally, it is expected that all test methods will obtain a high level of coverage.

Fault-diagnostic capability is expressed as a weighted average of resolution in terms of solder joints. Excellent results from ICT and BST are typical, while the result for card-edge test belies the simple function of this module.

Vector development effort is measured in terms of the estimated number of person-hours required to complete the test set. Boundary-scan test development is highly automated, while ICT is somewhat less so. On the other hand, card-edge test development tends to be manual.

Test-pattern size is expressed in bits. With full BST, the vector set is on the order of $\log_2$ (number of module nodes). ICT vector sets will be somewhat longer, while card-edge vector sets can be very lengthy, in order to obtain desired fault coverage and diagnostic resolution.

Test time is a factor of the number of vectors and the vector application time. BST uses a low vector bit rate, but due to the small number of vectors, performs quite adequately. ICT and card-edge testers can use much higher vector bit rates.

Tester cost is estimated and is a function of performance (vector bit rate), number of test channels, etc. The small number of channels required for BST and modest performance requirements result in very inexpensive test systems.

12. Conclusion

Considering the metrics and discussion provided in the prior section, boundary-scan test is clearly a winning manufacturing test strategy, even for a module of modest functional complexity. Add to this the ability to reuse boundary scan during burn-in, and more importantly in fielded systems, and a small investment in additional component cost for boundary scan will reap dividends many times over throughout the product's life cycle.

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