Application Report

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Biasing Requirements for TXS, TXB, and LSF Auto-Bidirectional Translators

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ABSTRACT

The TXS and LSF families of translators differ from the TXB translator family, because the outputs of the TXS and LSF families are not driven by buffers. Instead, the TXS and LSF families use internal or external pullup resistors to drive logic high, and an internal pass transistor that lets the host device drive logic low. This application report discusses the specific requirements of bidirectional translators for a minimum voltage separation between V_{CCA} and V_{CCB}. For TXS and TXB-type translators, V_{CCA} must be less than or equal to V_{CCB}. For translators from the LSF family, V_{ref_A} must be at least 0.8 V less than V_{ref_B}. This application report also examines the reason for these requirements and the implications when they are violated.

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1.1 V_{CCA} and V_{CCB} Separation of TXS and TXB-Type Translators

The internal architecture of the TXS family of translators contains a pass transistor, internal pullup resistors on both the I/O ports, and One-shot edge accelerator circuitry. Figure 1 shows a simplified diagram of this internal architecture. For more information, see the A Guide to Voltage Translation With TXS-Type Translators application report.

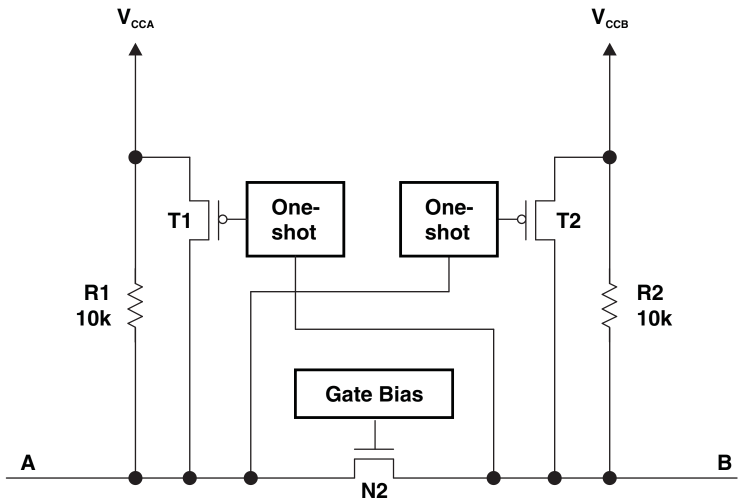

Figure 1. Simplified TXS Architecture

The TXB family of translators has a weak, buffered architecture with one-shot edge accelerator circuitry to improve the data rate. The devices can translate the CMOS push-pull logic, however, they are not suitable for open-drain signals.

Figure 2 shows a simplified diagram of this internal architecture. For more information, see the A Guide to Voltage Translation With TXB-Type Translators application report.

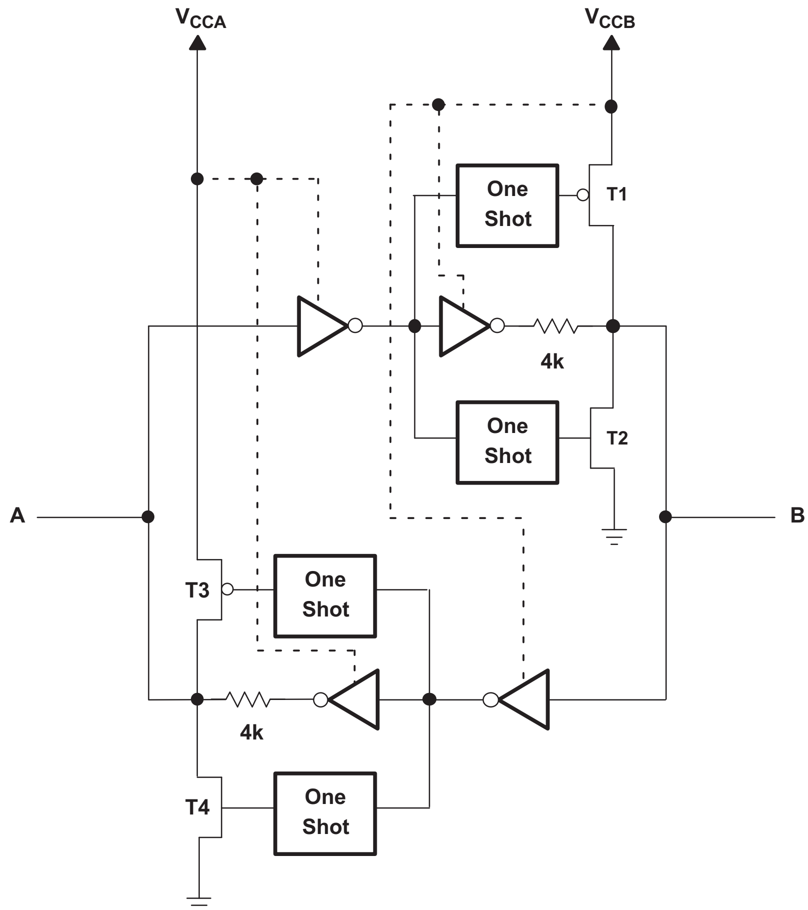

Figure 2. Simplified TXB010X Architecture

TXS and TXB-type translators require that V_{CCA} is less than or equal to V_{CCB}. This is due to an internal protection diode that can become forward biased when the voltage on V_{CCA} exceeds the voltage on V_{CCB}. When this occurs, large amounts of current flows through V_{CCA} and into the diode, increasing power consumption and potentially damaging the device. Figure 3 shows the test setup.

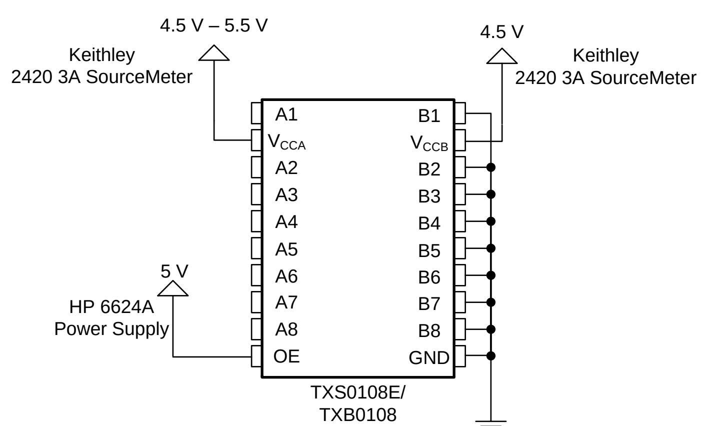

Figure 3. TXS and TXB V_{CCA} and V_{CCB} Separation Test Setup

V_{CCA} and V_{CCB} were supplied and measured through Keithley 2420 3-A source meters, with V_{CCB} fixed at 2.5 V and V_{CCA} swept from 2.5 V to 3.5 V. Figure 4, Figure 5, and Figure 6 show the resulting current through the supply pins.

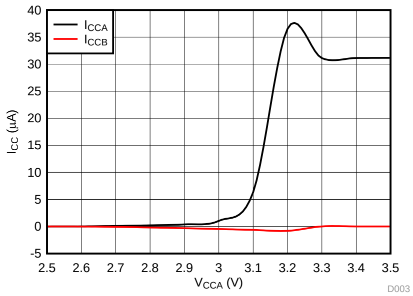

Figure 4. TXS0101 V_{CCA} > V_{CCB} Leakage

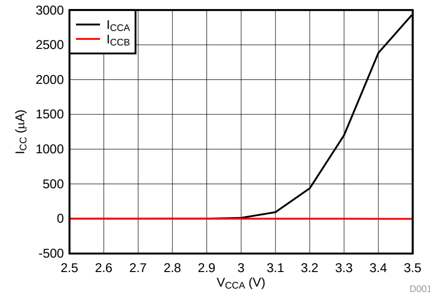

Figure 5. TXS0108E V_{CCA} > V_{CCB} Leakage

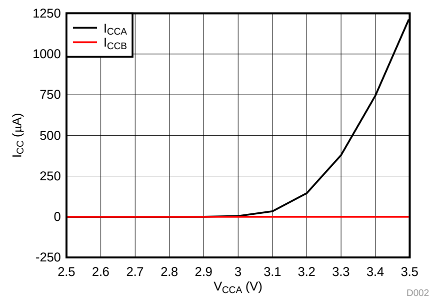

Figure 6. TXB0108 V_{CCA} > V_{CCB} Leakage

As shown in Figure 4, Figure 5, and Figure 6, when the voltage on V_{CCA} exceeds the voltage on V_{CCB} by roughly 0.6 V, the diode begins to conduct and the I_{CCA} current begins to drastically increase as V_{CCA} increases.

1.1.1 Summary: Bias Requirements for TXS and TXB Translators

TXS and TXB translators require that V_{CCA} be less than or equal to V_{CCB}. When this requirement is violated, there is potential for the internal protection diode to become forward biased, resulting in increased current consumption and potential damage to the device. When using separate power supplies for V_{CCA} and V_{CCB}, special care must be taken if V_{CCA} and V_{CCB} will operate at the same voltage node. The system designer must ensure that power supply tolerances will not result in a potential difference between V_{CCA} and V_{CCB} large enough to bias the internal protection diode.

1.2 V_{ref_A} and V_{ref_B} Bias for LSF Type Translators

For translators from the LSF family, TI recommends that V_{ref_A} is at least 0.8 V lower than V_{ref_B}. Figure 7 shows a simplified diagram of the LSF architecture. See the *Voltage Translation With the LSF Family* application report, and watch the LSF Logic Minute videos to understand the LSF device operation and it's applications.

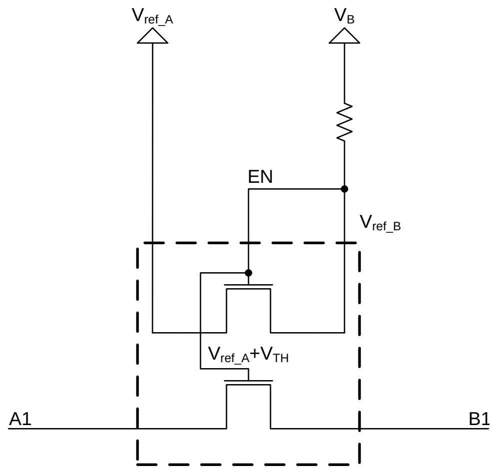

Figure 7. LSF010x Simplified Architecture

As shown in Figure 7, the LSF010x device contains a reference FET between V_{ref_A} and V_{ref_B}, as well as a pass FET on each channel. The reference FET is designed to set the gate bias voltage of each pass transistor equal to Equation 1.

$$V_{ref\_A} + V_{TH} \quad (1)$$

When the proper bias of Equation 2 is maintained, the reference FET conducts, allowing V_B to pull the voltage at EN to that of Equation 1, and setting the gate voltage on the pass transistor of the channel to that of Equation 1. The result is that the output port clamps at Equation 3.

$$V_{ref\_A} \le V_{ref\_B} - 0.8\ V \quad (2)$$

$$V_{ref\_A} + V_{TH} - V_{TH} = V_{ref\_A} \quad (3)$$

When the proper bias between V_{ref_A} and V_{ref_B} is not maintained, the gate bias of the pass transistor can no longer be accurately predicted and the voltage at which the pass transistor turns off is no longer known. By maintaining the proper bias between V_{ref_A} and V_{ref_B}, the system designer can accurately set the gate voltage of the pass transistor, allowing for predictable down-translation from the B-port to the A-port without the use of external pullup resistors.

As an example, the LSF0108 device was tested with V_{ref_A} = V_{ref_B} = 3.3 V. A 25-MHz, 3.3-V square wave was applied to B1 (blue) and the output was measured at A1 (green). Figure 8 shows the resulting waveform.

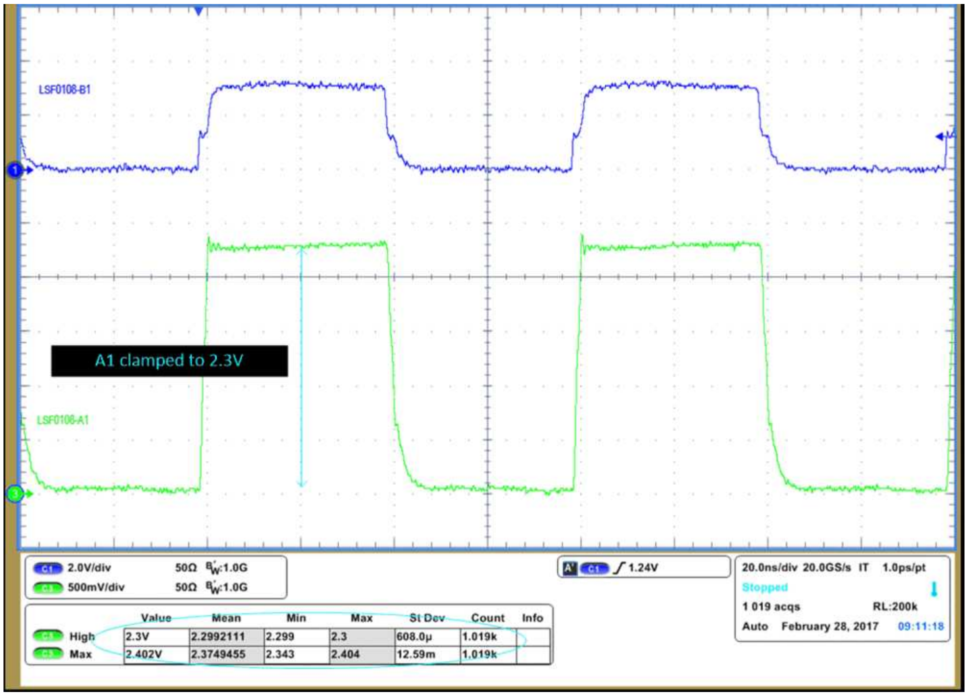

Figure 8. LSF010x Voltage Clamping

When the 3.3 V signal is applied to B1, the output A1 clamps at 2.3 V even though V_{ref_A} is set to 3.3 V. When the bias between V_{ref_A} and V_{ref_B} is not maintained, the system designer can no longer accurately set the gate voltage of the pass transistor. Therefore, the system designer can no longer accurately predict the voltage at which the pass transistor stops conducting. This can result in reduced flexibility and reduced signal integrity.

1.2.1 Bias Requirements Summary for LSF Translators

When the proper bias between V_{ref_A} and V_{ref_B} is not maintained, the gate bias of the pass transistor can no longer be accurately predicted, and the voltage at which the pass transistor turns off can no longer be known. By maintaining the proper bias between V_{ref_A} and V_{ref_B}, the system designer can accurately set gate voltage of the pass transistor, allowing for predictable down-translation from the B-port to the A-port without the use of external pullup resistors.

2 References

- Texas Instruments, Basics of Voltage-Level Translation, application report
- Texas Instruments, Voltage Translation With the LSF Family, application report
- Texas Instruments, A Guide to Voltage Translation With TXB-Type Translators, application report
- Texas Instruments, A Guide to Voltage Translation With TXS-Type Translators, application report
- Texas Instruments, Effects of External Pullup and Pulldown Resistors on TXS and TXB Devices, application report

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