

A Guide to Voltage Translation With TXS-Type Translators

Dave Moon, Aeysha Sultana
High Volume Linear

ABSTRACT

Modern trends are driving the need for lower supply voltages across many system-level designs. As most processor voltage levels continue to decrease in the interest of achieving the lowest possible power consumption, peripheral devices maintain a need for higher voltage levels, creating potential for voltage discontinuities within a system. To remedy this mixed voltage system incompatibility, a voltage translator can be used.

Texas Instruments High Volume Linear group offers a wide-range of voltage level translators. A variety of architectures provide solutions for different application environments including dual-supply direction-controlled, auto-direction sensing, and application-specific memory card interface translators.

The information in this application report is intended to help system designers understand the architecture and operation of the TXS-type auto-direction sensing translator family

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1 The Need For Voltage-Level Translation

The need for voltage level translation is becoming increasingly significant in today's electronic systems. As the digital switching level standards have continued to progress toward lower voltage levels, system incompatibilities have arisen. Figure 1 illustrates the trend toward lower system voltage levels and demonstrates the incompatibilities that mixed voltage systems can face.

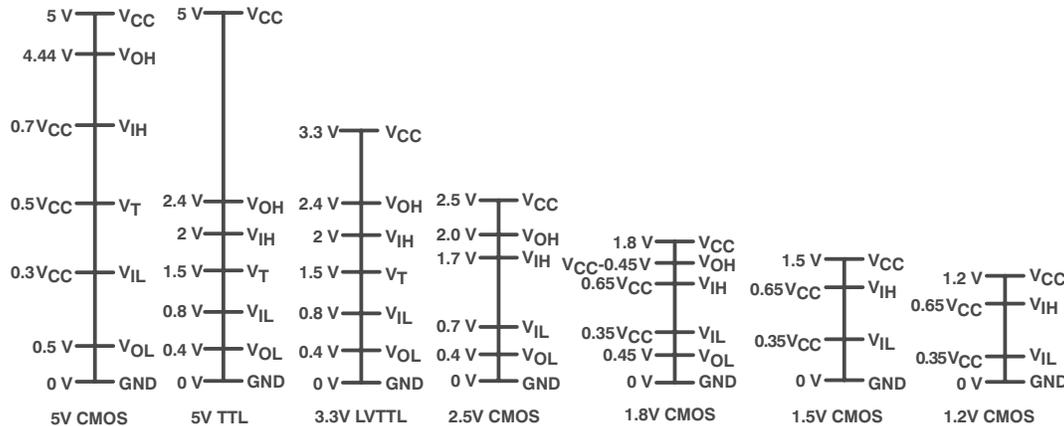


Figure 1. Digital Switching Levels

For two devices to interface reliably, the output driver voltages must be compatible with receiver input thresholds. For this condition to be met in mixed voltage systems, a voltage translator is often required.

Texas Instruments offers several unique device architectures for addressing voltage translation needs. The most familiar to system designers is probably a direction-controlled buffer translator, such as the SN74AVC8T245. These translators can help remedy many problems in system voltage compatibility but require DIR (direction) control pins. If the system environment does not provide a programmable GPIO to control the direction pin, an auto-direction sensing translator architecture can provide an alternative translation solution.

2 Auto-Direction Sensing Voltage Translator Architecture

If a processor GPIO input direction-control signal is not available or if one is not desired, an auto-direction sensing voltage translator can provide a robust solution. As the name implies, this type of translator does not require the use of a direction control signal, and each channel supports independent transmission or reception of data. This eliminates the need for a processor GPIO to control a DIR input, resulting in simplified software driver development as well as smaller device packaging due to reduced pin count.

The two types of auto-direction sensing voltage translator architectures are TXB buffered-type and TXS switch-type. Neither type of architecture requires a DIR control signal to establish the direction of data flow. The TXB translators are designed to exclusively be connected and interfaced with a push-pull drivers and are capable of driving a light capacitive or high impedance loads in applications such as Secure Digital (SD) or Serial Peripheral Interface (SPI). See the TI application report, *A Guide to Voltage Translation With TXB-Type Translators* ([SCEA043](#)) for more information on the TXB-type voltage translators.

Texas Instruments has developed several types of TXS-type (where the "S" indicates switch-type) translators that are designed to interface with open-drain drivers and can be used in applications such as I²C.

2.1 Initial Series of TXS Type Devices

The initial series of TXS type devices are the TXS0101, TXS0102, and TXS0104E. The basic block diagram architecture of a single-bit (or channel) is shown in Figure 2.

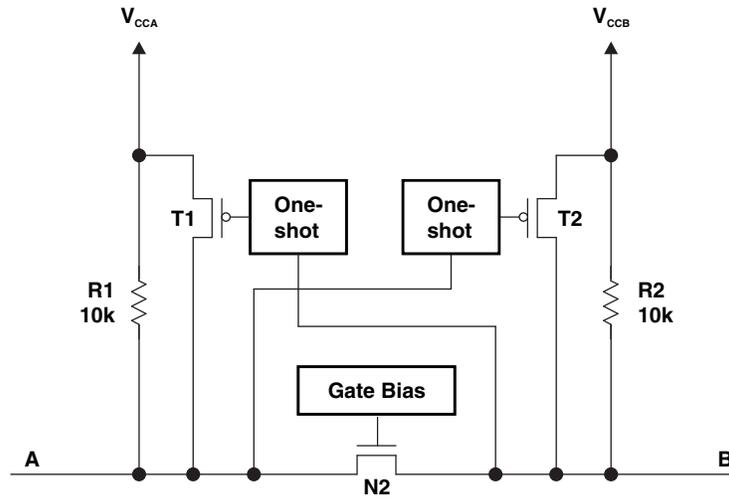


Figure 2. Basic TXS0101, TXS0102, and TXS0104 Architecture

These TXS translators are FET-based architectures that utilize an N-channel pass-gate transistor to open and close the connection between the A-port and B-port. When a driver connected to A or B port is low, the opposite port is, in turn, pulled low by the N2 pass-gate transistor. This pass-transistor type voltage translator is ideal for down-translation and over-voltage protection.

Figure 3 shows the transfer characteristics of the N2 pass-gate transistor, where the threshold voltage (V_T) is approximately 1 V and the gate bias voltage (V_{GATE}) is as shown.

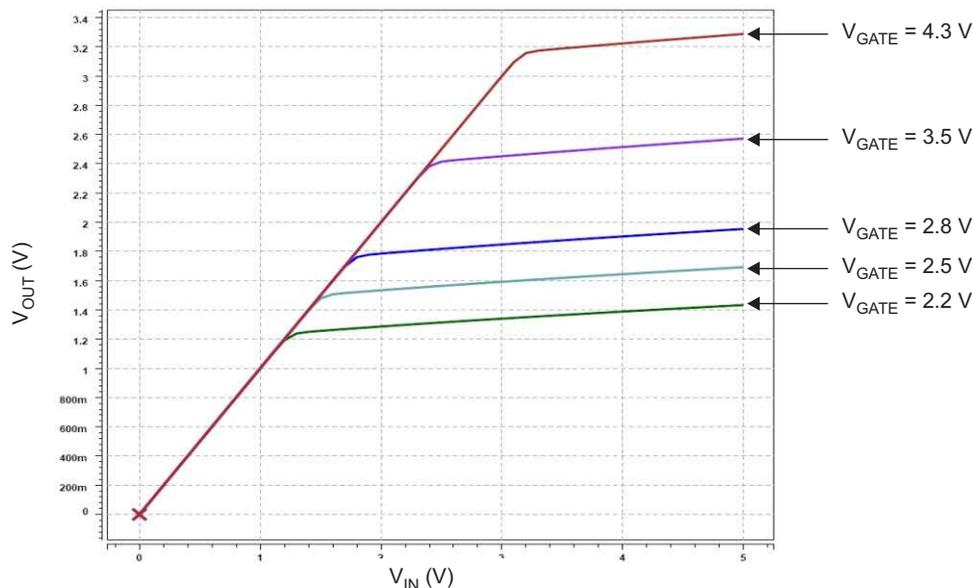


Figure 3. Transfer Characteristics of an N-Channel Transistor

The pass-gate transistor, N2, is on when $V_{GS} > V_T$. Consider first the case where one side of N2 is held low by an external driver. With the input to N2 at 0V, N2 will be “On” and the output of N2 will be held to nearly 0V due to the on-state resistance of N2. As can be seen in Figure 3, as the input voltage rises due to a rising edge, the output voltage of N2 will track the input until N2 turns off at $V_{GATE} - V_T$. After N2 stops conducting, the input and output ports will continue to rise to their respective supply voltages due to

the internal pull-up resistors on either port. Secondly, consider the case where both ports start out high. The ports will be held at static high levels due to the internal pull-up resistors. When the input port is pulled low by an external driver, N2 will begin to conduct once $V_{GS} > V_T$. As N2 starts to conduct the output will begin to track the input port following the curve in the [Figure 3](#). The sinking-current required to perform this translation function must be provided by an external system driver that is connected to either the A or B ports.

These pass-transistor voltage translators and their voltage clamping feature makes TXS type translators an ideal choice for applications requiring over-voltage protection and addition to voltage level translation. The signal propagation delay through the N2 transistor is extremely fast making it an elegant solution.

To achieve faster data rates through the device, these translators include rising edge-rate acceleration circuitry to provide stronger ac-drive by bypassing these integrated 10-k Ω pull-up resistors through a low impedance path during low-to-high signal transitions. A one-shot (O.S.) circuit with an associated T1/T2 PMOS transistors is used to increase switching speeds for the rising-edge input signals. When a rising edge is detected by the O.S. circuit, the T1/T2 PMOS transistors turn on momentarily to rapidly drive the port high, effectively lowering the output impedance seen on that port and speeding up rising edge inputs.

The combination of an N-channel pass FET, integrated 10-k Ω pull-up resistors, and edge-rate acceleration circuits makes the TXS type translators ideal for interfacing devices or systems operating at disparate voltage levels while also allowing for simple interfacing with open-drain (O.D.) as is required in I²C, 1-wire, and MMC-card interface applications.

The TXS0101, TXS0102, and TXS0104E translators also incorporate integrated pull-up resistors and higher level ESD protection which saves board space and overall BOM cost. TXS-type translators can support push-pull driving applications, and have the ability to drive slightly heavier Impedance loads than the TXB-type translators. However, the TXB-type translators may prove to be a better solution if the capacitive loading is <70pF.

2.2 Second Series of TXS Type Devices

The second series switch-type translator is the TXS0108E semi-buffered type architecture and is targeted for higher speed applications. The basic block diagram of a single-bit (or channel) of this "semi-buffered" translator is shown in [Figure 4](#).

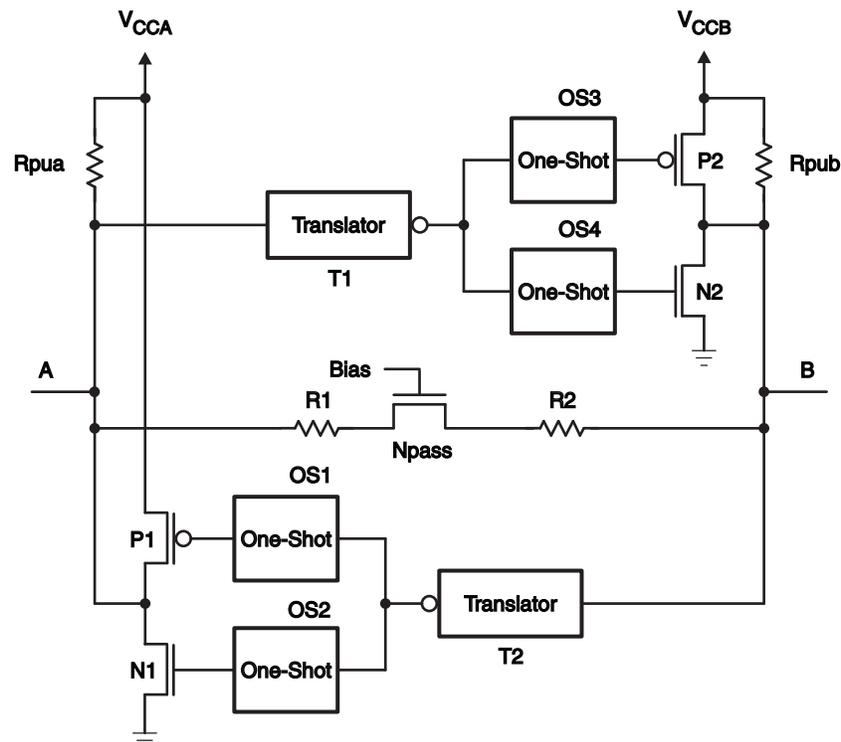


Figure 4. Basic TXS0108E Architecture

The design goals for this type of translator were to achieve faster data rates while also providing support for applications where a channel needs to start out in a low-speed open-drain (O.D.) mode, but eventually transition over to a higher-speed push-pull mode. MMC memory card applications are an example of this type of operating mode. The TXS0108E translator reliably supports high-speed data rates in excess of 60 Mbps, whereas the initial TXS series type translators supported slightly less than half this. The ability to translate down to the 1.2V operating-node is also supported in the TXS0108E device.

To achieve these faster data rates, both rising-edge and falling-edge rate acceleration circuitry is incorporated for symmetrical ac-drive. Again, these accelerators bypass the integrated pull-up resistors during low-to-high and high-to-low signal transitions and speed up the output slew rate after monitoring A and B port input rising and falling edges for signal transitions. Figure 4 shows the O.S. circuit and its associated P1/P2 PMOS transistor which are used to improve switching speeds for the rising edge signal by lowering the output impedance seen on that port and speeding up the rising edge rate.

Figure 5 shows a low-to-high transition.

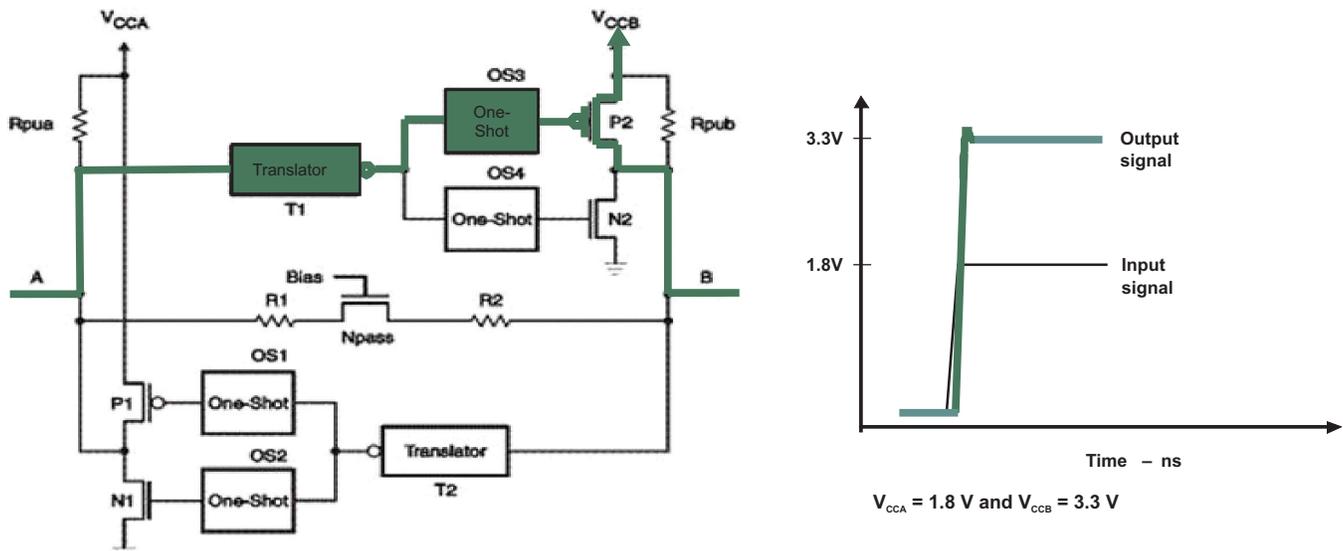


Figure 5. TXS0108E During Low-to-High Signal Transition

The translator's T1, OS3 and P2 element paths are activated when a low-to-high signal is applied at the A port. The OS3 edge-rate accelerator facilitates the fast ramping of low-to-high transition of the signal at the output. The pull-up resistors R_{pua} and R_{pub} provide dc-bias to hold the opposite port high when one of the ports is being driven high. During this acceleration phase, the output resistance of the driver is decreased to approximately $50\ \Omega$ - $70\ \Omega$ to increase the current drive capability of the device.

Figure 6 shows a high-to-low transition:

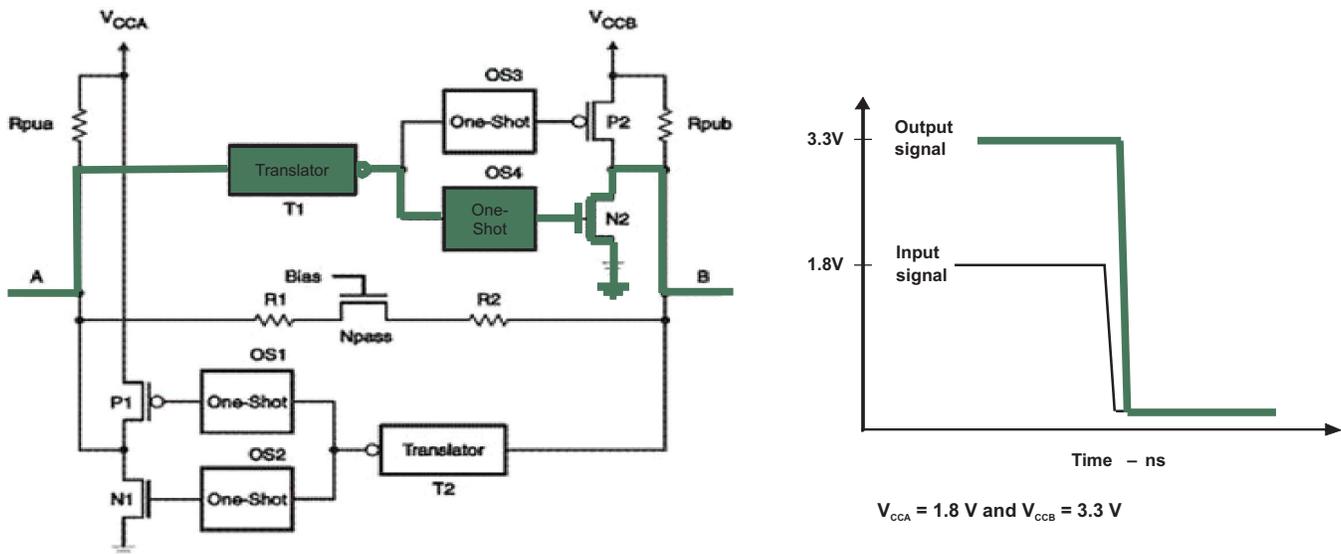


Figure 6. TXS0108E During High-to-Low Signal Transition

The translator's T1, OS4 and N2 element paths are activated when a high-to-low signal is applied at the A port. The OS4 edge-rate accelerator facilitates the fast ramping of high-to-low transition of the signal at the output. The N-channel pass-gate transistor and resistors R1 and R2 provide a dc path between ports A and B. They also provide dc-bias to hold the opposite port low when one of the ports is driven low.

The TXS0101/2/4 translators have fixed 10-k Ω value pull-up resistors which provide dc-bias and dc current sourcing/drive capabilities to maintain a high. A key feature that was included in the TXS0108E translator to allow it to operate better in SDIO applications is the use of "smart" pull-up resistors. This feature provides lower static power consumption (when the I/Os are passing a low), supports lower VOL values for the same size pass-gate transistor, and helps improve simultaneous switching performance. These smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line, as follows:

- R_{PUa} and R_{PUb} values are 4 k Ω when the output is driving a high.
- R_{PUa} and R_{PUb} values are 40 k Ω when the output is driving a low.
- The I/O goes into High-Z when the device is disabled via the OE pin or by pulling the either V_{CCA} or V_{CCB} to 0 V.

The series resistance values of R1 and R2 are 150 Ω (typical). The V_{GATE} gate bias voltage of the N-channel pass transistor is again set to a level that optimizes the switch characteristics for maximum data rate as well as minimal static supply leakage.

3 Input Driver Requirements With TXS-Type Translators

The continuous dc-current "sinking" capability is determined by the external system-level driver interfaced to the TXS-type translator. For high bandwidth bidirectional SDIO circuit applications, the I/O port needs to quickly change from an input to an output and vice-versa. Therefore, a modest dc-current "sourcing" capability of 100 to 200 micro-Amps is needed and the smart pullup resistor values determine the sinking capability. The fall time (t_{fA} , t_{fB}) of a signal depends on the edge rate and output impedance of the external device driving these SDIO lines as well as the capacitive loading on these lines. Similarly, the t_{pd} and max data rates also depend on the output impedance of the external driver. The values for t_{fA} , t_{fB} , t_{pd} , and maximum data rates specified in the TXS data sheets assume that the output impedance of the external driver is less than 50 Ω .

4 Driving External Loads With TXS-Type Translators

The TXS-type translators were architected for driving high-impedance loads. As such, the O.S. duration has been set to best optimize trade-offs between dynamic current consumption (I_{CC}), load driving capability, and maximum bit-rate considerations. Careful Printed-Circuit-Board (PCB) layout practices with short trace lengths should be followed to avoid excessive capacitive loading. Ensuring proper O.S. triggering will avoid bus contention, output signal oscillations, and other adverse system-level affects. To accomplish this, PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the source driver. The O.S. circuits have been designed to stay on for 10 to 30 ns so the maximum capacitance of the lumped load that can be driven also depends reliably also depends directly on this one-shot duration.

There is a tradeoff between achieving a maximum data rate and driving heavy capacitive loads simultaneously. With heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. In this scenario, only the pull-up resistors will pull the line high in accordance with its RC time-constant determined by the resistive and capacitive loadings. It is best to avoid this condition by driving capacitive loads less than 70pF when maximum data rate are desired. With capacitive loading >70pF, the TXS-type devices will still successfully operate at lower data rates.

If the application requires an external pullup or pulldown resistor (R_{pu} or R_{pd}) special consideration must be given to the resistor value. It is important to choose a large enough R_{pu} or R_{pd} to ensure adequate V_{OH} and V_{OL} levels at the output port of the translator.

To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turn-off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the Timing Requirements section of this data sheet. Once the O.S. is triggered and switched off, both the A and B ports must go to the same state (i.e. both high or both low) for the one-shot to trigger again. In a dc state, the output drivers maintain a low state through the pass transistor.

5 Output Enable Control

The TXS devices offer low power consumption of 5 to 10 μA maximum I_{CC} when the output enable is high. When the output enable is low, the TXS translator buffer is disabled and the outputs are placed into high impedance state for increased power savings. The OE input circuit is referenced to the V_{CCA} power supply and when the device is disabled, the pullup resistors are disabled. In addition, current leakage on the A or B ports will be less than $\pm 1 \mu A$ when the outputs are disabled. If the application does not require output enable control then the OE pin should be tied to the V_{CCA} supply. Leaving OE floating in an indeterminate state can cause undesirable quiescent current to flow in the device which subsequently increases the overall power dissipation of the device.

The outputs are also disabled and put into a high-impedance state under partial power down conditions and this feature is referred to as a V_{CC} isolation feature. If $V_{CCB} = 0 V$, the A-port is disabled. Likewise, if $V_{CCA} = 0 V$, the B-port is disabled. For the TXS type translators that do not have IEC level ESD protection (i.e. ± 15 -kV Air-Gap and ± 8 -kV Contact discharge), they are fully specified for partial-power-down applications using the I_{OFF} feature. This I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when these devices are powered down.

6 Conclusion

The TXS translators offer system designers a good solution to remedy mixed-voltage system incompatibilities when interfacing with open-drain drivers in applications such as I²C. These translators eliminate the need for provisioning a GPIO of a processor, since they change the direction of the data flow automatically without the use of a direction control pin. This can simplify software driver development and allows for solutions in smaller packages because of this direction control pin savings.

Visit www.ti.com for data sheets for all bit-width TXS translators along with the full line of Texas Instruments voltage translators.

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