Application Report
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Basics of the CDC7005 Hold Function

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ABSTRACT

The CDC7005 is a high-performance clock synthesizer and jitter cleaner with implemented hold functionality. The hold functionality can be used for fail-safe operation if the reference clock is missing. This application report describes the basics, the advantages, and the limitations of the CDC7005 hold functionality. Additionally, a discrete realization of a simplified external hold function is shown. It is assumed that the reader is familiar with the basics of PLLs and the CDC7005. The CDC7005 can be used with an external VCXO or a VCO. In this document, VCXO means both VCXO and VCO.

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1 Introduction

The CDC7005 hold functionality is a fail-safe feature that keeps the frequency of the VCXO constant, after the reference clock (REF) is missing. Because the output frequency is an integer fraction of the VCXO frequency, the output frequency remains constant, too. Therefore, the frequency of the VCXO and the outputs are similar before and after the reference clock is missing and remains almost constant until the reference clock is back. The hold function can be enabled with bit 2 in word 2 of the internal register and disabled by default.

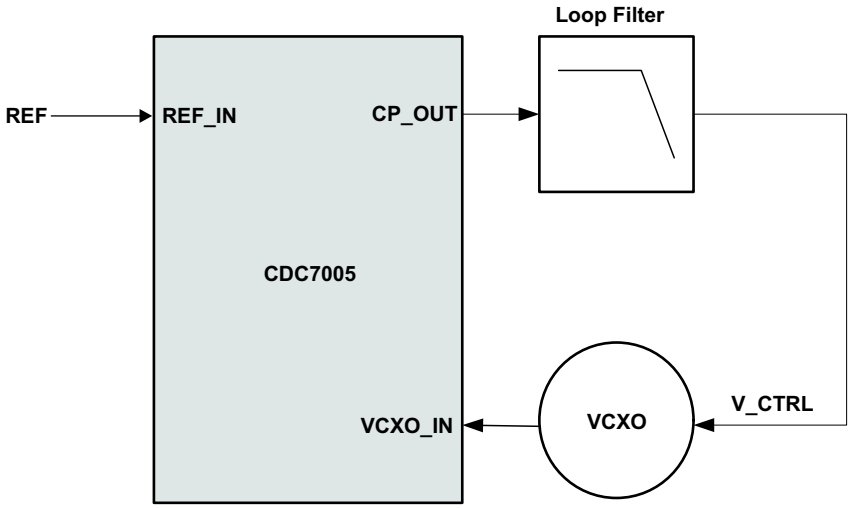

Figure 1. CDC7005 With Loop Filter and VCXO

Figure 1 shows a simplified block diagram of the CDC7005 PLL. The control voltage of the VCXO (V_CTRL) is typically around $V_{CC}/2$ if the PLL is locked. Assuming that the hold functionality is not activated, the output of the charge pump (CP_OUT) sets V_CTRL to 0 V within a short time, if the reference clock is missing. Therefore, the frequency of the VCXO is set to the minimum frequency (see Figure 2).

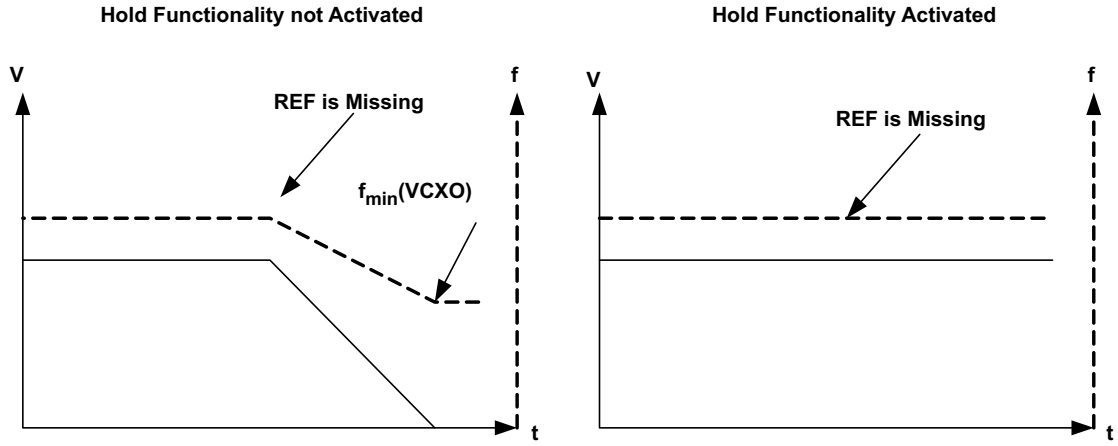

Figure 2. Behavior of the VCXO Control Voltage and Frequency After REF_IN is Missing

If the hold functionality is activated, the charge pump is placed in a 3-state condition, after the reference clock is missing. Therefore, the VCXO frequency remains almost equal.

2 Basics of the Hold Function

Figure 3 shows the state diagram of the CDC7005 hold function.

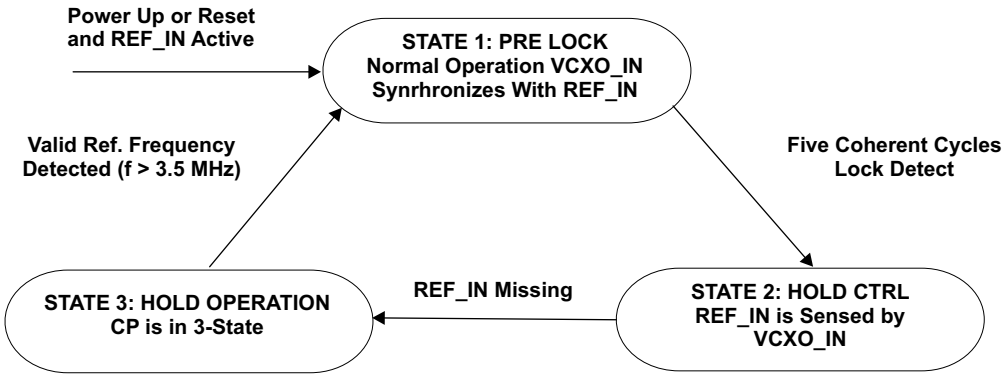

Figure 3. State Machine of the Hold Functionality

After power up, the state machine is in STATE 1. The charge pump is in normal operation, and the VCXO synchronizes with the reference clock (REF_IN). If the rising edge of the VCXO is inside the lock detect window for at least five successive cycles at the phase frequency detector (PFD), the PLL of the CDC7005 is considered to be in lock (see SCAS685 for more information). The hold functionality switches from STATE 1 to STATE 2, accordingly.

In STATE 2, the PLL is locked and in normal operation. A special reference detection circuit is used, which is faster than the circuit of STATUS_REF. This fast circuit is able to detect even a single missing reference cycle. The advantages and the limitations of this implementation are explained in more detail in the following section. If the reference clock is missing, the hold function switches to STATE 3.

In this state, the CP is in a 3-state condition to keep the control voltage of the VCXO constant. Therefore, the frequency of the VCXO and the frequency of the outputs remain almost equal to the frequency before the reference clock was missing.

After the reference clock is back, the hold function switches to STATE 1. A new PLL lock cycle is necessary before state machine switches to STATE 2.

3 Reference Detection Circuit

This section describes the reference detection circuit of the hold functionality. The circuit is located in front of the divider M and the divider N of the CDC7005. Locating the circuit before the dividers enables the hold function to detect a missing reference clock after the first missing cycle, but gives some limitations that depend on the duty cycle of the reference clock. Figure 4 shows the basic functionality.

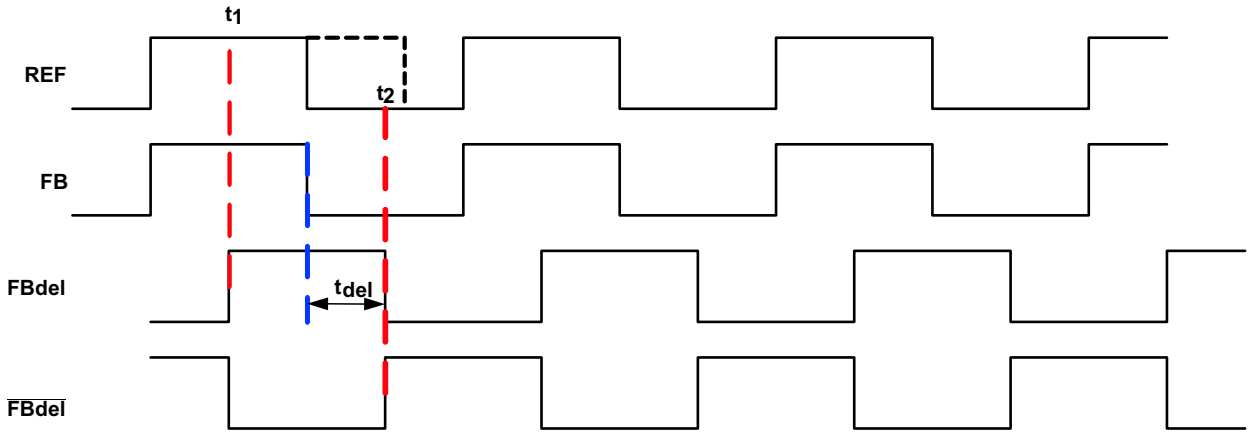

Figure 4. Reference Detection Circuit Timing Diagram

The following assumptions are necessary for the circuit explanation:

- The hold function is activated and the state machine is in STATE 2.
- The frequency of the reference clock (REF) and the VCXO (FB) must be equal before the divider M and the divider N, which means that both dividers have the same value.
- The PLL is in lock (phase difference between REF and FB is almost 0), and the reference detection circuit of the hold function is active.

To detect a missing reference cycle, the signals REF (reference clock) and FB (VCXO after P-Divider) are needed. FB is internally delayed and inverted, which is shown as FBdel and $\overline{\text{FBdel}}$. The level of the reference clock is checked at the rising edge of FBdel (REF(t1)) and the rising edge of $\overline{\text{FBdel}}$ (REF(t2)).

The reference detection circuit detects a valid reference clock, if REF(t1) is high and REF(t2) is low. The circuit detects a missing cycle, if REF(t1) and REF(t2) are both high or low and set the charge pump into a 3-state (STATE 3) condition.

The charge pump is in a 3-state condition after the first missing reference cycle. However, this reference detection circuit has some limitations.

The reference detection circuit can indicate that the reference clock is missing, even if this in not true. This happens, if the falling edge of the reference clock is after the rising edge of $\overline{\text{FBdel}}$ (dashed line). In this case, REF(t_1) and REF(t_2) are both high, but the reference clock has no missing cycle and is still valid. The charge pump is set into a 3-state condition and the PLL loses lock. However, STATUS_REF is still be high, because the reference clock is still applied to REF_IN. Therefore, the state machine will switch to STATE 1 and the PLL will start to lock again.

This behavior occurs, if the duty cycle is too large, because a large duty cycle can shift the falling edge of REF behind $\overline{\text{FBdel}}$. The hold function switches from STATE 2 to STATE 3 immediately after STATE 2 was reached. Therefore, no stable PLL lock is possible.

This becomes more critical if the reference frequency is low, because tdel is an absolute value which is typical about 4 ns. This means that a duty cycle of more than 56% is critical at 15.36 MHz and more than 72% at 30.72 MHz reference clock for the typical condition.

The following conditions must be applied to ensure a proper working of the missing reference detection circuit:

- Divider M and divider N need to have the same values.
- Fref_in max = 75 MHz
- Duty cycle of 45% to 55% for 25 MHz ≤ fref_in < 50 MHz
- Duty cycle of 40% to 60% for 50 MHz ≤ fref_in < 75 MHz
- Duty cycle of the VCXO should be in the 50% range.

4 Loop Filter Requirements

The loop filter is also important for a proper working of the hold function. Figure 5 shows a passive second-order loop filter with leakage currents through the capacitors.

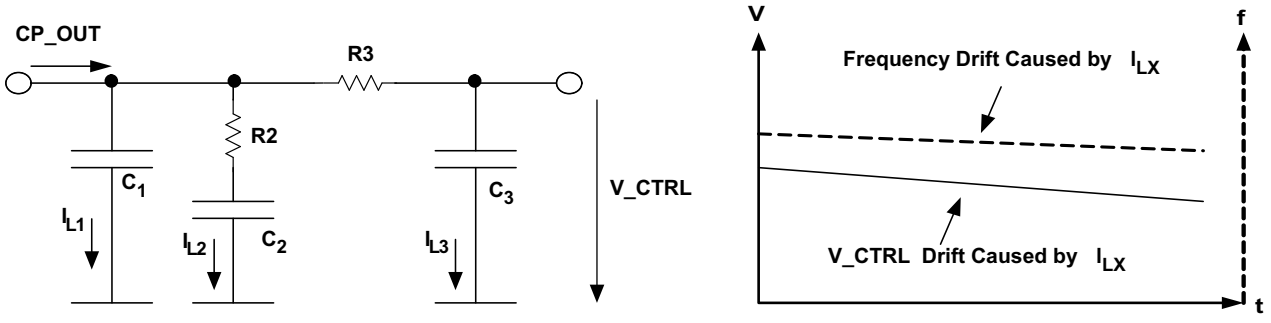

Figure 5. Loop Filter Leakage Currents

Because the CP is in a 3-state condition if the reference clock is missing, every leakage through the board, the loop filter components or the VCXO input causes a drift of the VCXO frequency. This leads to a wrong frequency at the outputs of the CDC7005. Further, the locking behavior after the reference clock returns can be negatively affected if V_CTRL is drifting to GND or to V_{CC} (possible with active filters).

To avoid this frequency drift, only loop filter capacitors and VCXOs with a high-resistive input should be used, or the number of missing cycles should be kept low (<100).

5 External Hold Function

The CDC7005 hold function provides the unique feature that the charge pump is placed in a 3-state condition after the first missing reference cycle. However, there are some limitations, because a special reference detection circuit is used for this. If the limitations of the hold function make it unsuited for a certain application, it is possible to switch to the CDCM7005 or to use an external workaround.

The advanced hold functionality of the CDCM7005 is using the lock detection circuit to detect if the reference clock is missing. Therefore, the limits discussed previously do not apply to the CDCM7005.

If it is not possible to switch to the CDCM7005, the following external circuit can be used:

Two resistors are placed close to the charge pump output (CP_OUT) of the CDC7005. The value of both resistors should be equal, and the impedance must be high enough to minimize the influence on the loop filter parameters.

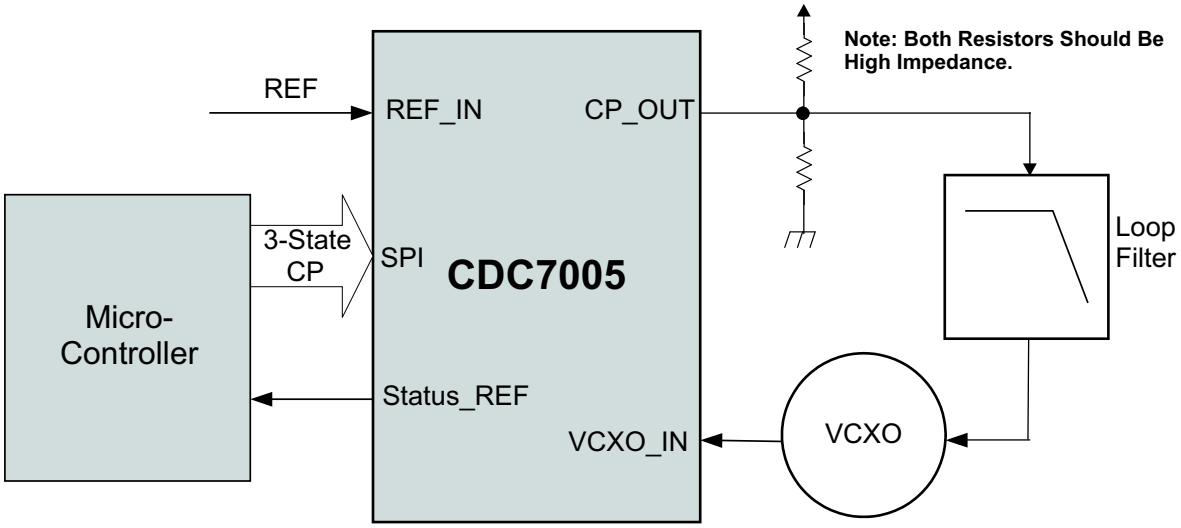

Figure 6. External Hold Function

The STATUS_REF pin of the CDC7005 is connected to a microcontroller. After power up, the CDC7005 is programmed with the microcontroller to the setup defined by the user, and the PLL is locked to the reference clock. The STATUS_REF pin is high.

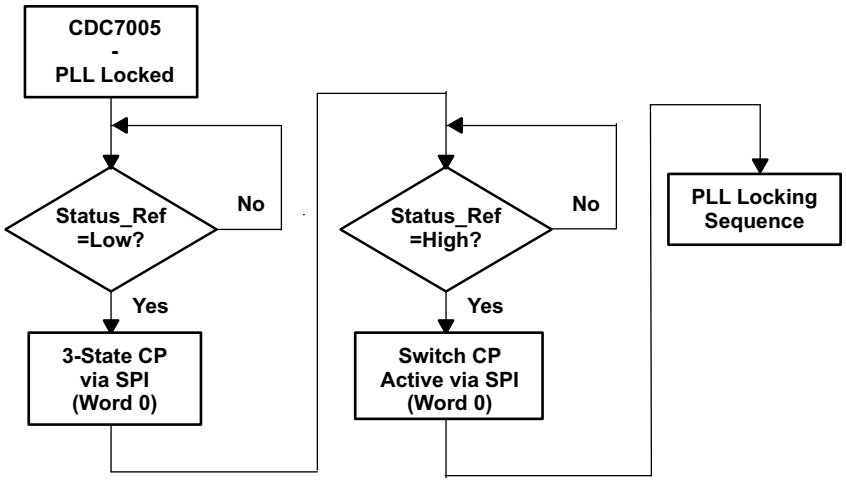

Figure 7. Hold Function Flow Chart

If the reference clock is missing, the STATUS_REF pin is set to low and the microcontroller places the charge pump in a 3-state condition via SPI. The control voltage of the VCXO shifts to $V_{CC}/2$, due to the resistors at the charge pump output. Typically, the control voltage of the VCXO is at $V_{CC}/2$ if the PLL is locked. If this is the case, the frequency of the VCXO is similar to the locked condition after the reference clock is missing. The accuracy of the frequency depends on the voltage gain of the VCXO and on the operating point of the VCXO.

After the reference clock is back again, the charge pump is switched back to the active mode via SPI. A new locking sequence of the PLL is necessary.

6 Conclusion

The CDC7005 hold function has the unique feature of detecting a missing reference clock with the first missing reference cycle. Therefore, the charge pump is placed in a 3-state mode fast, if the reference clock is missing and the VCXO control voltage remains equal. However, some limitations need to be considered.

If the limitations of the CDC7005 hold function make it impossible to use this hold function, an option is to switch to the CDCM7005 hold function or to develop an external workaround as previously described.

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