Application Report
SCAA074–September 2004

Dual Purposes: Data Buffer, the Other Face of the CDCP1803

H. McClendon, C. Sterzik, K. Mustafa *High Performance Analog*

ABSTRACT

The CDCP1803 is a clock driver by design, but can be used as a data buffer. The CDCP1803 performance as a data buffer is demonstrated both in terms of the bit error rate (BER) and eye pattern diagrams. The CDCP1803 is tested over several signaling rates and different PRBS patterns.

Contents

List of Figures

1 Introduction

When choosing a data buffer the amount of jitter introduced by the buffer is crucial. One quantitative measurement that provides insight to the performance of the buffer is the bit error rate (BER). The BER is the ratio of bits that have errors to the total number of bits received. A buffer with more jitter gives the opportunity for more errors, thus a higher BER. The desired BER is dependent on the system requirements. Another measurement that is often used to judge the worthiness of the buffer is the eye pattern diagram. An eye pattern diagram is obtained by overlapping multiple cycles of the signal on the screen of an oscilloscope. The eye opening/closure is indicative of the signal integrity. The deviation of the signal crossing shows the jitter in the signal and its complement, the eye opening, which is usually given as a percentage of the unit interval (UI). A more open eye has a higher margin for the sampling window and therefore a lower chance of bit errors. While the jitter allowed is system dependent, 20% is the recommended maximum.

1.1 Test Setup

The CDCP1803 is a 3.3 V, 1:3 LVPECL (low voltage positive emitter coupled logic) clock buffer with a programmable divider. The CDCP1803 is characterized for industrial temperature (–40°C to 85°C) and has a maximum operating frequency of 800 MHz. The BER measurements were taken with the Anritsu MP1632C a 3.2G bit error rate analyzer with a total of 2E13 bits sent. A Tektronix TDS694C 4-channel digital real-time oscilloscope was used to capture the eye diagrams included in this report. Both test procedures included two meters of cable between the CDCP1803 output and the measurement tool. The block diagrams of the test setups are shown in Figure 1 and Figure 2.

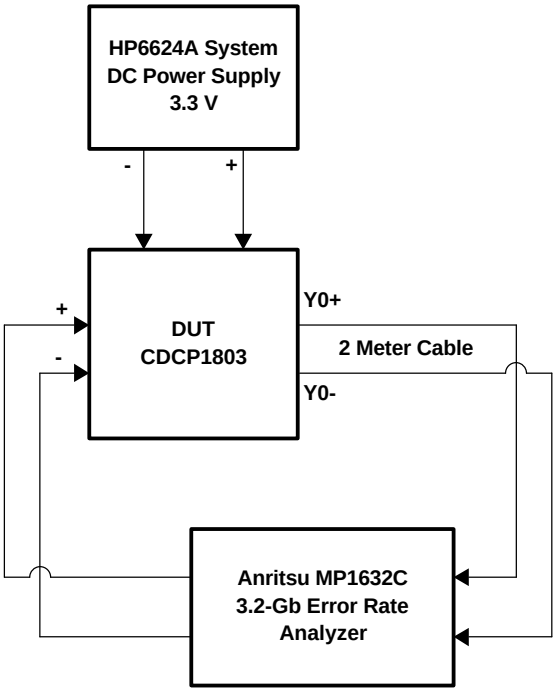

Figure 1. Test Setup for BER Measurements

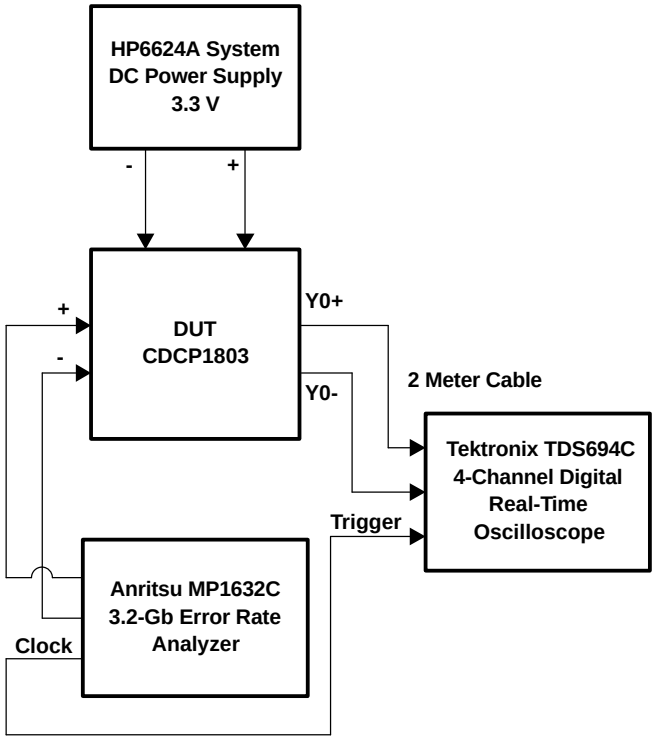

Figure 2. Test Setup for Eye Diagrams

At each data rate tested, the DUT buffered 2E13 total bits for both PRBS patterns of 2^7–1 and 2^{23}–1. For the eye pattern diagram test setup, the data and /data output from the DUT were sent to Channels 2 and 3, respectively, of the oscilloscope. The clock from the bit error rate analyzer was used as the trigger for the oscilloscope.

2 Measurement Results

2.1 BER and Eye Opening

DATA RATE	PRBS PATTERN	BER	EYE OPENING	SHOWN IN
700 Mbps	2^7–1	< 5 E-14	93.49%	Figure 3
700 Mbps	2^{23}–1	< 5 E-14	91.25%	Figure 4
900 Mbps	2^7–1	< 5 E-14	88.29%	Figure 5
900 Mbps	2^{23}–1	< 5 E-14	88.29%	Figure 6
1.1 Gbps	2^7–1	< 5 E-14	84.03%	Figure 7
1.1 Gbps	2^{23}–1	< 5 E-14	84.49%	Figure 8
1.3 Gbps	2^7–1	< 5 E-14	84.78%	Figure 9
1.3 Gbps	2^{23}–1	< 5 E-14	85.82%	Figure 10
1.5 Gbps	2^7–1	< 5 E-14	84.56%	Figure 11
1.5 Gbps	2^{23}–1	< 5 E-14	82.76%	Figure 12

2.2 Eye Diagrams

The cursors are set to measure the openness of the eye diagram which is shown in the top right corner as delta (1.336 ns in Figure 3). Calculations of the % openness follow:

Delta/Unit Interval = 1.336 ns/(1/700 Mbps)

= 1.336 ns/(1.429 ns)

= 0.9349

= 93.49% eye open

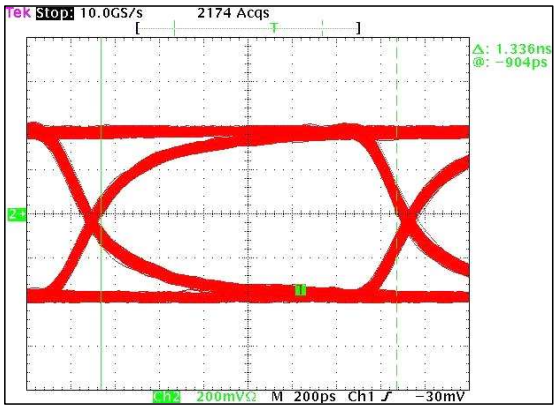

Figure 3. Eye Pattern Diagram at 700 Mbps, PRBS Pattern of 2^7-1

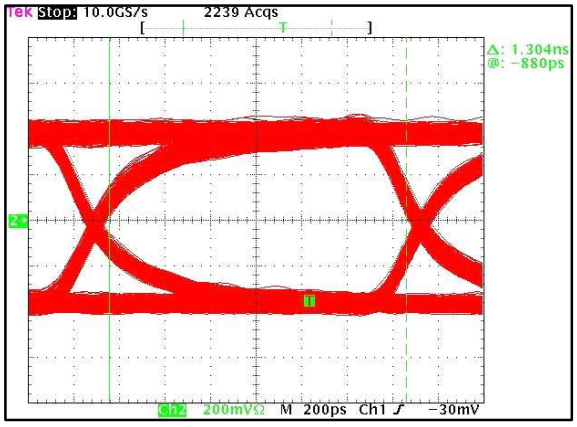

Figure 4. Eye Pattern Diagram at 700 Mbps, PRBS Pattern of 2^{23}–1

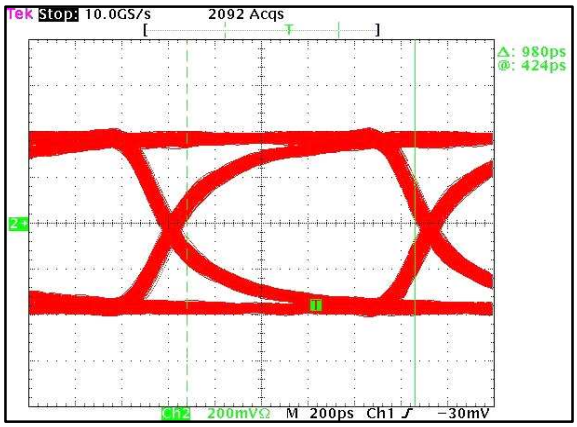

Figure 5. Eye Pattern Diagram at 900 Mbps, PRBS Pattern of 2^7–1

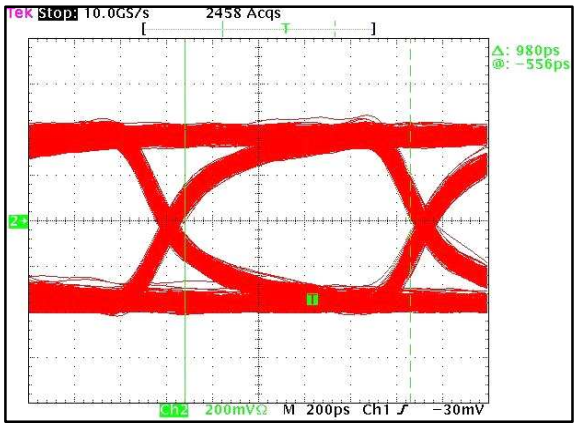

Figure 6. Eye Pattern Diagram at 900 Mbps, PRBS Pattern of 2^{23}–1

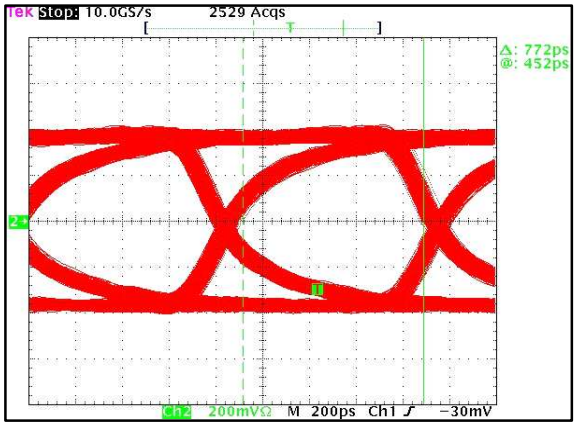

Figure 7. Eye Pattern Diagram at 1.1 Gbps, PRBS Pattern of 2^7–1

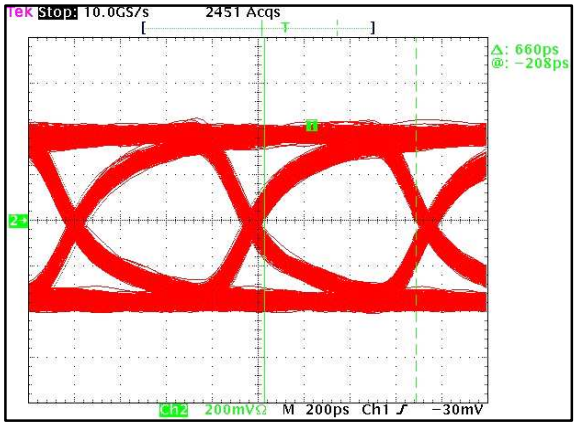

Figure 10. Eye Pattern Diagram at 1.3 Gbps, PRBS Pattern of 2^{23}–1

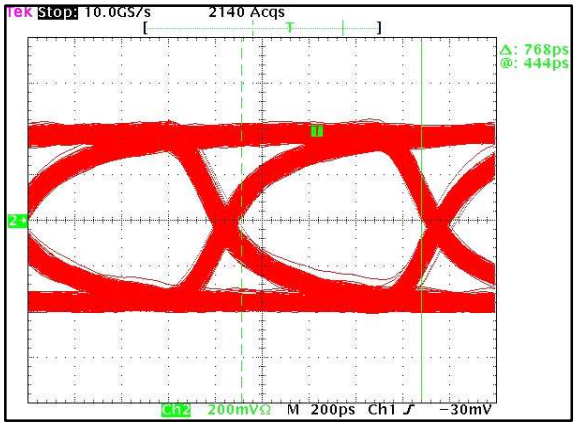

Figure 8. Eye Pattern Diagram at 1.1 Gbps, PRBS Pattern of 2^{23}–1

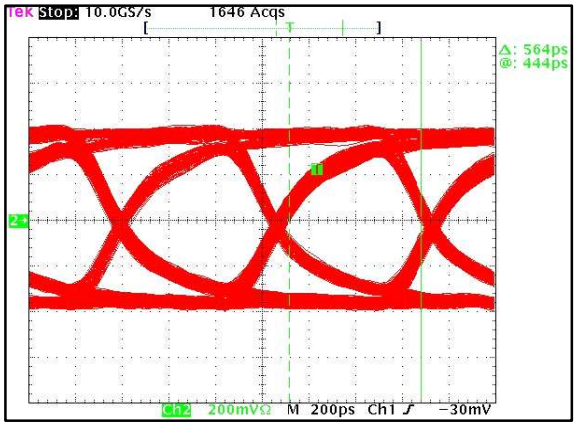

Figure 11. Eye Pattern Diagram at 1.5 Gbps, PRBS Pattern of 2^7–1

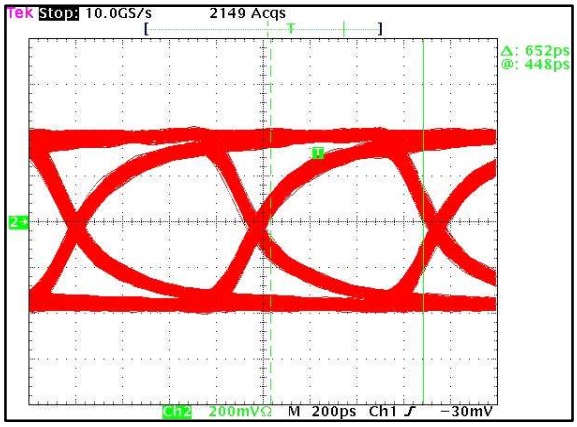

Figure 9. Eye Pattern Diagram at 1.3 Gbps, PRBS Pattern of 2^7–1

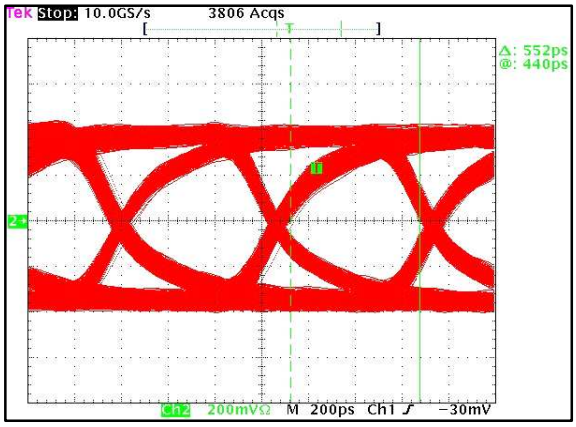

Figure 12. Eye Pattern Diagram at 1.5 Gbps, PRBS Pattern of 2^{23}–1

3 Summary

The data buffer is just one piece of the data communication chain and one contributor to the total interconnect jitter budget. While it is difficult to quantify how a part contributes to the jitter budget of a particular system, a sufficient measure of data performance is the BER or eye opening. The CDCP1803(1) provides an 80% or greater eye opening for signaling rates ranging from 700 Mbps to 1.5 Gbps and for PRBS patterns of 2^7–1and 2^{23}–1. While the CDC1803 is typically used with clocks, the CDC1803 can also be successfully applied to data applications

(1) It should also be noted that the CDCM1802 LVPECL output has similar performance characteristics.

3.1 References

1. CDCP1803 data sheet, Texas Instruments, (SCAS727)
2. CDCM1802 data sheet, Texas Instruments, (SCAS759)
3. *Small Package, Big Performance*, Texas Instruments application report, (SCAA073)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265