No Tradeoffs: Linear Power Supplies for Ultra-Low Power and Dynamic Performance

Design engineers are increasingly looking to shrink power management components in modern electronics, while also making them more efficient. In battery-operated applications, the main constraints are: the size of the system, the size of the battery, and the ability to respond to dynamic loads. Designers must now select power supplies that address these constraints. One such device is theTPS7A02.

Extending Runtime of the Application

Quiescent current (I_Q) is a critical parameter in battery-powered systems. (To learn more about quiescent current, see the *LDO Basics eBook*). This parameter refers to the current consumption of the device in an enabled, light-load situation. In the case of TPS7A02, this device has an ultra-low I_Q of 25 nA which is achieved by utilizing multiple techniques to ensure minimal current draw.

A traditional LDO consists of a pass device, a voltage reference, and an error amplifier, as Figure 1 shows. The voltage reference and error amplifier are the major consumers of current and typically contribute > 80% of the overall current consumption of the device.

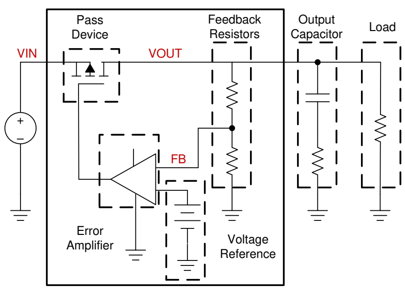
One way to reduce current consumption is by taking advantage of a dynamic biasing circuit. This circuit enables on-the-fly tradeoffs by automatically controlling auxiliary circuits within the regulator which will boost the ground current (I_Q at no load) at a certain level of load without compromising light-load efficiency.

This allows the ground current consumed by the regulator to maintain a very high current efficiency as compared to the load current consumed by the system, as shown in the *Ground Current Efficiency vs Output Current* figure in the *TPS7A02 Nanopower I_Q, 25-nA, 200-mA, Low-Dropout Voltage Regulator With Fast Transient Response Data Sheet*. Equation 1 can be used to calculate the current efficiency (I_η) of a system.

Another feature that sets the TPS7A02 apart from traditional LDOs is its I_Q performance during a dropout condition. This is a very helpful feature to have in battery-powered systems as the battery will deplete over time and approach the output voltage. Typical LDOs show a behavior similar to Figure 2, where I_Q has an overshoot when the device enters into dropout. Thus this may have a negative impact on a product by shortening its battery life.

As Figure 3 shows, when the TPS7A02 experiences a dropout condition, the device uses the improved dynamic-biasing circuit mentioned previously to change the error amplifier loop to allow for proper regulation while maintaining I_Q performance. A device that can inherently do this can increase the lifetime of a battery-powered application.

Figure 1. Traditional PMOS LDO



$$I_\eta\ (\%) = \frac{I_{OUT}}{I_{OUT} + I_Q} \times 100 \quad (1)$$

Figure 2. Typical LDO I_Q vs V_{IN} Behavior

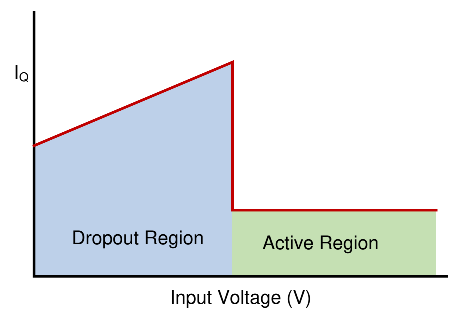
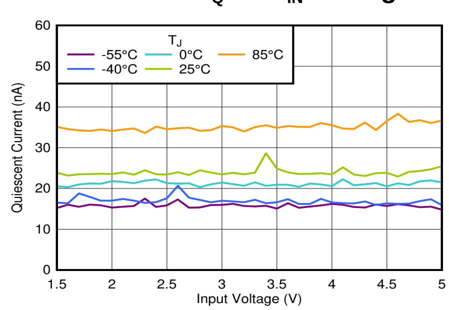


Figure 3. TPS7A02 - I_Q vs V_{IN} During Dropout

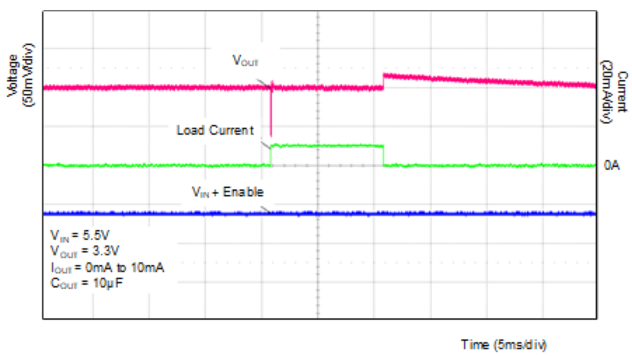


Maintaining Dynamic Performance

Dynamic performance is the most important design tradeoff when considering devices used to minimize the power consumption of a system. It can be distilled into the performance of either the load or line transients. Having the output voltage respond quickly to changes in load or line voltage with minimal deviation is critical when powering sensitive analog and digital loads.

Low I_Q devices have traditionally had slower dynamic performance. A device like the TPS782, for example, boasts 500-nA I_Q and a load transient response as shown in the *Load Transient Response, TPS78233* figure in the *TPS782 500-nA I_Q, 150-mA, Ultra-Low Quiescent Current Low-Dropout Linear Regulator Data Sheet*. Even though this device has 500-nA I_Q, it is not suited for applications where transient response is a critical parameter. When the TPS7A02 device is put under the same conditions, it results in the response as shown in Figure 4. As Table 1 shows, when the TPS7A02 device undergoes a similar load transient, the device shows vast improvement over the TPS782 device.

Figure 4. TPS7A02 Load Transient Response in TPS782 Conditions



It is also common to see devices address the disparity between I_Q performance versus transient response by implementing several modes within an application. The typical scheme is to have an active-mode and a low-power mode. Some manufacturers dedicate a pin within the device to switch between these two states. Toggling the pin to HI will result in a larger current consumption and a faster transient response, versus LO which will result in lower current consumption and a slower transient response.

This combination is helpful in applications where the system is periodically brought from a low-power mode to an active mode. If the transition between these two states is very fast, then large undershoots could be experienced. However, adding an additional pin increases complexity within the system. Designers who use these devices must now not only consider when to toggle the pin for optimum performance, but also manage the routing on the board, which inadvertently increases the solution size. In other words, this is not the easiest solution to the problem.

Table 1. TPS782 vs TPS7A02 Load Transients

Parameters	TPS782	TPS7A02
I_Q	500 nA	25 nA
Overshoot	75 mV	+10 mV
Undershoot	–125 mV	–60 mV
Recovery Time	10 ms	5 µs
V_{IN} = 5.5 V, V_{OUT} = 3.3 V, I_{OUT} = 0 mA to 10 mA, C_{OUT} = 10 µF		

The TPS7A02 device transitions between active and low-power mode automatically without an additional pin. The dynamic biasing circuit detects any change on the output to ensure excellent transient response while maintaining nano-power quiescent current consumption.

The dynamic biasing increases the I_Q as the DC load current increases and based on any error on the output, extending the bandwidth of the loop. The device response time across the output voltage range is constant because it uses a buffered reference topology, which keeps the control loop in unity gain at any output voltage.

Line transient performance is equally as important especially on noisy battery-powered rails powering motors where there can be an expected voltage increase. The TPS7A02 device also utilizes the dynamic biasing circuit to achieve a stable output when experiencing fast line transients. V_{IN} transients figures on the *TPS7A02 Data Sheet* shows examples from typical battery voltages as well as when the device enters dropout conditions.

These features give the device a wide loop bandwidth during transients that ensures excellent dynamic performance while maintaining the ultra-low I_Q of the device in steady-state conditions.

No Tradeoffs

Improving the current consumption of an LDO traditionally meant sacrificing the dynamic performance of your application. TI's family of ultra-low I_Q devices like the TPS7A02 and TPS7A03 provide the advantage of ultra-low nano I_Q level, while maintaining excellent dynamic performance without the complexity of an additional pin.

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