TPS75005 Advanced Information: Sequencer and State Machine

Masashi Nogawa *Power Management Products*

1 OVERVIEW

The TPS75005 is a complete power management solution for the C2000™ controllers from Texas Instruments. This document is supplemental advanced information to the TPS75005 data sheet.

In this advanced information document, the integrated sequencer logic (state machine) is explained in detail.

2 C2000 POWER SEQUENCING

2.1 Sequencing Order by the C2000 Controllers

Depending on the C2000 controller series, the required power-up and power-down order of V_{DD} and V_{DDIO} can be different, as shown in Table 1. Figure 1 and Figure 2 show the typical waveforms of two different sequencing cycles set by the SEQ pin. In these two sequence charts, the TPS75005 signals (OUT1, OUT2, and PG) go to the C2000 pins (V_{DD}, V_{DDIO}, and $\overline{XRS}$), respectively; see Figure 3.

Table 1. Required Power-Up and Power-Down Sequence of C2000 Controllers

C2000 CONTROLLER	POWER-UP ORDER		POWER-DOWN ORDER		TPS75005 SEQ SETTING	TYPICAL WAVEFORM
	1ST CHANNEL TURNED ON	2ND CHANNEL TURNED ON	1ST CHANNEL TURNED OFF	2ND CHANNEL TURNED OFF		
F280x/F2801x	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DD}	Logic low	Figure 1
F281x	V_{DDIO}	V_{DD}	V_{DD}	V_{DDIO}	Logic high	Figure 2
F2823x	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DD}	Logic low	Figure 1
F2833X	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DD}	Logic low	Figure 1

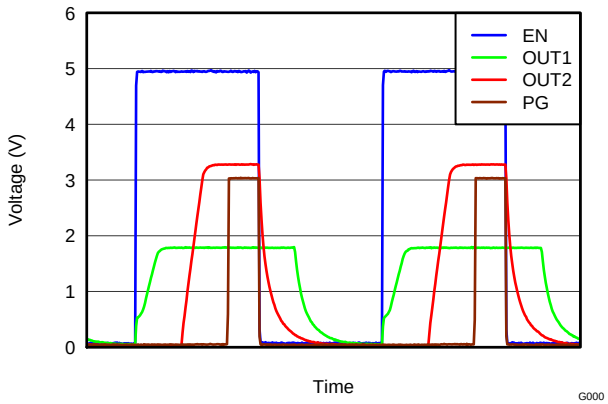

Figure 1. Power Sequence with SEQ = L

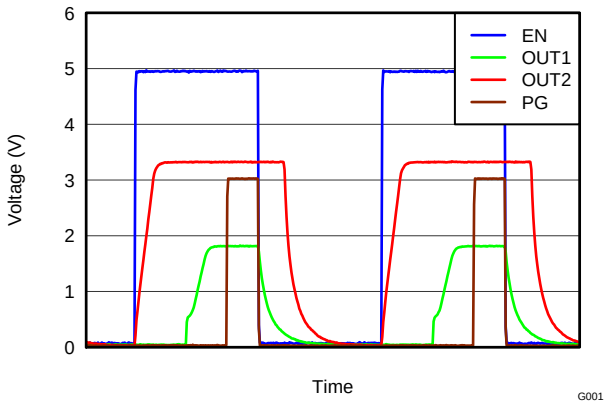

Figure 2. Power Sequence with SEQ = H

2.2 Outline Scenario of Sequencing

Figure 1 and Figure 2 describe the power-up and power-down cycles. A typical outline scenario for these cycles is:

(A) Start from idle status, assuming VIN is higher than the UVLO threshold

(B) Receive EN = H

(C) Power up the first channel in the order set with SEQ

(D) Power up the second channel in the order set with SEQ

(E) 1.8 V and 3.3 V are up and ready, PG goes high, and a C2000 controller begins operation. Usually, the TPS75005 remains at this status while the C2000 controller is processing.

(F) Receive EN = L and immediately PG goes low

(G) Power-down the first channel in the order set with SEQ

(H) Power-down the second channel in the order set with SEQ

(I) Return to idle status

3 SIGNALS USED IN THE SEQUENCER

Refer to Figure 3 for a block diagram that lists all signals used by the TPS75005 sequencer; Table 2 details each signal.

Table 2. List of Signals

NAME	INTERNAL OR EXTERNAL	LOGIC H	LOGIC L	DESCRIPTION
EN	External	Enable the TPS75005	Disable the TPS75005	Enable the control logic input
SEQ	External	See Table 1		Sequence order control logic input
VSET	External	Set the OUT1 voltage to 1.9 V	Set the OUT1 voltage to 1.8 V	LDO1 voltage control logic input
$\overline{UVLO}$	Internal	VIN > 3.55 V (typ)	VIN < 3.55 V (typ)	Active low, undervoltage lock out
iEN	Internal	Logic AND of EN and $\overline{UVLO}$		Master enable signal for the TPS75005
EN1	Internal	Enable LDO1	Disable LDO1	Internal LDO1 enable
EN2	Internal	Enable LDO2	Disable LDO2	Internal LDO2 enable
TSD	Internal	$T_J > T_{TSD}$ (= 165°C)	$T_J < T_{TSD}$ (= 165°C)	Thermal shut down
PG1	Internal	$V_{OUT1} > V_{SVS1}$ (98% of the target Voltage)	$V_{OUT1} < V_{SVS1}$ (98% of the target Voltage)	Internal Power Good for LDO1 See the TPS75005 data sheet for the V_{SVS1} value.
PG2	Internal	$V_{OUT2} > V_{SVS2}$ (98% of the target Voltage)	$V_{OUT2} < V_{SVS2}$ (98% of the target Voltage)	Internal Power Good for LDO2 See the TPS75005 data sheet for the V_{SVS2} value.
PD1	Internal	$V_{OUT1} > V_{DOWN1}$ (= 0.3 V)	$V_{OUT1} < V_{DOWN1}$ (= 0.3 V)	Internal power-down monitor for LDO1
PD2	Internal	$V_{OUT2} > V_{DOWN2}$ (= 0.3 V)	$V_{OUT2} < V_{DOWN2}$ (= 0.3 V)	Internal power-down monitor for LDO2
SW1	Internal	Activate the LDO1 pull-down switch	Deactivate the LDO1 pull-down switch	LDO1 pull-down switch
SW2	Internal	Activate the LDO2 pull-down switch	Deactivate the LDO2 pull-down switch	LDO2 pull-down switch

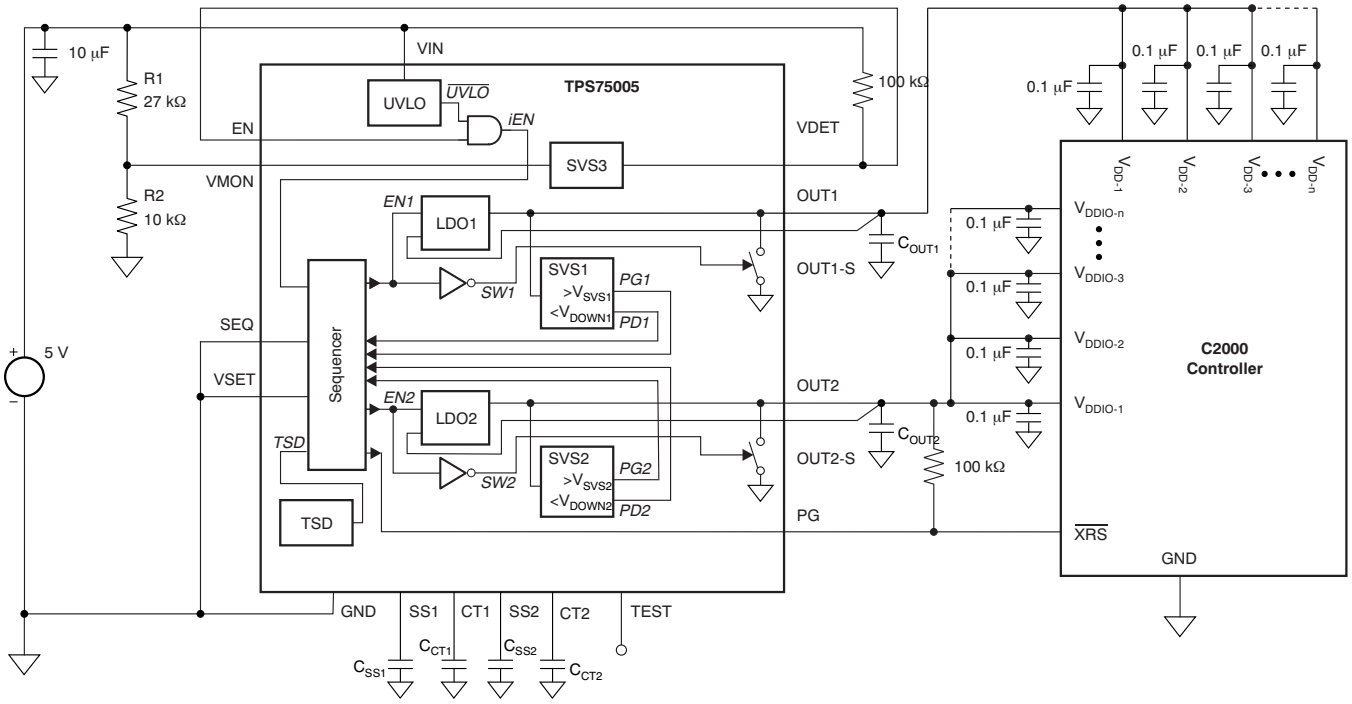

Figure 3. Block Diagram for Signals

In Figure 3, SVS1 and SVS2 stand for *supply voltage supervisor one* or *supply voltage supervisor two*. These blocks contain the voltage threshold detection and the related delay circuitry.

Also in Figure 3, the TPS75005 integrates the small parallel capacitances corresponding to C_{SS1}, C_{CT1}, C_{SS2}, and C_{CT2} on the silicon. Even though these capacitors are not connected on the printed circuit board (PCB), these integrated capacitors are used to perform operations described in this document.

4 SEQUENCE DETAIL

To perform sequencing operations (including error handling), the state machine described in Figure 4, Figure 5, and Table 3 is used. Note that Figure 4 and Figure 5 are identical with only the power sequence order swapped by the SEQ pin logic. In this document, the case of SEQ = L (Figure 4) is primarily used to explain the sequencer.

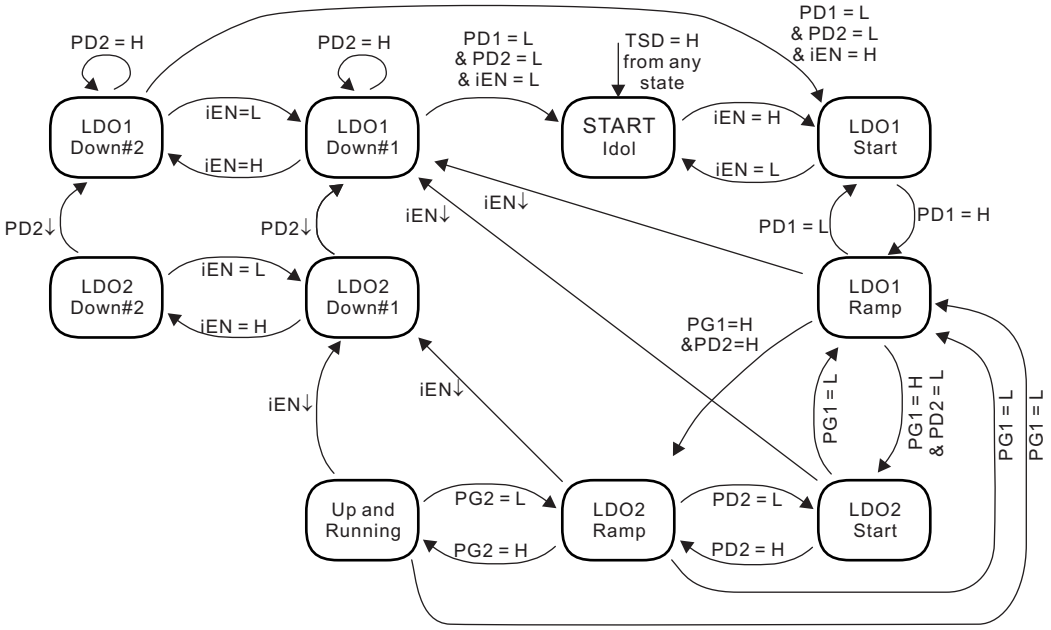

Figure 4. TPS75005 State Diagram (SEQ = L)

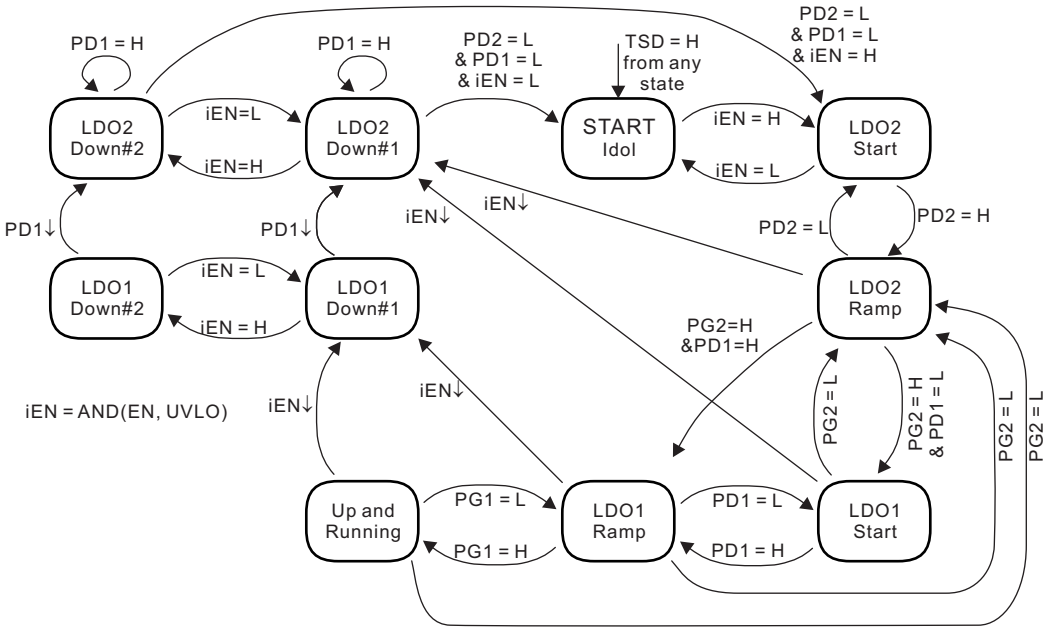

Figure 5. TPS75005 State Diagram (SEQ = H)

Table 3. TPS75005 Sequencing States

	STATE NAME		DESCRIPTION (WITH SEQ = L)
	WITH SEQ = L	WITH SEQ = H	
	START (Idle)	START (Idle)	Device idle state. The device waits for the iEN = H event to begin operation. When iEN goes high, move to the LDO1 Start state.
Power-up sequence	LDO1 Start	LDO2 Start	First LDO1 power-up channel is enabled. A one-shot circuit discharges C_{SS1} at the beginning of this state. Then V_{OUT1} follows $V_{(SS1)}$. When PD1 goes high ($V_{OUT1} > V_{DOWN1}$), move to the LDO1 Ramp state. When iEN goes low, move to the START (Idle) state.
	LDO1 Ramp	LDO2 Ramp	LDO1 continues ramping up. When PG1 goes high ($V_{OUT1} > V_{SVS1}$), move to the LDO2 Start or LDO2 Ramp state. When iEN goes low, move to the LDO1 Down#1 state.
	LDO2 Start	LDO1 Start	Second LDO2 power-up channel is enabled. A one-shot circuit discharges C_{SS2} at the beginning of this state. Then V_{OUT2} follows $V_{(SS2)}$. When PD2 goes high ($V_{OUT2} > V_{DOWN2}$), move to the LDO2 Ramp state. When iEN goes low, move to the LDO1 Down#1 state.
	LDO2 Ramp	LDO1 Ramp	LDO2 continues ramping up. When PG2 goes high ($V_{OUT2} > V_{SVS2}$), move to the Up and Running state. When iEN goes low, move to the LDO2 Down#1 state.
	Up and Running	Up and Running	Because both LDO1 and LDO2 reach the target, PG goes high and the C2000 controller is enabled. When iEN goes low, move to the LDO2 Down#1 state.
Power-down sequence	LDO2 Down#1	LDO1 Down#1	First LDO2 power-down channel is disabled. The SW2 signal activates the pull-down switch and LDO2 decreases. When PD2 goes low ($V_{OUT2} < V_{DOWN2}$), move to the LDO1 Down#1 state. When iEN goes high, move to the LDO2 Down#2 state.
	LDO2 Down#2	LDO1 Down#2	First LDO2 power-down channel is disabled and the next iEN event waits to complete the power-down sequence. With SW2, LDO2 decreases. When PD2 goes low ($V_{OUT2} < V_{DOWN2}$), move to the LDO1 Down#2 state. When iEN goes low, move to the LDO2 Down#1 state.
	LDO1 Down#1	LDO2 Down#1	Second LDO1 power-down channel is disabled. The SW1 signal activates the pull-down switch and LDO1 decreases. When PD1 goes low ($V_{OUT1} < V_{DOWN1}$), move to the START (Idle) state. When iEN goes high, move to the LDO1 Down#2 state.
	LDO1 Down#2	LDO2 Down#2	Second LDO1 power-down channel is disabled and the next iEN event waits to complete the power-down sequence. With SW1, LDO1 decreases. When PD1 goes low ($V_{OUT1} < V_{DOWN1}$), move to the LDO1 Start state. When iEN goes low, move to the LDO1 Down#1 state.

In Table 3, *LDO1 Start* (SEQ = L) is the unique state among the power-up sequence states. At a disable event, the LDO1 Ramp, LDO2 Start, and LDO2 Ramp states move into the corresponding power-down sequence states, but LDO1 Start moves into the START (Idle) state. This difference is because the output of LDO1 is low enough (lower than V_{DOWN1}) that it does not require the power-down operation from LDO1 Start.

5 NORMAL POWER-UP AND POWER-DOWN SEQUENCE

See Figure 6 for the oscilloscope waveforms of the TPS75005 in a normal power-up and power-down sequence with SEQ = L. Refer to the timelines labeled Event A through Event H in Figure 6. A typical sequence is:

1. Before Event A, the TPS75005 is in the START (Idle) state.

   (Power-Up Sequence Begins)

2. At Event A, EN goes to logic high and the device immediately enters the LDO1 Start state. With the LDO1 Start state, a soft-start capacitor (C_{SS1}) is discharged by using a one-shot circuit. Then, the LDO1 soft-start circuit starts charging C_{SS1}. The OUT1 voltage follows the SS1 voltage.
3. Between Event A and Event B, the OUT1 voltage exceeds the V_{DOWN1} threshold to enter the LDO1 Ramp state. The difference between the LDO1 Start and LDO1 Ramp states is the next state when the device is disabled; see Table 3. Without such a disable event, there is no visible boundary between the LDO1 Start and LDO1 Ramp.
4. At Event B, the OUT1 voltage exceeds the V_{SVS1} threshold and the SVS1 delay circuit starts charging C_{CT1}. The device is still in the LDO1 Ramp state.
5. At Event C, the CT1 voltage exceeds the V_{CT1} threshold and enters the LDO2 Start state. With the LDO2 Start state, a soft-start capacitor (C_{SS2}) is discharged by using a one-shot circuit. Then, the LDO2 soft-start circuit starts charging C_{SS2}. The OUT2 voltage follows the SS2 voltage.
6. Between Event C and Event D, the OUT2 voltage exceeds the V_{DOWN2} threshold and enters the LDO2 Ramp state. The difference between the LDO2 Start and the LDO2 Ramp states is the next state when the device is disabled; see Table 3. Without such a disable event, there is no visible boundary between the LDO2 Start and LDO2 Ramp.
7. At Event D, the OUT2 voltage exceeds the V_{SVS2} threshold and the SVS2 delay circuit starts charging C_{CT2}. The device is still in the LDO2 Ramp state.

   (Power-Up Sequence Ends)

8. At Event E, the CT2 voltage exceeds the V_{CT2} threshold and enters the Up and Running state. With the Up and Running state, PG goes high and the C2000 controller is enabled. The device remains in the Up and Running state as long as a disable or an error event occurs.

   (Power-Down Sequence Begins)

9. At Event F, EN goes to logic low and the device immediately enters the LDO2 Down#1 state. With the LDO2 Down#1 state, PG goes to logic low and the C2000 controller is disabled. Then, the internal signal EN2 goes to logic low in order to disable LDO2. Because the active pull-down switch is enabled by the SW2 signal, the OUT2 voltage starts decreasing (note that this ramp-down speed depends on the application circuits).
10. At Event G, the OUT2 voltage underruns the V_{DOWN2} threshold and enters the LDO1 Down#1 state. With the LDO1 Down#1 state, the internal signal EN1 goes to logic low to disable LDO1. Because the active pull-down switch is enabled by the SW1 signal, the OUT1 voltage starts decreasing (note that this ramp-down speed depends on the application circuits).
11. At Event H, the OUT1 voltage underruns the V_{DOWN1} threshold and returns to the START (Idle) state.

    (Power-Down Sequence Ends)

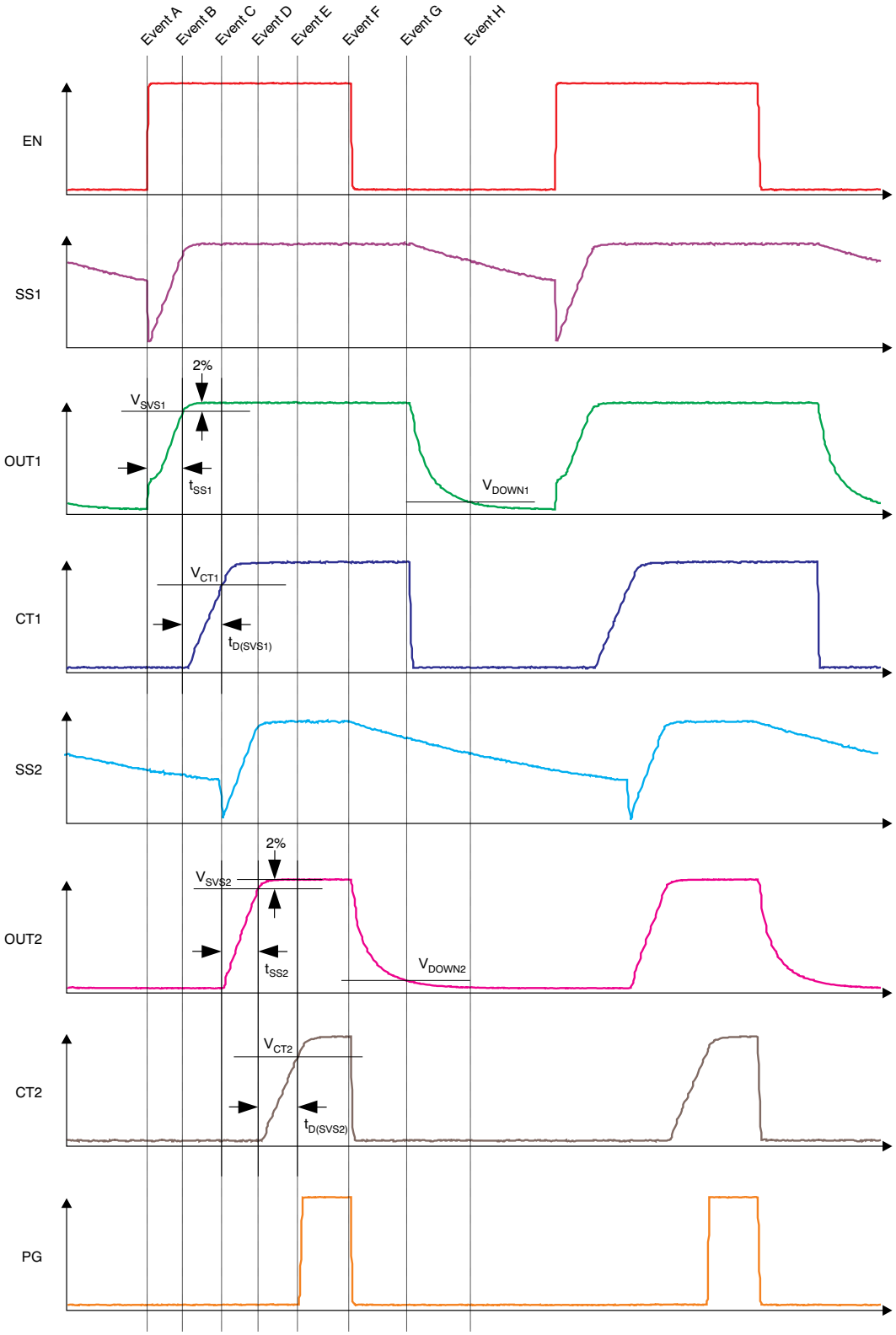

Figure 6. Timing Diagram (EN Enters Power-Down Sequence)

6 REPEATED ENABLE EVENT

Figure 7 illustrates the TPS75005 behavior of a repeated EN signal when the EN signal enters in the middle of a power-down sequence. Figure 7 is nearly identical to Figure 6, except that the second EN rising edge is placed between Event F and Event G. In this situation, the sequencer is designed to complete the current power-down sequence first, and then perform the next power-up process. The power-down sequence described in the *Normal Power-Up and Power-Down Sequence* section is changed in this manner for Figure 7.

(Power-Down Sequence Begins)

9. At Event F, EN goes to logic low and the device immediately enters the LDO2 Down#1 state. With the LDO2 Down#1 state, PG goes to logic low and the C2000 controller is disabled. Then, the internal signal EN2 goes to logic low in order to disable LDO2. Because the active pull-down switch is enabled by the SW2 signal, the OUT2 voltage starts decreasing (note that this ramp-down speed depends on the application circuits).

9a. At Event K, EN goes to logic high during the LDO2 Down#1 state and the device enters the LDO2 Down#2 state. Because the internal signal EN2 remains at logic low, the discharging action with SW2 continues to decrease the OUT2 voltage.

10a. At Event G, the OUT2 voltage underruns the V_{DOWN2} threshold and enters the LDO1 Down#2 state (because EN = H), instead of entering the LDO1 Down#1 state. With the LDO1 Down#2 state, the internal signal EN1 goes to logic low in order to disable LDO1. Because the active pull-down switch is enabled by the SW1 signal, the OUT1 voltage starts decreasing (note that this ramp-down speed depends on the application circuits).

11a. At Event H, the OUT1 voltage underruns the V_{DOWN1} threshold and jumps into the LDO1 Start state instead of entering the START (Idle) state because the EN = H signal for the next powering cycle is still pending from item 9a.

(Power-Down Sequence Ends; Continues to Next Power-Up Sequence)

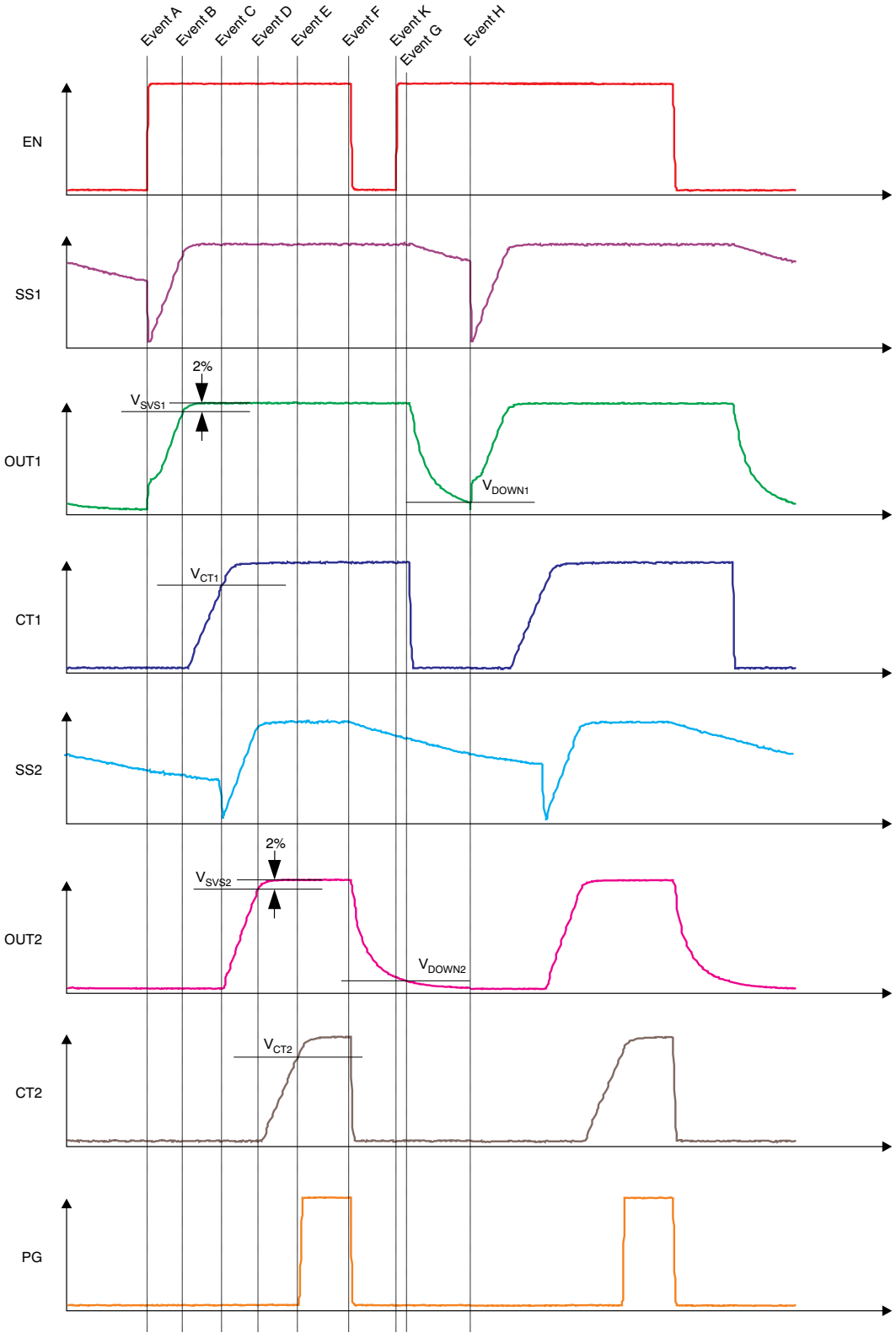

Figure 7. Timing Diagram (EN Enters Power-Down Sequence)

7 INTERRUPTION (DISABLE DURING POWER-UP)

When the TPS75005 is disabled during a power-up sequence, the device immediately begins a power-down sequence from the corresponding state. See Figure 8 for an example of disabling the device when OUT2 is ramping up. The power-up and power-down sequence described in the *Normal Power-Up and Power-Down Sequence* section is changed in this manner for Figure 8.

Note that the TPS75005 performs a proper power-down sequence with a disable event in all power-up sequence states: LDO1 Ramp, LDO2 Start, and LDO2 Ramp (also refer to the *Sequence Detail* section, especially the last paragraph after Table 3).

1. Before Event A, the TPS75005 is in the START (Idle) state.

   (Power-Up Sequence Begins)

2. At Event A, EN goes to logic high and the device immediately enters the LDO1 Start state. With the LDO1 Start state, a soft-start capacitor (C_{SS1}) is discharged by using a one-shot circuit. Then, the LDO1 soft-start circuit starts charging C_{SS1}. The OUT1 voltage follows the SS1 voltage.
3. Between Event A and Event B, the OUT1 voltage exceeds the V_{DOWN1} threshold and enters the LDO1 Ramp state. The difference between the LDO1 Start and LDO1 Ramp states is the next state when the device is disabled; see Table 3. Without such a disable event, there is no visible boundary between LDO1 Start and LDO1 Ramp.
4. At Event B, the OUT1 voltage exceeds the V_{SVS1} threshold and the SVS1 delay circuit starts charging C_{CT1}. The device is still in the LDO1 Ramp state.
5. At Event C, the CT1 voltage exceeds the V_{CT1} threshold and enters the LDO2 Start state. With the LDO2 Start state, a soft-start capacitor (C_{SS2}) is discharged by using a one-shot circuit. Then, the LDO2 soft-start circuit starts charging C_{SS2}. The OUT2 voltage follows the SS2 voltage.

   (Power-Up Sequence Interrupted and Power-Down Sequence Begins)

9b. At Event F, EN goes to logic low and the device immediately enters the LDO2 Down#1 state. Because the previous power-up sequence did not reach the Up and Running state, PG remains at logic low and the C2000 controller is never enabled. The internal signal EN2 goes to logic low to disable LDO2. Because the active pull-down switch is enabled by the SW2 signal, the OUT2 voltage starts decreasing (note that this ramp-down speed depends on the application circuits).

10b. At Event G, the OUT2 voltage underruns the V_{DOWN2} threshold and enters the LDO1 Down#1 state. With the LDO1 Down#1 state, the internal signal EN1 goes to logic low to disable LDO1. Because the active pull-down switch is enabled by the SW1 signal, the OUT1 voltage starts decreasing (note that this ramp-down speed depends on the application circuits).

11b. At Event H, the OUT1 voltage underruns the V_{DOWN1} threshold and returns to the START (Idle) state.

   (Power-Down Sequence Ends)

Although only a disable event while OUT2 ramps up is shown in Figure 8, the TPS75005 properly performs the power-down sequence when EN = L during any step of the power-up sequence. Figure 4, Figure 5, and Table 3 clearly define how such a power-down sequence is performed. Refer to the iEN = L or iEN falling (↓) events in Figure 4, Figure 5, and Table 3.

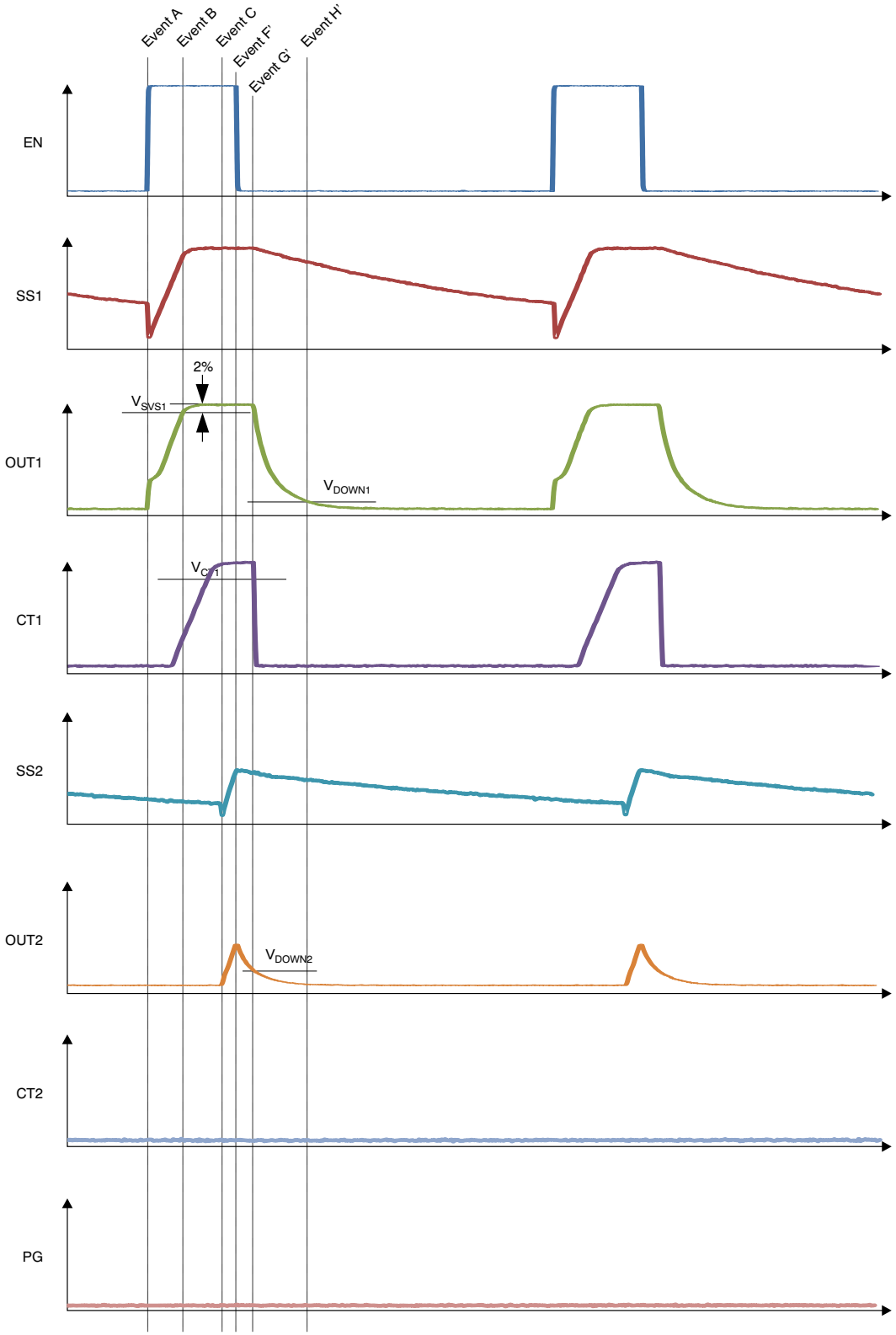

Figure 8. Timing Diagram (Disabled When OUT2 is Ramping Up)

8 ERROR HANDLING

8.1 TSD

Referring to Figure 4 and Figure 5, an arrow above the START (Idle) state bubble explains that the thermal shutdown (TSD) event forces the sequence back to this START (Idle) state from any other state. When TDS is logic high, the sequencer remains at the START (Idle) state. Forcing a return to the START (Idle) state means that both LDO1 and LDO2 are disabled.

8.2 Current Limit

When a current limit event occurs, the device behavior differs depending on whether it occurs at the first channel in power-up or at the second channel in power-up. Refer to the sequencing description in the *Normal Power-Up and Power-Down Sequence* section.

Assuming that SEQ = L, if a current limit event occurs at the second channel of the power-up sequence, that current limit forces the internal signal PG2 low, and the state returns to the LDO2 Ramp state. As soon as PG2 goes low, PG goes low to disable the C2000 controller, and the sequencer waits for PG to go high. When the current limit event ends, the OUT2 voltage returns to the target voltage, and the sequencer returns to the Up and Running state.

Note that after a current limit event, a soft-start function is not performed at the channel that encounters the current limit because a reference voltage to the error amplifier of the channel must be maintained for the current limit to function properly.

If a current limit occurs at the first channel of the power-up sequence, that current limit causes PG1 to go low and the state returns to the LDO1 Ramp state. Note that this state transition is not described in Figure 4 or Figure 5. When the state returns to LDO1 Ramp, PG immediately goes low to disable the C2000 controller. Additionally, the internal LDO2 enable signal (EN2) goes low to discharge the OUT2 voltage. By disabling LDO2, the TPS75005 continues to meet the C2000 power requirements, even with an error condition.

In the LDO1 Ramp state, the sequencer waits for OUT1 to return to the regulated state. When the current limit event ends, the OUT1 voltage returns and the sequencer performs the remaining power-up sequence steps numbered 5 to 8. Here, soft-start for LDO2 is performed in step 5 (there is no soft-start for LDO1).

9 SEQUENCE DOWN

As explained in the *Normal Power-Up and Power-Down Sequence*, *Repeated Enable Event*, and *Error Handling* sections, the TPS75005 device is designed to perform a proper power-down sequence whenever the device receives a disable event. The device is also designed to hold on to the next enable event during a current power-down sequence.

This power-down sequence feature requires one very important application guideline.

NOTE: ***In any application circuit, one or two diodes in series should not be placed from OUT1 (anode, 1.8 V) to OUT2 (cathode, 3.3 V). For more information, see the following paragraphs.***

Such diodes prevent the TPS75005 from performing the power-down sequence, and the application circuit never completes the power-down sequence. Here, the diodes include both discrete and parasitic components inside the device. An example of a parasitic diode is an input protection diode of an operational amplifier. When an input of an op amp is connected to the OUT1 node through small resistance and the op amp is powered by OUT2, an input protection diode meets the criterion to be avoided.

Such diodes conduct current from OUT1 to OUT2 during a power-down sequence when SEQ = L (OUT2 is turned down first and OUT1 is turned down next). Assuming 0.8 V of forward voltage (V_F), OUT2 is clamped at approximately 1.0 V (equal to 1.8 V – 0.8 V) during the power-down sequence. Because that 1.0 V exceeds V_{DOWN2}, the sequencer waits forever for OUT2 to underrun the threshold.

This notice is not applicable to very weak diodes that cannot conduct enough current through an active pull-down resistor of 360 Ω. During a power-down sequence, a 360-Ω resistor pulls down the OUT2 node. If current through the weak diode is low, the voltage across the 360-Ω resistor is also low and the power-down sequence is not affected.

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