



## Table of Contents

1 Overview.....	2
2 Functional Safety Failure In Time (FIT) Rates.....	3
3 Failure Mode Distribution (FMD).....	4
4 Pin Failure Mode Analysis (Pin FMA).....	5

### Trademarks

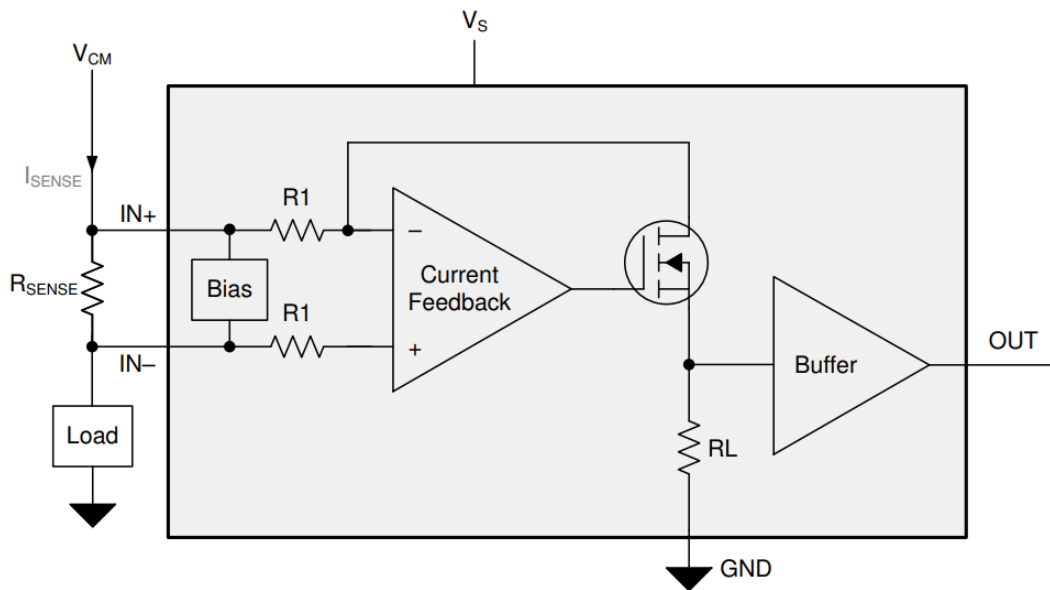
All trademarks are the property of their respective owners.

## 1 Overview

This document contains information for the INA290-Q1/INA280-Q1 (SC-70-5 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



**Figure 1-1. Functional Block Diagram**

The INA290-Q1/INA280-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the INA290-Q1/INA280-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total Component FIT Rate	6
Die FIT Rate	4
Package FIT Rate	2

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 20 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
4	BICMOS Op Amp, Comparators, Voltage Monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the INA290-Q1/INA280-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution (%)
OUT open (Hi-Z)	20%
OUT to GND	25%
OUT to VS	25%
OUT functional, not in specification	30%

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA290-Q1/INA280-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

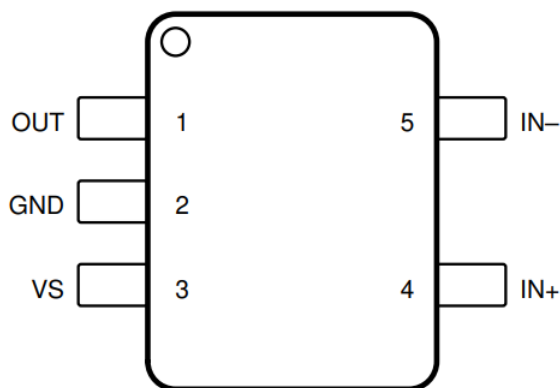
- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 4-1](#) shows the INA290-Q1/INA280-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA290-Q1/INA280-Q1 data sheet.



**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- $V_+ = 2.7\text{ V}$  to  $20\text{ V}$
- $V_{CM} = 2.7\text{ V}$  to  $+120\text{ V}$

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed $150^{\circ}\text{C}$ .	B
GND	2	Normal operation.	D
VS	3	Power supply shorted to GND.	B
IN+	4	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. In low side configuration, input pins are shorted.	B
IN-	5	5 In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. In low side configuration, normal operation.	B for high side; D for low side

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
GND	2	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
VS	3	No power supply to device.	B
IN+	4	IN+ will be at the same potential as IN-. Differential input voltage is effectively 0 V	B
IN-	5	IN- will be at the same potential as IN+. Differential input voltage is effectively 0 V.	B

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	2 – GND	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	3 – VS	Power supply shorted to GND.	B
VS	3	4 – IN+	In high-side configuration, device power supply shorted to bus supply, which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND.	A for high side; B for low side
IN+	4	5 – IN-	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN-	5	1 – OUT	In high-side configuration, OUT is shorted to bus supply, which may cause damage if high voltage is present. In low-side configuration, OUT is shorted to GND.	A for high side; B for low side

**Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	Power supply shorted to GND.	B
VS	3	Normal operation.	D
IN+	4	In high-side configuration, device power supply shorted to bus supply, which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND (through RSHUNT).	A for high side; B for low side
IN-	5	In high-side configuration, device power supply shorted to bus supply (through RSHUNT), which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND.	A for high side; B for low side

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated