Application Report

RTD Wire-Break Detection Using Precision Delta-Sigma ADCs

ABSTRACT

Sensor wire breaks are an uncommon but inevitable challenge in industrial environments, requiring fault identification to enable the host to take corrective action. Resistance temperature detectors (RTDs) fall into this category of sensors where wire-break detection is necessary. This application report discusses ways to use features commonly found in delta-sigma (ΔΣ) analog-to-digital converters (ADCs) to help identify wire breaks for all common RTD configurations.

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Trademarks

1 Introduction

Resistance temperature detectors (RTDs) are highly-accurate sensors that can measure wide temperature ranges. RTDs are used in a variety of industrial applications, including analog input modules in programmable logic controllers (PLC), temperature transmitters, and patient monitoring equipment. These dynamic commercial and industrial environments occasionally result in RTD wires becoming damaged or disconnected. For reliable operation, these fault conditions must be detected so the host controller can either correct the fault if possible, or put the system in a default state if necessary.

To aid this process, this application report defines a methodology for broken-wire detection in all common RTD configurations using the integrated features in precision ΔΣ ADCs. This document begins by describing these features in detail, including how they work and why they are useful for wire-break detection. The subsequent sections present each RTD configuration, stepping through what occurs as each wire (or group of wires) breaks and how these breaks are identified. Finally, additional features to aid in wire-break detection and pseudo code are included in Appendix A and Appendix B, respectively. This information generally applies to many precision ΔΣ ADCs, including the devices in Table 1-1:

Table 1-1. Precision ΔΣ ADCs for RTD Measurements

Cost-Optimized	Low Power	Lowest Noise
ADS1120	ADS114S06B	ADS125H02
ADS112C04	ADS114S08B	ADS1260
ADS112U04	ADS114S06	ADS1261
ADS1220	ADS114S08	ADS1262
ADS122C04	ADS124S06	ADS1263
ADS122U04	ADS124S08	—

Finally, this application report assumes a general understanding of the various RTD configurations and how they work under normal operating conditions. To learn more about these topics, see the related *A Basic Guide to RTD Measurements* application report.

2 Features Used to Detect Wire Breaks in RTD Systems

RTD wire breaks can be detected using just the excitation current sources (IDACs) integrated into the ADC along with voltage reference (VREF) monitoring.

All devices in Table 1-1 integrate two matched current sources, which are commonly used to establish a voltage across an RTD that is then measured by an ADC. For VREF monitoring, many ADCs include a discrete diagnostic circuit that can be read in real-time. Or, another option for VREF monitoring involves reading back the differential reference voltage with an unused measurement channel. Both of these scenarios are discussed in the following subsections.

2.1 Detecting a Wire Break Using a Continuous VREF Monitor

Figure 2-1 shows a 4-wire RTD using a low-side reference resistor (R_{REF}) as an example of how to use IDACs and VREF monitoring to detect an RTD wire break. One IDAC is used for this RTD configuration, flowing through lead 1, R_{RTD}, lead 4, and finally through R_{REF} to ground. The ADC measures the RTD voltage at AINP and AINN and uses the voltage established across R_{REF} as the reference voltage.

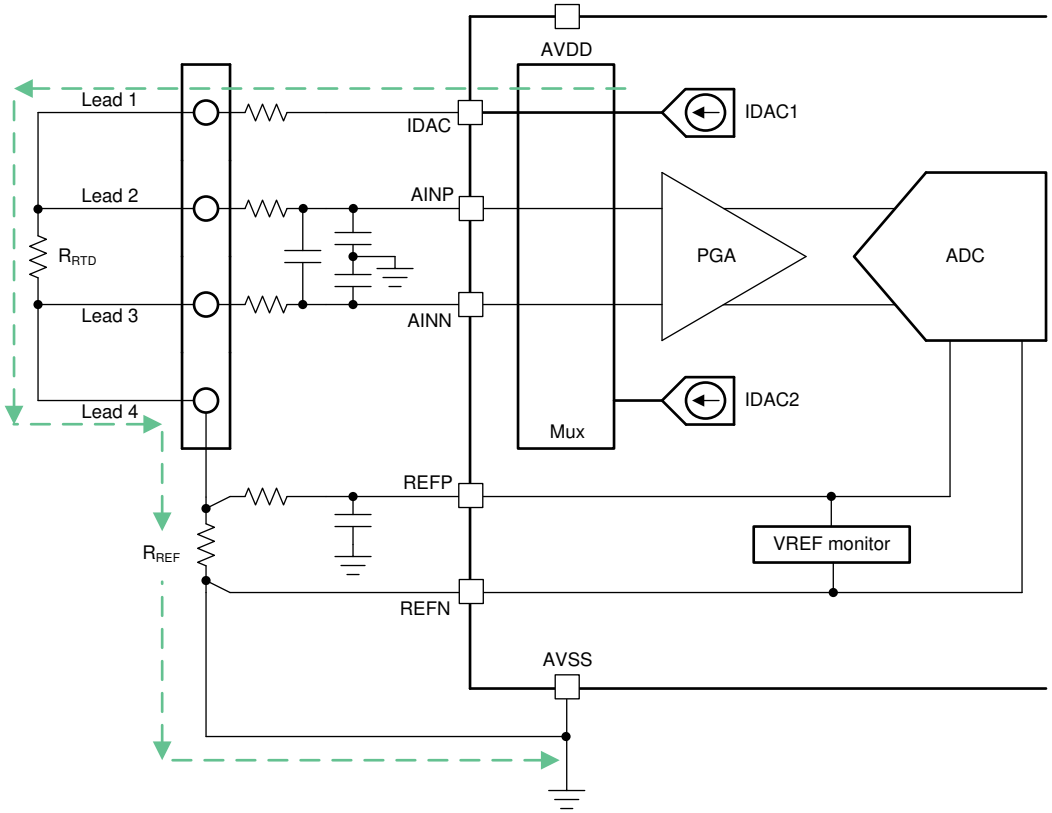


Figure 2-1. IDAC Current Flow in a 4-Wire RTD With a Low-Side R_{REF}

When a wire breaks, the current may no longer flow through the RTD, or more specifically through R_{REF}. With no current flowing through R_{REF}, the ADC reads a differential reference voltage of approximately 0 V between REFP and REFN. For example, Figure 2-2 shows that the IDAC current return path becomes an open circuit if lead 4 breaks.

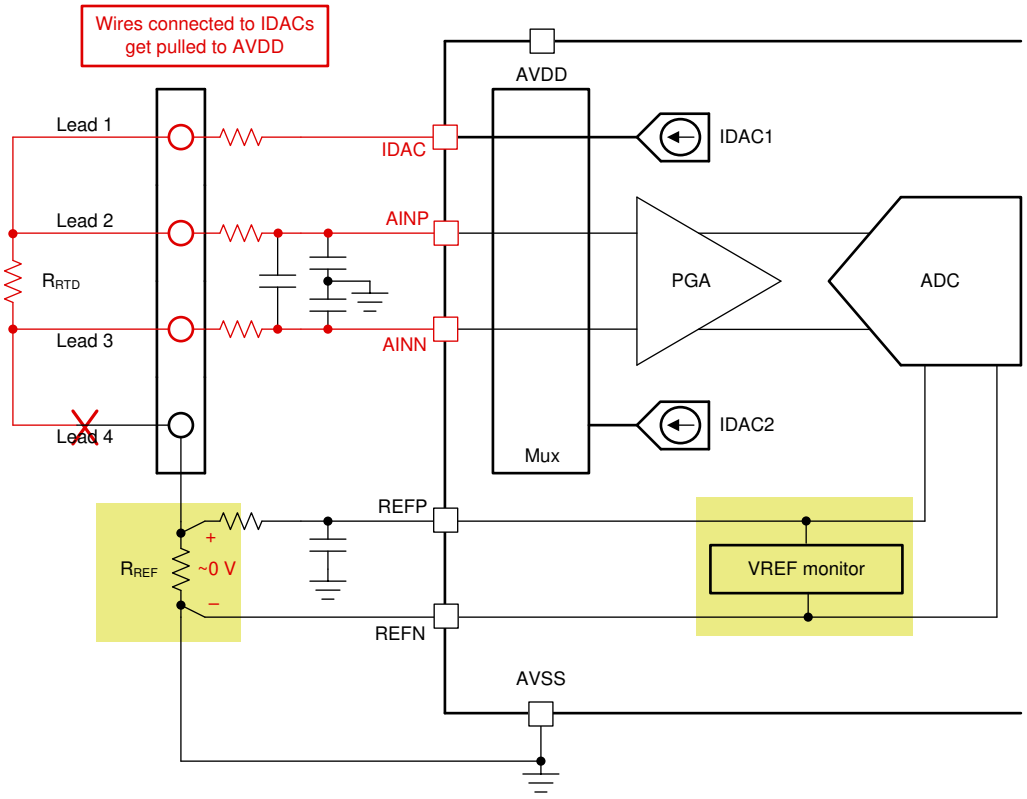


Figure 2-2. Detecting a Wire Break Using a Continuous VREF Monitor

In Figure 2-2, the near-zero differential voltage applied between REFP and REFN trips the VREF monitor in the ADC, which has a typical threshold of a few hundred millivolts. This monitor sets a flag in the ADC STATUS byte that can be read continuously by the host to determine corrective action. In other words, this monitoring is completed in real-time without interrupting the precision RTD measurement.

2.2 Detecting a Wire Break Using a Periodic VREF Monitor

The ADS1220, ADS122C04, and ADS122U04 (as well as their 16-bit counterparts) offer a specific input multiplexer configuration that measures back the external VREF voltage using the internal VREF as the reference. Table 2-1 from the ADS1220 data sheet shows that setting MUX[3:0] = 1100b measures (VREFPx – VREFNx) / 4. In the event of a wire break where no current flows through R_{REF}, this measurement is approximately 0 V, indicating a fault.

Table 2-1. Enabling the ADS1220 Periodic VREF Monitor Using the MUX[3:0] Bits

Bit	Field	Type	Reset	Description
7-4	MUX[3:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. For settings where AINN = AVSS, the PGA must be disabled (PGA_BYPASS = 1) and only gains 1, 2, and 4 can be used. 0000: AINP = AIN0, AINN = AIN1 (default) 0001: AINP = AIN0, AINN = AIN2 0010: AINP = AIN0, AINN = AIN3 0011: AINP = AIN1, AINN = AIN2 0100: AINP = AIN1, AINN = AIN3 0101: AINP = AIN2, AINN = AIN3 0110: AINP = AIN1, AINN = AIN0 0111: AINP = AIN3, AINN = AIN2 1000: AINP = AIN0, AINN = AVSS 1001: AINP = AIN1, AINN = AVSS 1010: AINP = AIN2, AINN = AVSS 1011: AINP = AIN3, AINN = AVSS 1100: (V(REFPx) – V(REFNx)) / 4 monitor (PGA bypassed) 1101: (AVDD – AVSS) / 4 monitor (PGA bypassed) 1110: AINP and AINN shorted to (AVDD + AVSS) / 2 1111: Reserved

The challenge with this approach is that the VREF voltage cannot be monitored continuously. Instead, halt RTD measurements and switch over to the monitoring channel, increasing system latency and complexity compared to using an ADC with a continuous VREF monitor. Choose how often to interleave diagnostic measurements by balancing increased latency with the required system response time to a fault condition.

2.3 Detecting a Wire Break Using Separate Analog Inputs

If the ADC does not have any method for integrated VREF monitoring, Figure 2-3 shows how a dedicated set of analog inputs can be used to measure back the reference voltage using the ADC signal path.

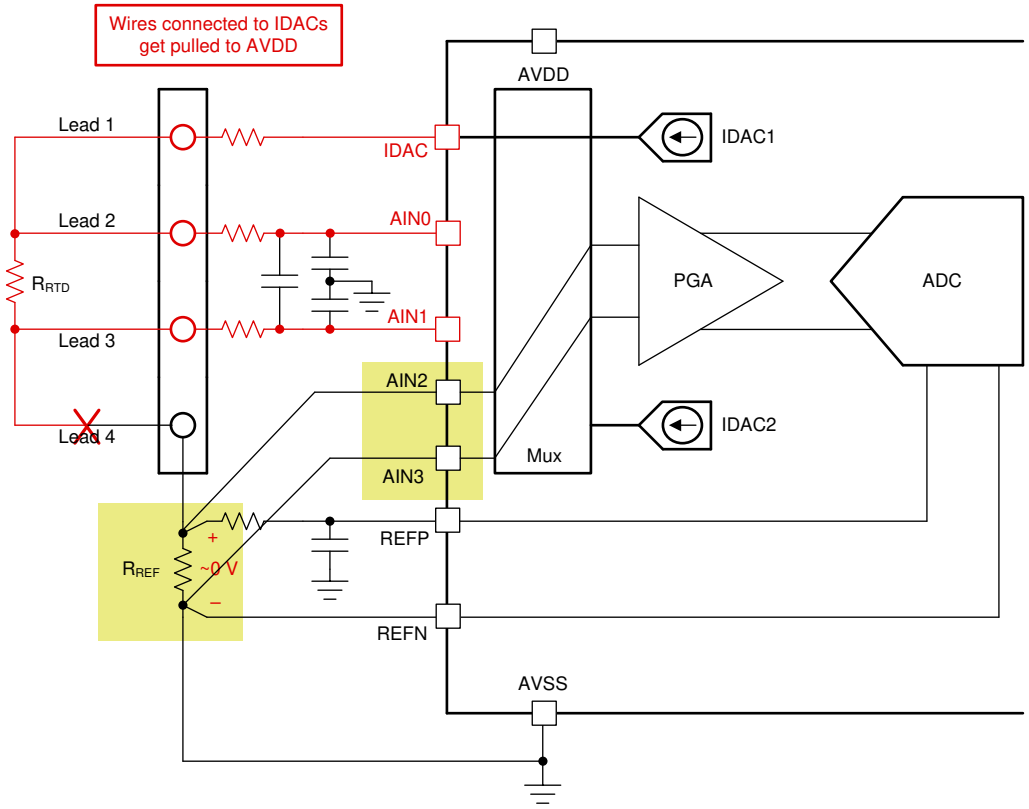


Figure 2-3. Detecting a Wire Break Using Separate Analog Inputs

The system in Figure 2-3 uses AIN0 and AIN1 to measure the RTD voltage and AIN2 and AIN3 are used to read back the voltage across R_{REF}. Just like in the periodic VREF monitoring case, a fault is detected if the measured voltage between AIN2 and AIN3 is close to 0 V. At this point, the host can take corrective action if necessary. Similar to the case described in Section 2.2, the challenge with this approach is that the VREF voltage cannot be monitored constantly. Instead, RTD measurements must be halted in order to switch over to the monitoring channel, increasing system latency and complexity compared to using an ADC with an integrated VREF monitor. Moreover, the ADC requires another reference voltage source when using separate analog inputs to measure back the VREF voltage, as the reference voltage source for the RTD is now the measurement channel.

Although increased latency resulting from internal multiplexer switching cannot be overcome, the system can be simplified as shown in Figure 2-3 by using an ADC with multifunction analog inputs. Using such an ADC eliminates the dedicated traces running from R_{REF} to the input multiplexer because REFx are shared with AINx. As an example, Figure 2-4 illustrates how REFP1 and REFN1 are shared with AIN0 and AIN3, respectively, in the ADS1220.

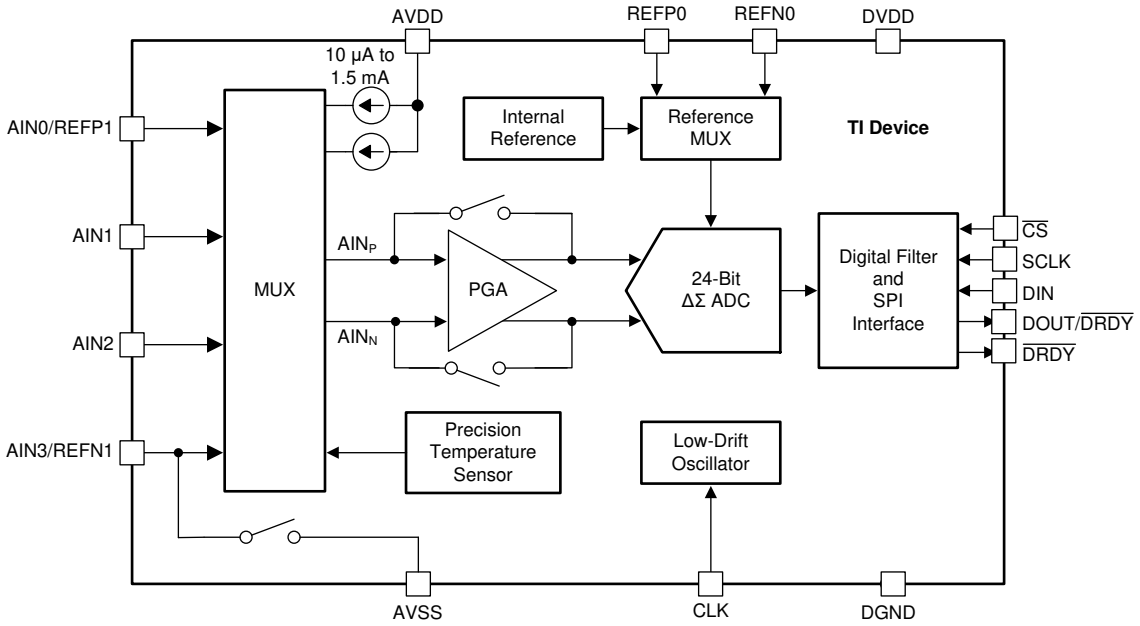


Figure 2-4. ADS1220 Block Diagram

Table 2-2 summarizes the wire-break detection features integrated into the precision ΔΣ ADCs highlighted in Table 1-1.

Table 2-2. Summary of Wire-Break Detection Features in Precision ΔΣ ADC

Device	Dual, Matched IDACs?	VREF Monitor?
ADS1120	Yes: any analog input	Periodic = (VREFPx – VREFNx) / 4
ADS112C04		
ADS112U04		
ADS1220		
ADS122C04		
ADS122U04		
ADS114S06B		Continuous = 300-mV threshold
ADS114S08B		
ADS114S06		
ADS114S08		
ADS124S06		
ADS124S08		
ADS1260		Continuous = 400-mV threshold
ADS1261		
ADS1262		
ADS1263		
ADS125H02	Yes: dedicated pins	

For the remainder of this document, the continuous VREF monitor is used to detect RTD wire breaks because this method is the simplest to implement. However, using a periodic VREF monitor or dedicated analog inputs are still acceptable methods for determining wire breaks in all configurations.

3 Wire-Break Detection Methods for Different RTD Configurations

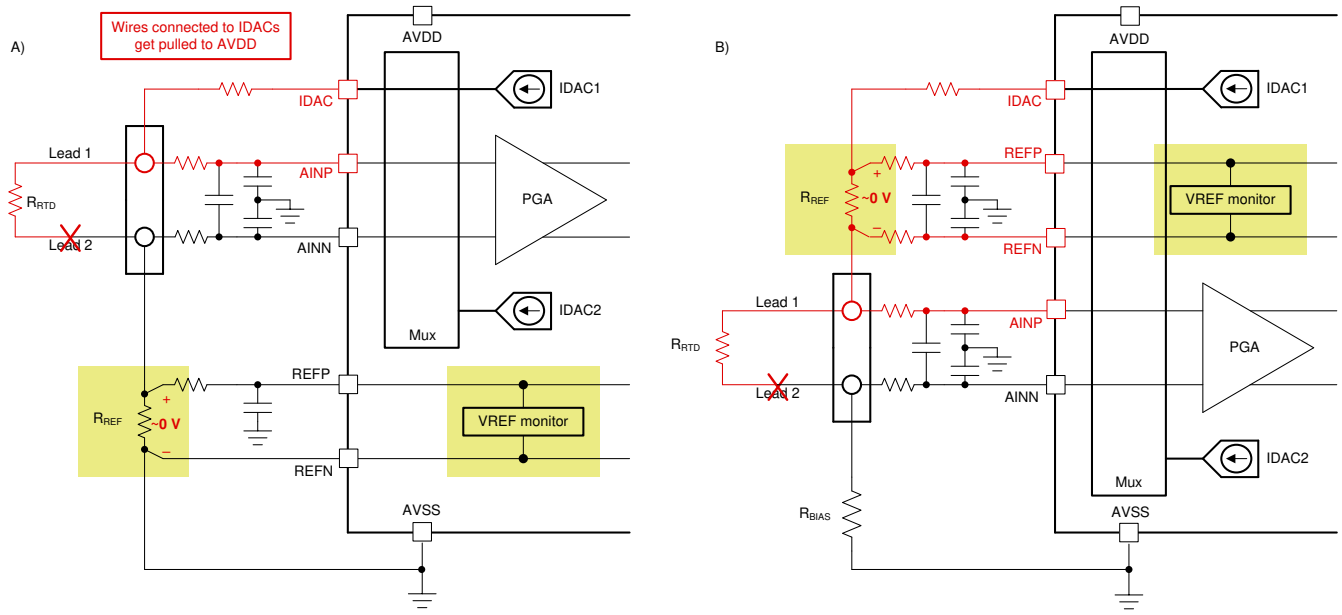
The simplest form of RTD wire-break detection is the ability to detect *any* wire breaks. In other words, the system only needs to identify if one or more wires are broken but does not need to determine *which* wire breaks. This document discusses the events that occur as each wire (or group of wires) breaks in the following RTD configurations:

- 2-wire RTD using a low-side R_{REF}
- 2-wire RTD using a high-side R_{REF}
- 3-wire RTD using one IDAC and a low-side R_{REF}
- 3-wire RTD using one IDAC and a high-side R_{REF}
- 3-wire RTD using two IDACs and a low-side R_{REF}
- 3-wire RTD using two IDACs and a high-side R_{REF}
- 4-wire RTD using a low-side R_{REF}
- 4-wire RTD using a high-side R_{REF}

3.1 Wire-Break Detection Using 2-Wire RTDs

Two-wire RTDs provide low-accuracy measurements because no option exists to compensate for lead resistance. However, 2-wire RTDs are low cost and easy to implement, making them attractive for cost-sensitive applications. Moreover, wire-break detection in 2-wire RTDs is straightforward, although determining which wire (or wires) is no longer attached is not possible.

Figure 3-1 shows what happens when lead 2 breaks in the 2-wire RTD configuration: Figure 3-1a shows the low-side R_{REF} implementation and Figure 3-1b shows the high-side R_{REF} implementation. Although Figure 3-1 shows a break in lead 2, the same detection scheme applies to a break in lead 1 or if both wires break.



A) Wire breaks (2W RTD, LS R_{REF})
B) Wire breaks (2W RTD, HS R_{REF})

Figure 3-1. Lead 2 Broken in a 2-Wire RTD Implementation: Low-Side (Left) and High-Side (Right) R_{REF}

For both reference configurations, a broken wire (or wires) results in no current flow through R_{REF} because the path to ground is disconnected. This event drops the voltage across R_{REF} to 0 V, thereby setting the VREF monitor flag high. Therefore, to identify a break in either wire in a 2-wire RTD configuration using either a low-side or high-side R_{REF}, use the VREF monitor in the ADC. Table 3-1 summarizes the wire-break detection method and expected results for all wire-break conditions using a 2-wire RTD.

Table 3-1. Wire-Break Detection Summary for 2-Wire RTD Systems (Low-Side or High-Side R_{REF})

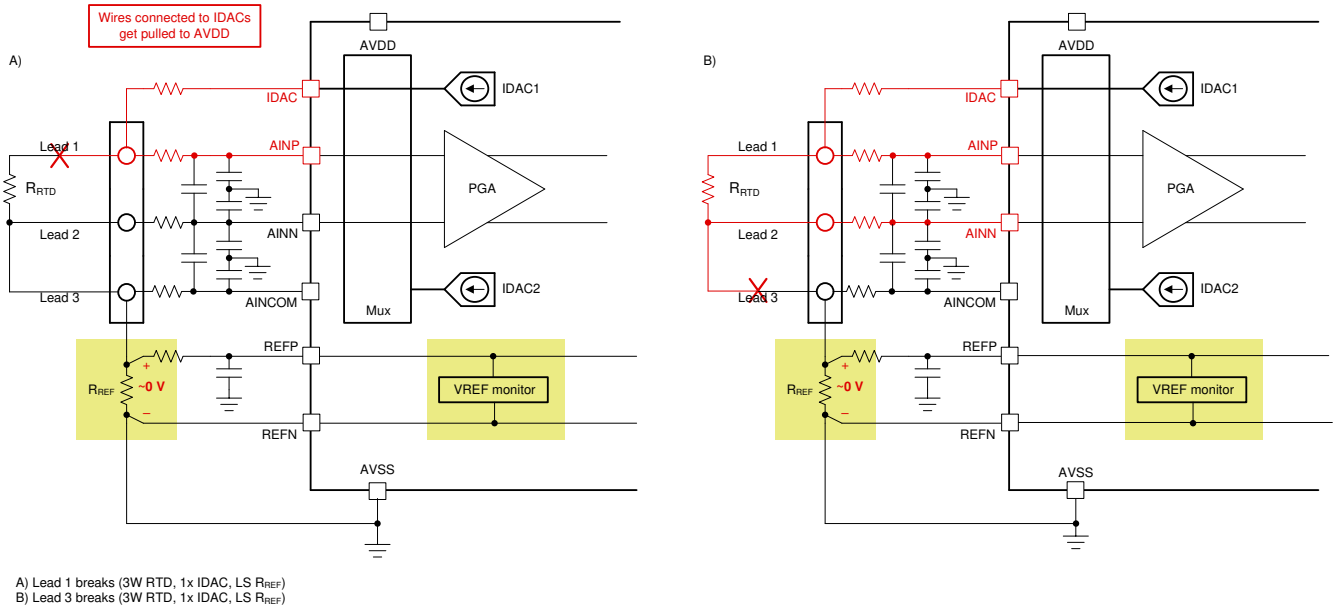
Lead 1	Lead 2	Wire-Break Detection Method and Result
Connected	Broken	• VREF monitor → VREF voltage ≈ 0 V
Broken	Connected	
Broken	Broken	

3.2 Wire-Break Detection Using 3-Wire RTDs

Three-wire RTDs offer a good balance between accuracy and cost, and are very common in precision industrial applications. Lead resistance errors can be removed in either a one-IDAC or two-IDAC implementation. The one-IDAC and two-IDAC implementations employ slightly different wire-break detection schemes, as discussed in the following subsections.

3.2.1 Wire-Break Detection in a One-IDAC, 3-Wire RTD System

Similar to the 2-wire RTD configurations, a wire break can be detected in a one-IDAC, 3-wire RTD system in most cases just by reading the VREF monitor. Figure 3-2 shows that the IDAC current has no return path to ground when lead 1 (shown in Figure 3-2a) or lead 3 (shown in Figure 3-2b) breaks. In these cases, the VREF monitor identifies a fault.



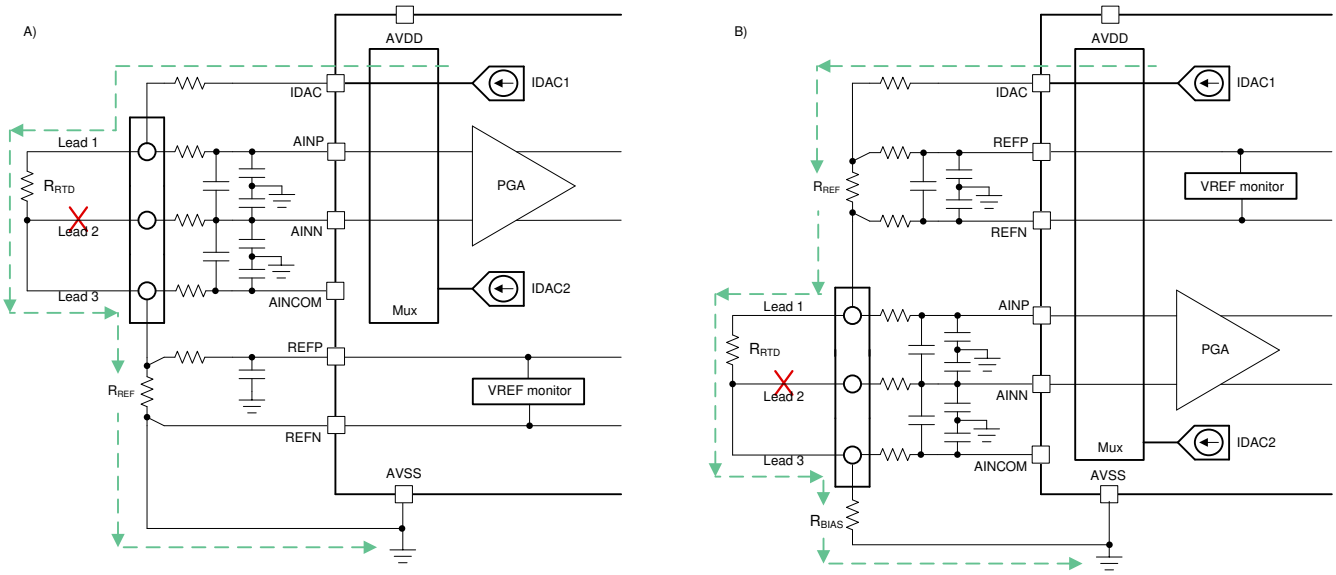
A) Lead 1 breaks (3W RTD, 1x IDAC, LS R_{REF})
B) Lead 3 breaks (3W RTD, 1x IDAC, LS R_{REF})

Figure 3-2. Lead 1 (left) and Lead 3 (right) Break in a One-IDAC, 3-Wire RTD System

Lead 2 can also be broken in any case shown in Figure 3-2, but would have to be verified separately from the VREF flag and is discussed in Section 3.2.1.1 and Section 3.2.1.1.1. These conclusions are true for measurements using both a low-side and high-side R_{REF}, even though Figure 3-2 shows low-side R_{REF} configurations only.

3.2.1.1 Detecting a Break in Lead 2 in a One-IDAC, 3-Wire RTD System

As stated in Section 3.2.1, the VREF monitor cannot detect a break in lead 2 when using a one-IDAC, 3-wire RTD system. In other words, a fault can occur during normal operation that cannot be detected by the VREF monitor alone. Data may start to deviate from the expected value, but do not assume that this deviation results from a wire break as opposed to some other system anomaly. Figure 3-3 shows this behavior.



A) Lead 2 breaks (3W RTD, 1x IDAC, LS R_{REF})
B) Lead 2 breaks (3W RTD, 1x IDAC, HS R_{REF})

Figure 3-3. No VREF Monitor Fault When Lead 2 breaks in a One-IDAC, 3-Wire RTD System Using a Low-Side (Left) and High-Side (Right) R_{REF}

In order to detect a wire break, perform a diagnostic measurement by first halting precision RTD measurements and then changing the system configuration settings. Because RTD measurements must be stopped in this case, choose how often to interleave diagnostic measurements by balancing increased latency with the required system response time to a fault condition.

Detecting a break in lead 2 using a one-IDAC, 3-wire RTD system requires differentiating between a low-side and a high-side R_{REF} configuration as well as switching the IDAC output to a different analog input. Some ADCs do not integrate the functionality to route an IDAC to any analog input, especially ADCs with dedicated IDAC pins. Therefore, external circuitry may be required to perform this function. Either way, Figure 3-4 illustrates how to enable the IDACs using a low-side R_{REF}.

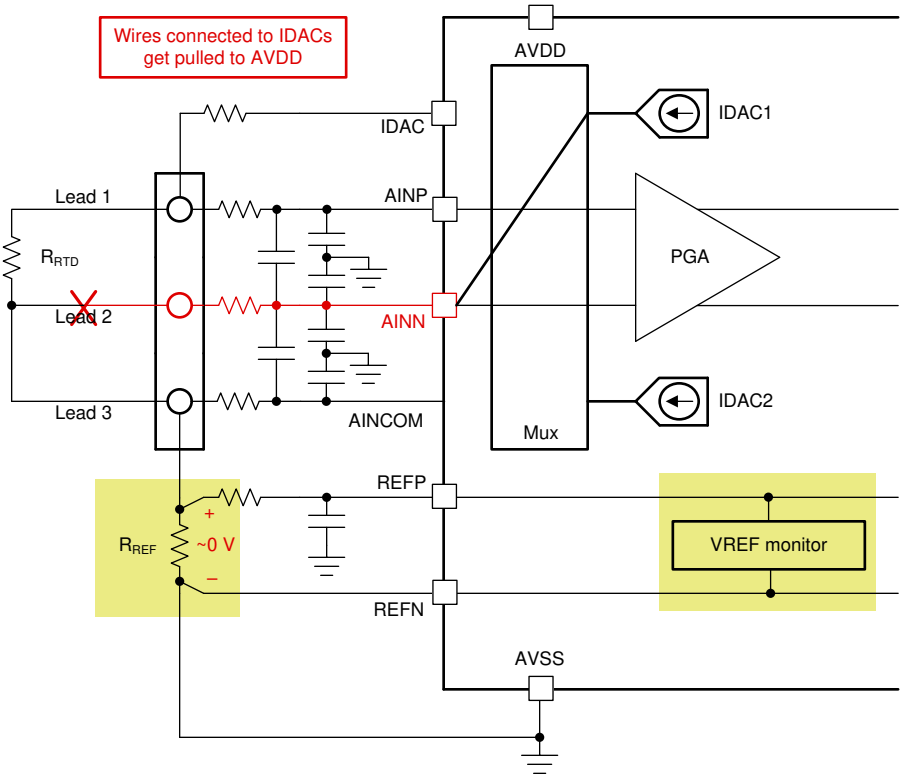


Figure 3-4. Diagnostic Measurement Checks if Lead 2 is Broken Using a Low-Side R_{REF}

In the low-side R_{REF} case, switch the IDAC current to flow through lead 2. Then, use the VREF monitor to indicate a fault just as if lead 1 or lead 3 is broken. The high-side R_{REF} case is more complicated, requiring a dedicated discussion as described in Section 3.2.1.1.1.

3.2.1.1.1 Detecting a Break in Lead 2 in a One-IDAC, 3-Wire RTD System Using a High-Side R_{REF}

The high-side R_{REF} case requires a diagnostic measurement with several configuration changes:

- Switch IDAC1 to output on lead 2 (AINN)
- Enable IDAC2 to output on lead 3 (AINCOM)
- Select the ADC internal VREF as the reference voltage source
- Select AINN and AINCOM as the measurement inputs (if necessary)
- Reduce the PGA gain (if necessary)
- Reduce the IDAC current magnitude (if necessary)

A different voltage reference source is required in order to check the measurement result for a fault because current cannot be forced through R_{REF} in this case. This action is dissimilar from all other diagnostic measurement routines, and care must be taken to ensure that the external VREF inputs are reselected when the diagnostic cycle completes.

Also, the last three steps are considered *if necessary* because the system may already be configured as such before the diagnostic measurement begins. For example, a one-IDAC, 3-wire RTD system always requires two measurements for lead resistance cancellation: first, between AINP and AINN and second, between AINN and AINCOM. Therefore, this diagnostic routine can be implemented after the second measurement when AINN and AINCOM are already selected, eliminating some communication and switching time. Moreover, the system may be measuring a large RTD (for example, a Pt1000), where the PGA gain is already set to 1 V/V and the IDAC current magnitude is small. These latter two steps are important for fault detection and are described in more detail later in this section.

Figure 3-5 shows how to implement the diagnostic measurement for a one-IDAC, 3-wire RTD system using a high-side R_{REF}.

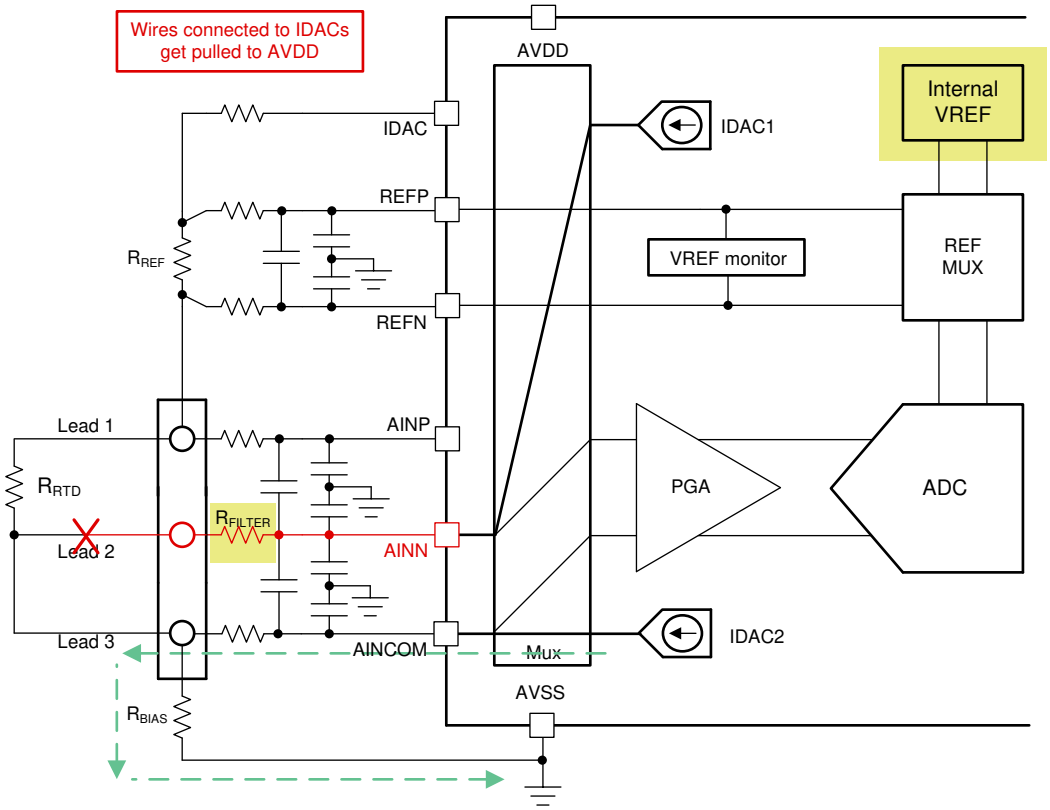


Figure 3-5. Diagnostic Measurement Checks if Lead 2 is Broken Using a High-Side R_{REF}

If lead 2 is not broken during this diagnostic measurement, expect the following voltages (given by Equation 1 and Equation 2) at the AINx pins:

$$V_{AINN} = IDAC1 \cdot (R_{FILTER} + R_{LEAD2} + R_{LEAD3} + R_{BIAS}) + IDAC2 \cdot R_{BIAS} \quad (1)$$

$$V_{AINCOM} = IDAC1 \cdot R_{BIAS} + IDAC2 \cdot (R_{FILTER} + R_{BIAS}) \quad (2)$$

The resulting differential voltage, $V_{IN\ (no\ wire\ break)}$, between AINN and AINCOM is given by Equation 3, assuming $R_{LEAD2} = R_{LEAD3}$, IDAC1 = IDAC2, and the R_{FILTER} resistors are well-matched:

$$V_{IN\ (no\ wire\ break)} = V_{AINN} - V_{AINCOM} = IDAC1 \cdot (2 \cdot R_{LEADx}) \quad (3)$$

If there is no fault to alter the circuit operation, $V_{IN\ (no\ wire\ break)}$ is a very small voltage because R_{LEADx} is typically less than 10 Ω in most cases.

Comparatively, a break in lead 2 eliminates the IDAC1 path to ground, causing IDAC1 to try to force current into the high-impedance analog input, AINN. The high impedance acts as an open circuit, raising the voltage level on AINN as the IDAC circuitry tries to maintain constant current. Eventually, this voltage is driven to the positive supply (AVDD) such that AINN is now approximately at AVDD as well.

Moreover, the voltage at AINCOM has actually reduced, because IDAC1 is no longer able to flow through R_{LEAD3} and R_{BIAS}, resulting in an absolute voltage at AINCOM as given by Equation 4:

$$V_{AINCOM\ (wire\ break)} = IDAC2 \cdot (R_{FILTER} + R_{BIAS}) \quad (4)$$

The resulting differential voltage, $V_{IN\ (wire\ break)}$, between AINN and AINCOM is given by Equation 5:

$$V_{IN\ (wire\ break)} = V_{AINN} - V_{AINCOM} = AVDD - IDAC2 \cdot (R_{FILTER} + R_{BIAS}) \quad (5)$$

Assuming that a small IDAC2 magnitude is chosen as per the configuration changes discussed at the beginning of this section, $V_{IN(wire\ break)}$ is significantly larger than $V_{IN(no\ wire\ break)}$ and therefore easy to detect. In order to quantify what is meant by a *small IDAC2 magnitude*, consider the AVDD voltage as well as the size of R_{FILTER} and R_{BIAS} in the system, which are typically on the order of 1 kΩ to 5 kΩ each. For example, if AVDD = 5 V, R_{FILTER} = 5 kΩ, and R_{BIAS} = 2 kΩ, selecting an IDAC magnitude of 100 µA is a good starting point. Assuming that R_{LEADx} = 10 Ω, these values can be entered into Equation 6 and Equation 7 to determine if the results clearly indicate when a fault has occurred:

$$V_{IN\ (no\ wire\ break)} = IDAC1 \cdot (2 \cdot R_{LEADx}) = 100\ \mu A \cdot 2 \cdot 10\ \Omega = 0.002\ V \quad (6)$$

$$V_{IN\ (wire\ break)} = AVDD - IDAC2 \cdot (R_{FILTER} + R_{BIAS}) = 5\ V - 100\ \mu A \cdot (5\ k\Omega + 2\ k\Omega) = 4.3\ V \quad (7)$$

For this example, set the PGA gain to 1 V/V in order to measure $V_{IN\ (wire\ break)}$ without saturating the amplifier. The specific gain required for the system ultimately depends on the different resistance values, AVDD, and the IDAC current magnitude chosen, so take care to select these values appropriately.

3.2.1.2 Wire-Break Detection Summary for a One-IDAC, 3-Wire RTD System

Table 3-2 and Table 3-3 summarize the wire-break detection method and expected results for all wire-break conditions using a one-IDAC, 3-wire RTD system with a low-side and high-side R_{REF}, respectively.

Table 3-2. Wire-Break Detection Summary for One-IDAC, 3-Wire RTD Systems Using a Low-Side R_{REF}

Lead 1	Lead 2	Lead 3	Wire-Break Detection Method and Result
Connected	Connected	Broken	• VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Connected	• Set IDAC to channel connected to lead 2 • VREF monitor → VREF voltage ≈ 0 V
Broken	Connected	Connected	• VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Broken	
Broken	Connected	Broken	
Broken	Broken	Connected	
Broken	Broken	Broken	

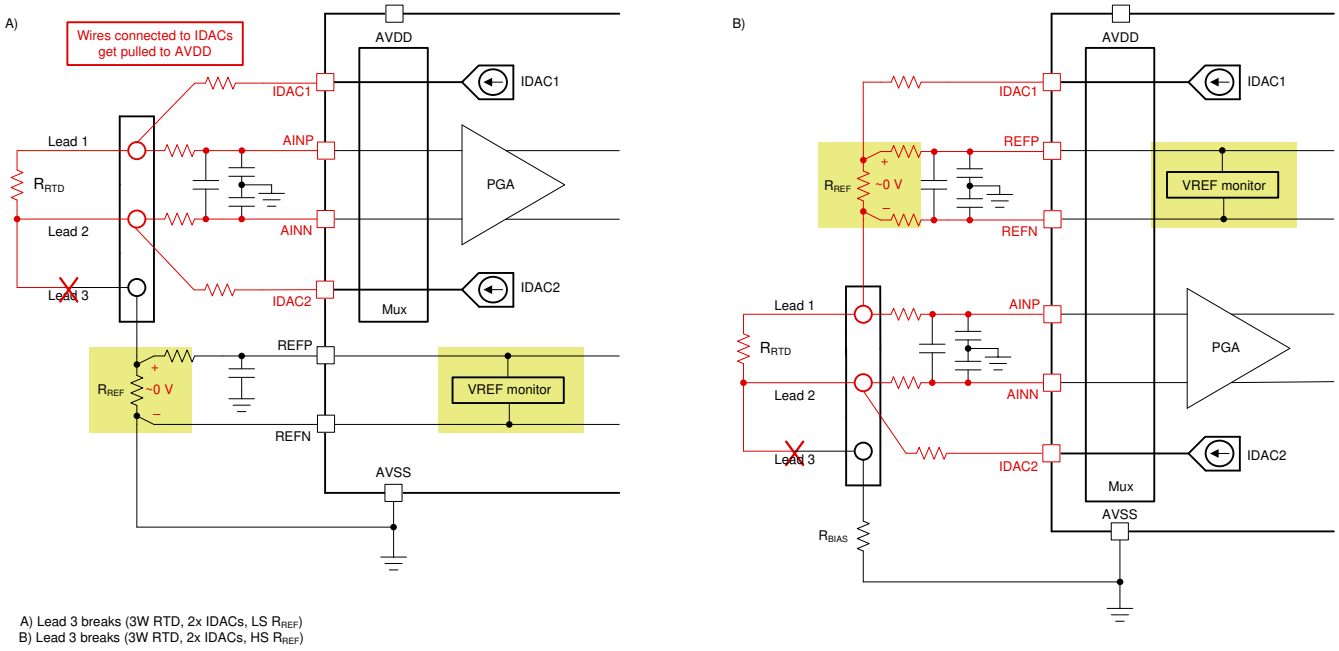
Table 3-3. Wire-Break Detection Summary for One-IDAC, 3-Wire RTD Systems Using a High-Side R_{REF}

Lead 1	Lead 2	Lead 3	Wire-Break Detection Method and Result
Connected	Connected	Broken	• VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Connected	• Set IDAC1 to lead 2 and IDAC 2 to Lead 3 • Select internal VREF • Change AINx, gain, IDAC magnitude (if necessary) • Check measurement result → large value indicates a fault
Broken	Connected	Connected	• VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Broken	
Broken	Connected	Broken	
Broken	Broken	Connected	
Broken	Broken	Broken	

3.2.2 Wire-Break Detection in a Two-IDAC, 3-Wire RTD System

Many of the same techniques employed in the previous sections can help identify wire breaks in a two-IDAC, 3-wire RTD system, though there are some corner cases that require special attention. These cases are described in Section 3.2.2.1 (low-side R_{REF}) and Section 3.2.2.2 (high-side R_{REF}).

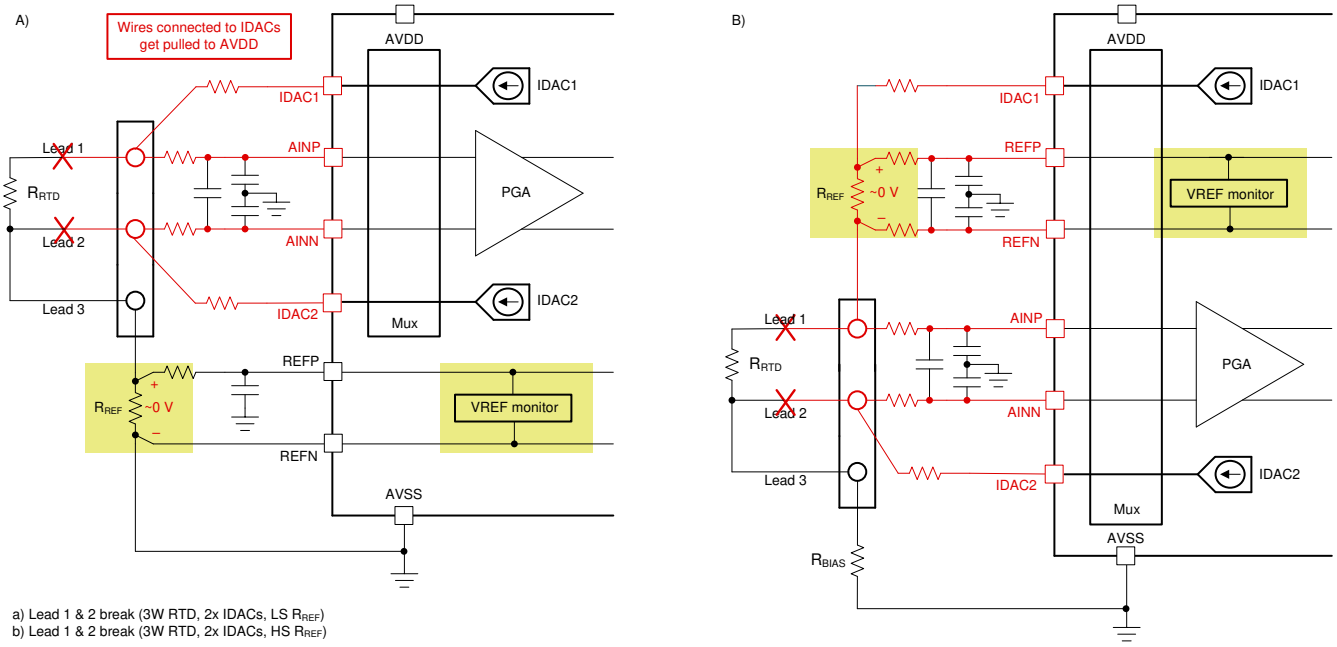
Regardless if a low-side or high-side R_{REF} is being used, a break in lead 3 automatically eliminates the IDAC path to ground and results in a VREF monitor fault. Figure 3-6 shows how this break occurs in a low-side (left) and high-side (right) R_{REF} configuration. This result is true if any other lead is also broken in addition to lead 3.



A) Lead 3 breaks (3W RTD, 2x IDACs, LS R_{REF})
B) Lead 3 breaks (3W RTD, 2x IDACs, HS R_{REF})

Figure 3-6. VREF Monitor Fault Detected if Lead 3 Breaks in a Two-IDAC, 3-Wire RTD System Using a Low-Side (Left) and High-Side (Right) R_{REF}

Similarly, if both lead 1 and lead 2 break in either the low-side or high-side R_{REF} configuration, neither IDAC has a path to ground and the result is a VREF monitor fault. Figure 3-7 illustrates how this break occurs in a low-side (left) and high-side (right) R_{REF} configuration.



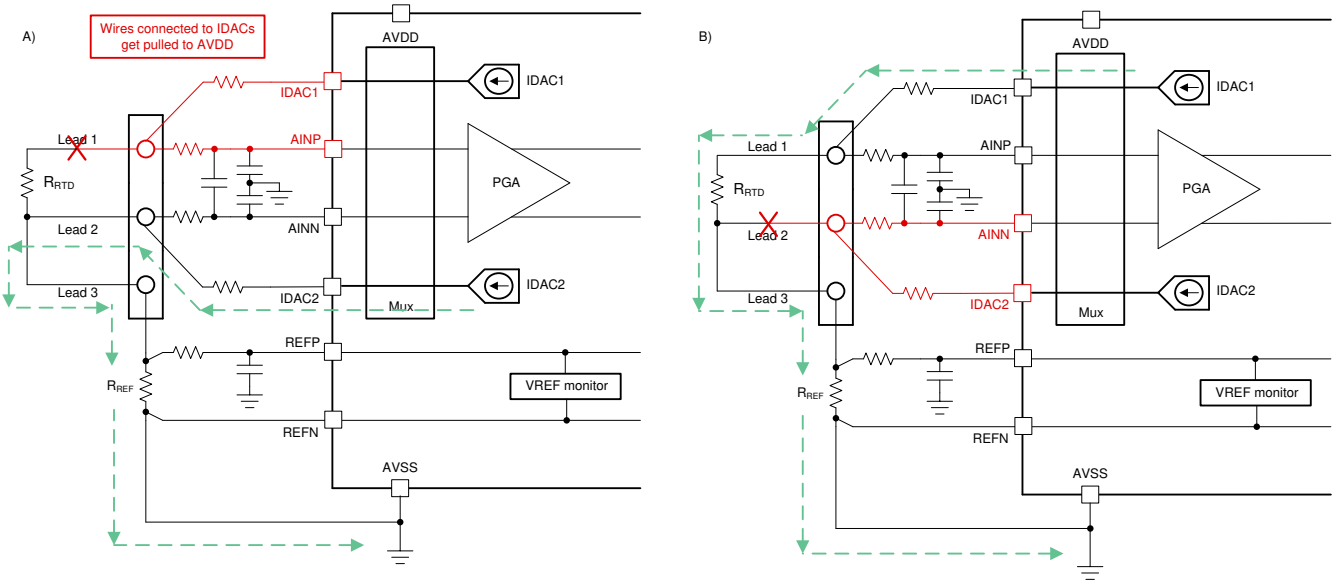
a) Lead 1 & 2 break (3W RTD, 2x IDACs, LS R_{REF})
b) Lead 1 & 2 break (3W RTD, 2x IDACs, HS R_{REF})

Figure 3-7. VREF Monitor Fault Detected if Lead 1 and Lead 2 Break in a Two-IDAC, 3-Wire RTD System Using a Low-Side (Left) and High-Side (Right) R_{REF}

The challenge in a two IDAC, 3-wire RTD system stems from a break in lead 1 ***or*** lead 2. In these cases, one IDAC still has a path to ground, making detection less simple. Moreover, the detection schemes differ depending on if a low-side or high-side R_{REF} configuration is used.

3.2.2.1 Detecting Lead 1 or 2 breaks in a two IDAC, 3-wire RTD system using a low-side R_{REF}

In the low-side R_{REF} configuration, a break in lead 1 or lead 2 eliminates the path to ground for one IDAC. However, the second IDAC current still flows through R_{REF} such that a VREF monitor fault is unlikely. Figure 3-8 shows this scenario.



a) Lead 1 breaks (3W RTD, 2x IDACs, LS R_{REF})
b) Lead 2 breaks (3W RTD, 2x IDACs, LS R_{REF})

Figure 3-8. Lead 1 (Left) or Lead 2 (Right) Breaks in a Two-IDAC, 3-Wire RTD System Using a Low-Side R_{REF}

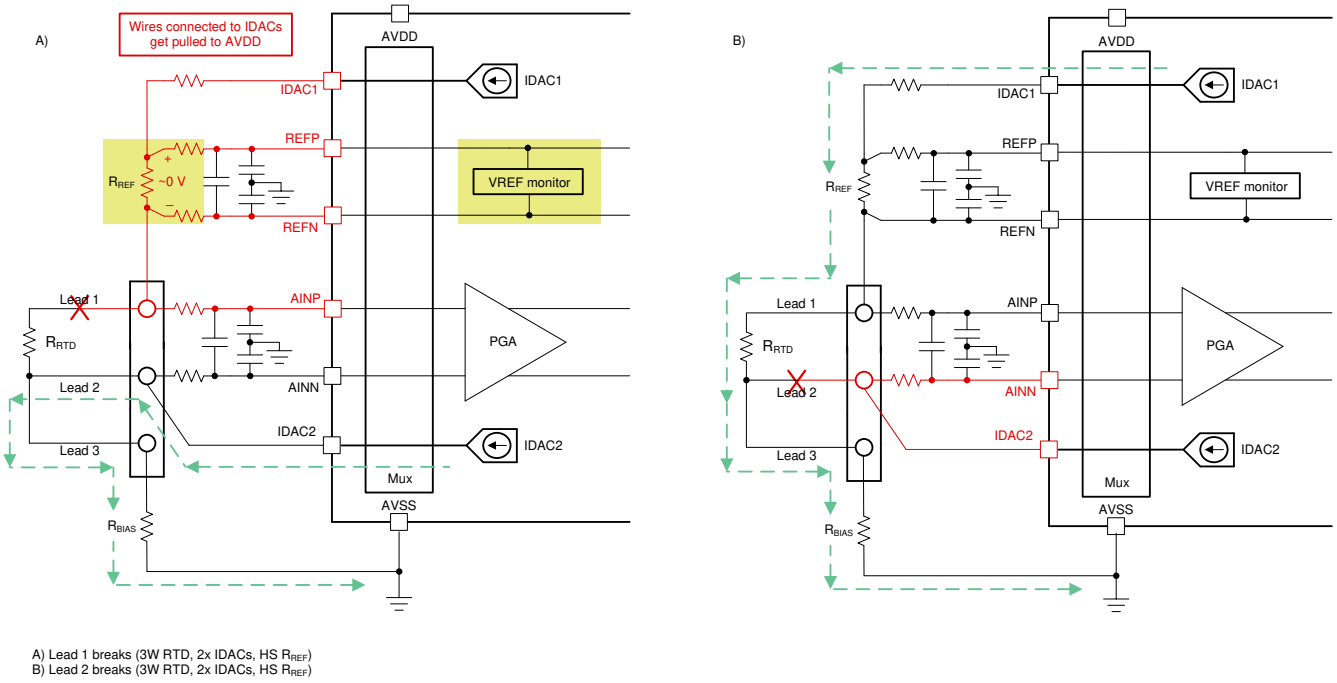
If either lead breaks in the configurations depicted in Figure 3-8, the voltage across R_{REF} is reduced by one-half compared to normal operation. However, this reduction may still not be sufficient to trip the VREF monitor in all cases and for all ADCs.

Instead, a diagnostic measurement is required, similar to a lead 2 break in the one-IDAC, 3-wire RTD system. And similar to any diagnostic measurement that interrupts the precision RTD measurement, choose how often to interleave diagnostics by balancing increased latency with the required system response time to a fault condition.

In the case of the two-IDAC, 3-wire RTD system using a low-side R_{REF}, the diagnostic measurement is fairly straightforward: turn off the IDAC that is still providing current to R_{REF}, which in turn trips the VREF monitor. For example, to detect a fault on lead 1 (Figure 3-8a), turn off IDAC2. To detect a fault on lead 2 (Figure 3-8b), turn off IDAC1. In both cases, the VREF monitor can detect a fault because no current flows across R_{REF}.

3.2.2.2 Detecting Lead 1 or 2 Breaks in a Two-IDAC, 3-Wire RTD System Using a High-Side R_{REF}

In the high-side R_{REF} configuration, only one IDAC current flows through R_{REF} under normal operating conditions, leading to distinct fault detection schemes depending on which lead breaks. Figure 3-9 shows how the current flows differently if lead 1 breaks (left) versus lead 2 (right).



A) Lead 1 breaks (3W RTD, 2x IDACs, HS R_{REF})
B) Lead 2 breaks (3W RTD, 2x IDACs, HS R_{REF})

Figure 3-9. Lead 1 (Left) or Lead 2 (Right) Breaks in a Two-IDAC, 3-Wire RTD System Using a High-Side R_{REF}

As shown in Figure 3-9a, the VREF monitor detects a break in lead 1 in the high-side R_{REF} configuration. The VREF monitor is tripped in this case because the break in lead 1 eliminates the path to ground for IDAC1 such that there is a near-zero voltage across R_{REF}. The current from IDAC2 still flows through R_{BIAS} to ground, but does not impact the result observed by the VREF monitor.

A break in lead 2 is not detectable by the VREF monitor in the high-side R_{REF} configuration. As Figure 3-9b shows, the IDAC1 current still flows through R_{REF} such that the VREF monitor does not indicate a fault. Instead, use a change in the measurement result to detect a break in lead 2.

Under normal conditions in a two-IDAC, 3-wire RTD system using a high-side R_{REF}, expect the following voltages (given by Equation 8 and Equation 9) at the AINx pins:

$$V_{AINP\ (no\ wire\ break)} = IDAC1 \cdot (R_{RTD} + R_{LEAD1} + R_{LEAD3} + R_{BIAS}) + IDAC2 \cdot (R_{LEAD3} + R_{BIAS}) \quad (8)$$

$$V_{AINN\ (no\ wire\ break)} = IDAC1 \cdot (R_{LEAD3} + R_{BIAS}) + IDAC2 \cdot (R_{LEAD2} + R_{LEAD3} + R_{BIAS}) \quad (9)$$

The resulting differential voltage, $V_{IN\ (no\ wire\ break)}$, between AINP and AINN is given by Equation 10, assuming $R_{LEAD1} = R_{LEAD2} = R_{LEAD3}$ and IDAC1 = IDAC2:

$$V_{IN\ (no\ wire\ break)} = V_{AINP} - V_{AINN} = IDAC1 \cdot R_{RTD} \quad (10)$$

Therefore, without a fault to alter the circuit operation, the voltage at AINP is always greater than AINN because the IDAC current only flows in one direction. As a result, normal operating conditions always yield a positive output code.

Comparatively, a break in lead 2 eliminates the path to ground for IDAC2, forcing the IDAC2 current into the high-impedance analog input, AINN. The high impedance acts as an open circuit, raising the voltage level on AINN as the IDAC circuitry tries to maintain constant current. Eventually, this voltage is driven to the positive supply (AVDD) such that AINN is now approximately at AVDD as well.

Moreover, the voltage at AINP has actually reduced because IDAC2 is no longer able to flow through R_{LEAD3} and R_{BIAS}, resulting in an absolute voltage at AINP given by Equation 11:

$$V_{AINP(wire\ break)} = IDAC1 \cdot (R_{RTD} + R_{LEAD1} + R_{LEAD3} + R_{BIAS}) \quad (11)$$

If AINN is pulled to AVDD and AINP is reduced in magnitude, $V_{AINN\ (wire\ break)}$ is greater than $V_{AINP\ (wire\ break)}$, resulting in a negative output code.

This diagnostic routine is very similar to the one employed in Section 3.2.1.1.1 for the one-IDAC, 3-wire RTD system using a high-side R_{REF}, though in this case there is no need to switch to the ADC internal reference or change the IDAC current magnitude. In fact, neither detection scheme in the two-IDAC, 3-wire RTD system using a high-side R_{REF} actually requires a separate diagnostic measurement, allowing wire-break detection to occur without interrupting the precision RTD measurement.

3.2.2.3 Wire-Break Detection Summary for a Two-IDAC, 3-Wire RTD System

Table 3-4 and Table 3-5 summarize the wire-break detection method and expected results for all wire-break conditions using a two-IDAC, 3-wire RTD system with a low-side and high-side R_{REF}, respectively.

Table 3-4. Wire-Break Detection Summary for Two-IDAC, 3-Wire RTD Systems Using a Low-Side R_{REF}

Lead 1	Lead 2	Lead 3	Wire-Break Detection Method and Result
Connected	Connected	Broken	• VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Connected	• Disable IDAC1 (connected to lead 1) • VREF monitor → VREF voltage ≈ 0 V
Broken	Connected	Connected	• Disable IDAC2 (connected to lead 2) • VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Broken	• VREF monitor → VREF voltage ≈ 0 V
Broken	Connected	Broken	
Broken	Broken	Connected	
Broken	Broken	Broken	

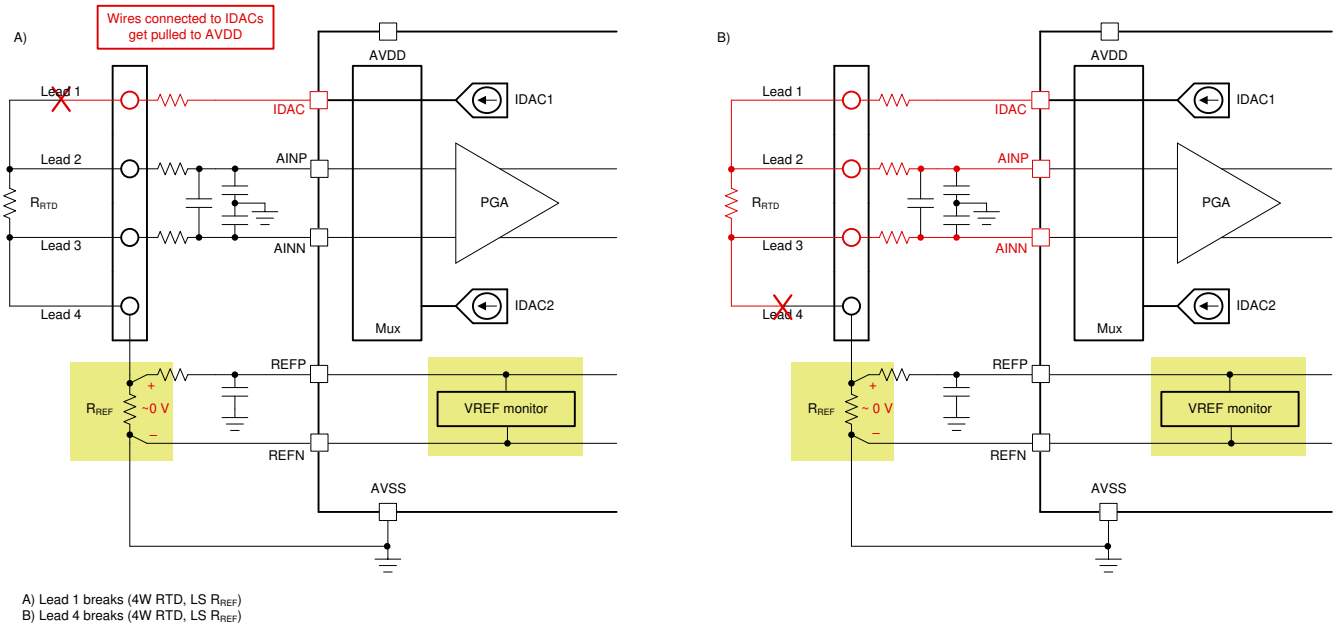
Table 3-5. Wire-Break Detection Summary for Two-IDAC, 3-Wire RTD Systems Using a High-Side R_{REF}

Lead 1	Lead 2	Lead 3	Wire-Break Detection Method and Result
Connected	Connected	Broken	• VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Connected	• IDAC current pulls AINN to AVDD, so $V_{AINN} > V_{AINP}$ and $V_{IN} < 0$ V
Broken	Connected	Connected	• VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Broken	
Broken	Connected	Broken	
Broken	Broken	Connected	
Broken	Broken	Broken	

3.3 Wire-Break Detection in a 4-Wire RTD System

Four-wire RTDs are the most accurate configuration because they do not suffer from the challenges inherent to the 3-wire RTD implementations: multiple measurements in the case of the one-IDAC system, or mismatched current sources in the case of the two-IDAC systems. As a result, 4-wire RTDs are also the most expensive sensors and consume the most PCB space because they require four terminals. Four-wire RTDs are generally used where temperature measurement accuracy is the most critical system parameter.

Similar to the 3-wire RTD fault detection methods, the VREF monitors can be used to detect the majority of the wire breaks in a 4-wire RTD system. Under normal operating conditions, any combination of wire breaks that include a break in lead 1 or lead 4 always eliminates the path to ground for the IDAC, resulting in a fault detectable by the VREF monitor. Figure 3-10 shows this result in a low-side R_{REF} configuration, though the same detection scheme can be used for a high-side R_{REF}.



A) Lead 1 breaks (4W RTD, LS R_{REF})
B) Lead 4 breaks (4W RTD, LS R_{REF})

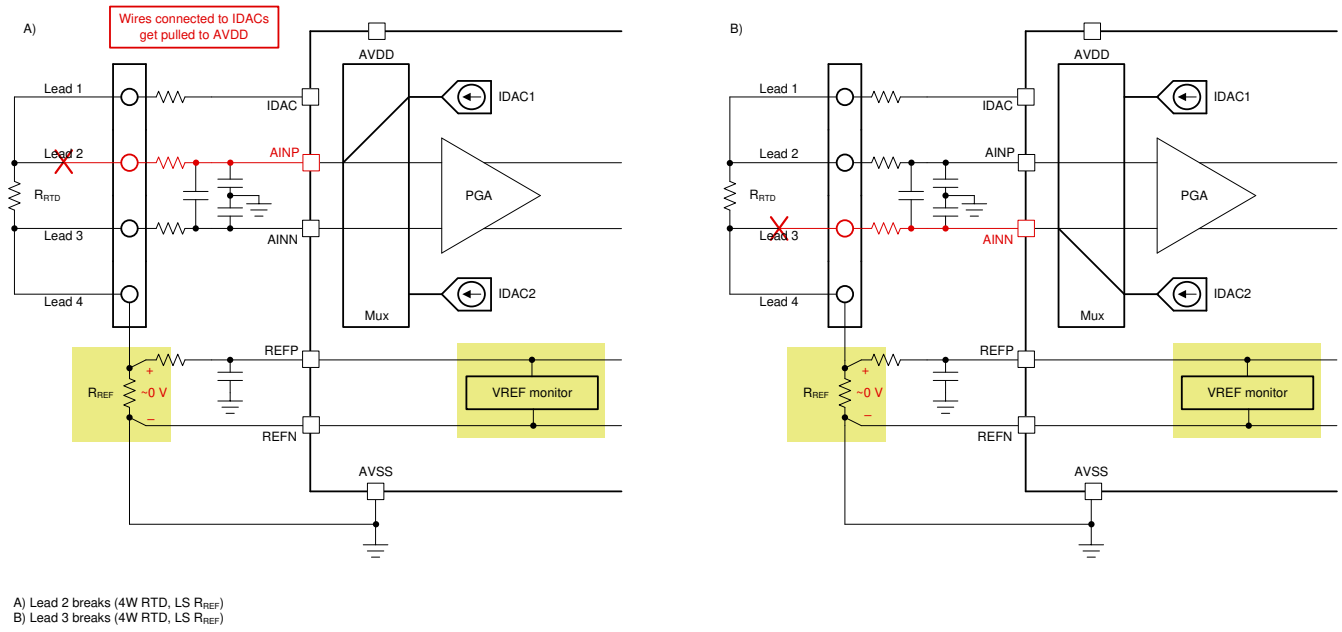
Figure 3-10. Lead 1 (Left) and Lead 4 (Right) Breaks in a 4-Wire RTD System

The only cases where the VREF monitor does not detect a wire break in a 4-wire RTD system is if ***only*** lead 2, lead 3, or both lead 2 and lead 3 break. In these cases, a wire break likely causes the ADC output to deviate from the expected value, but the cause cannot be assumed to be a wire break as opposed to some other system anomaly.

Therefore, perform a diagnostic measurement routine using the IDACs in the ADC similar to those described in the previous sections. Furthermore, as previously described, the routine is different depending if a low-side or high-side R_{REF} configuration is used.

3.3.1 Detecting Lead 2 and Lead 3 Breaks in a 4-Wire RTD System Using a Low-Side R_{REF}

The diagnostic routine used in the 4-wire RTD, low-side R_{REF} case is similar to the method described in Section 3.2.2.1: reroute the IDAC pins to drive current through lead 2 and lead 3, then check the VREF monitor. Figure 3-11 shows how current flows when performing these diagnostic measurements, assuming that lead 2 or lead 3 are broken.



A) Lead 2 breaks (4W RTD, LS R_{REF})
B) Lead 3 breaks (4W RTD, LS R_{REF})

Figure 3-11. Diagnostic Measurement Checks if Lead 2 (Left) and Lead 3 (Right) are Broken in a 4-Wire RTD System Using a Low-Side R_{REF}

The main difference between the previous diagnostic measurements in the 3-wire RTD system and the 4-wire RTD case is that the latter requires two steps to fully determine if both lead 2 and lead 3 are still intact. In other words, two measurement steps must be implemented as part of the diagnostic cycle, further increasing the system latency compared to the 3-wire RTD case. Therefore, this increased latency must be balanced with the required system response time to a fault condition when choosing how often to interleave diagnostic measurements.

3.3.2 Detecting Lead 2 and Lead 3 Breaks in a 4-Wire RTD System Using a High-Side R_{REF}

Compared to using a low-side R_{REF}, identifying a break in lead 2 or lead 3 is more difficult in a 4-wire RTD system using a high-side R_{REF}. The main challenge stems from an inability to force current from lead 2 or lead 3 through R_{REF} to trip the VREF monitors. Instead, use a similar diagnostic routine as detailed in Section 3.2.1.1.1. This routine involves the following configuration changes:

- Switch IDAC1 to output on lead 2 (AINP)
- Switch IDAC2 to output on lead 3 (AINN)
- Select the ADC internal VREF as the reference voltage source
- Reduce the PGA gain (if necessary)
- Reduce the IDAC current magnitude (if necessary)

Just as in Section 3.2.1.1.1, the diagnostic cycle requires a different reference source to check the measurement result for a fault because current cannot be forced through R_{REF} in this case. Take care to ensure that the external VREF inputs are reselected when the diagnostic cycle completes.

Also, the last two steps are considered *if necessary* because the system may already be configured as such before the diagnostic measurement begins. For example, the system may be measuring a large RTD (for example, Pt1000), where the PGA gain is already set to 1 V/V and the IDAC current magnitude is small. These latter two steps are important for fault detection and are described in more detail at the end of Section 3.2.1.1.1.

Figure 3-12 shows how to implement the diagnostic measurement for a 4-wire RTD system using a high-side R_{REF}. Lead 4 is assumed to be intact in this case because the VREF monitor is not tripped.

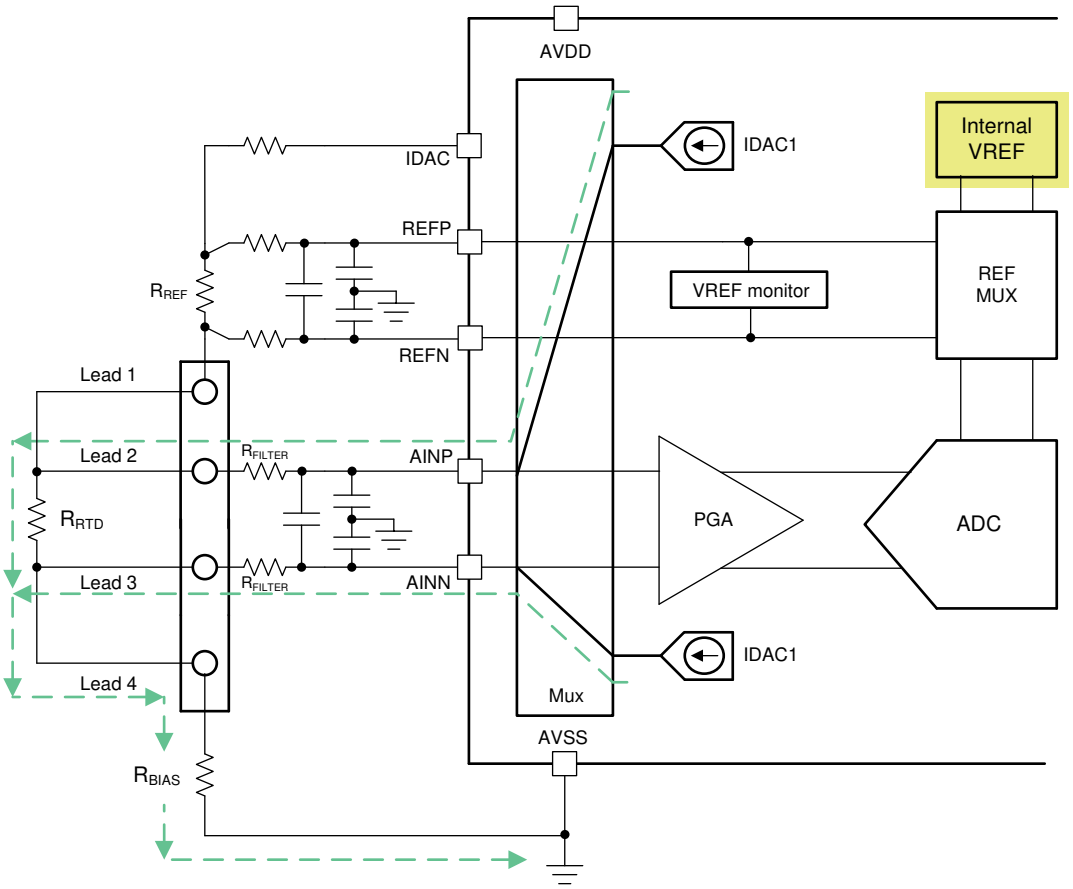


Figure 3-12. Diagnostic Measurement Checks if Lead 2 and Lead 3 are Broken in a 4-Wire RTD System Using a High-Side R_{REF}

Determine if any faults have occurred by monitoring the conversion result during this diagnostic measurement cycle and interpreting the ADC output as follows:

- If both leads are intact, the conversion result is $V_{IN} = V_{AINP} – V_{AINN} = IDAC1 \cdot R_{RTD}$, assuming perfectly matched filter resistors. This result is equivalent to just the voltage across the RTD, and is effectively implementing a two-IDAC, 3-wire RTD system that uses the internal voltage reference instead of a ratiometric reference configuration.
- If lead 2 is broken, IDAC1 pulls AINP to AVDD and IDAC2 drives AINN to $IDAC2 \cdot (R_{FILTER} + R_{LEAD3} + R_{LEAD4} + R_{BIAS})$. The resulting output code is a large positive value that is easy to distinguish from the voltage across the RTD.
- If lead 3 is broken, IDAC1 drives AINP to $IDAC1 \cdot (R_{FILTER} + R_{LEAD2} + R_{RTD} + R_{LEAD4} + R_{BIAS})$ and IDAC2 pulls AINN to AVDD. The resulting output code is a large negative value that is easy to distinguish from the voltage across the RTD.
- If both leads are broken, IDAC1 pulls AINP to AVDD and IDAC2 pulls AINN to AVDD as well. With AINP ≈ AINN, the resulting output code is approximately 0, indicating a fault.

See the end of Section 3.2.1.1.1 to understand why a small IDAC current magnitude and reduced PGA gain are required for this diagnostic measurement, as well as guidelines for choosing these values for the system.

3.3.3 Wire-Break Detection Summary for a 4-Wire RTD System

Table 3-6 and Table 3-7 summarize the wire-break detection method and expected results for all wire-break conditions using a 4-wire RTD system with a low-side and high-side R_{REF}, respectively.

Table 3-6. Wire-Break Detection Summary for 4-Wire RTD Systems Using a Low-Side R_{REF}

Lead 1	Lead 2	Lead 3	Lead 4	Wire-Break Detection Method and Result
Connected	Connected	Connected	Broken	• VREF monitor → VREF voltage ≈ 0 V
Connected	Connected	Broken	Connected	• Set IDAC to lead 3 • VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Connected	Connected	• Set IDAC to lead 2 • VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Broken	Connected	• Covered by lead 2, lead 3 cases
Broken	Connected	Connected	Connected	• VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Connected	Broken	
Connected	Connected	Broken	Broken	
Broken	Connected	Connected	Broken	
Broken	Connected	Broken	Connected	
Broken	Broken	Connected	Connected	
Connected	Broken	Broken	Broken	
Broken	Connected	Broken	Broken	
Broken	Broken	Connected	Broken	
Broken	Broken	Broken	Connected	
Broken	Broken	Broken	Broken	

Table 3-7. Wire-Break Detection Summary for 4-Wire RTD Systems Using a High-Side R_{REF}

Lead 1	Lead 2	Lead 3	Lead 4	Wire-Break Detection Method and Result
Connected	Connected	Connected	Broken	• VREF monitor → VREF voltage ≈ 0 V
Connected	Connected	Broken	Connected	• Set IDAC1 to lead 2 and IDAC 2 to lead 3 • Select internal VREF • Change AINx, gain, IDAC magnitude (if necessary) • Check conversion result
Connected	Broken	Connected	Connected	• See broken lead 3 case
Connected	Broken	Broken	Connected	
Broken	Connected	Connected	Connected	• VREF monitor → VREF voltage ≈ 0 V
Connected	Broken	Connected	Broken	
Connected	Connected	Broken	Broken	
Broken	Connected	Connected	Broken	
Broken	Connected	Broken	Connected	
Broken	Broken	Connected	Connected	
Connected	Broken	Broken	Broken	
Broken	Connected	Broken	Broken	
Broken	Broken	Connected	Broken	
Broken	Broken	Broken	Connected	
Broken	Broken	Broken	Broken	

4 Settling Time Considerations for RTD Wire-Break Detection

One practical challenge in implementing the wire-break detection schemes discussed in this document is settling time resulting from analog filters on the measurement and reference input channels. All RTD configurations described in this document include generic low-pass RC filters on both sets of inputs to reduce noise, prevent aliasing, and limit current into the inputs in case of an overvoltage event. These figures do not include component values because the amount of filtering required for a specific system can vary greatly. To learn more about this topic, reference this short application note that discusses a general process for selecting low-pass RC filter component values.

However, the component values selected for a design can have an impact on the overall system response time and therefore how quickly the circuit is able to respond to a fault. For example, Figure 4-1 shows how the IDAC current flows in a 2-wire RTD system with a low-side R_{REF}. Sample component values are included in this specific figure, though these values were chosen to help explain settling time challenges and do not necessarily follow best design practices.

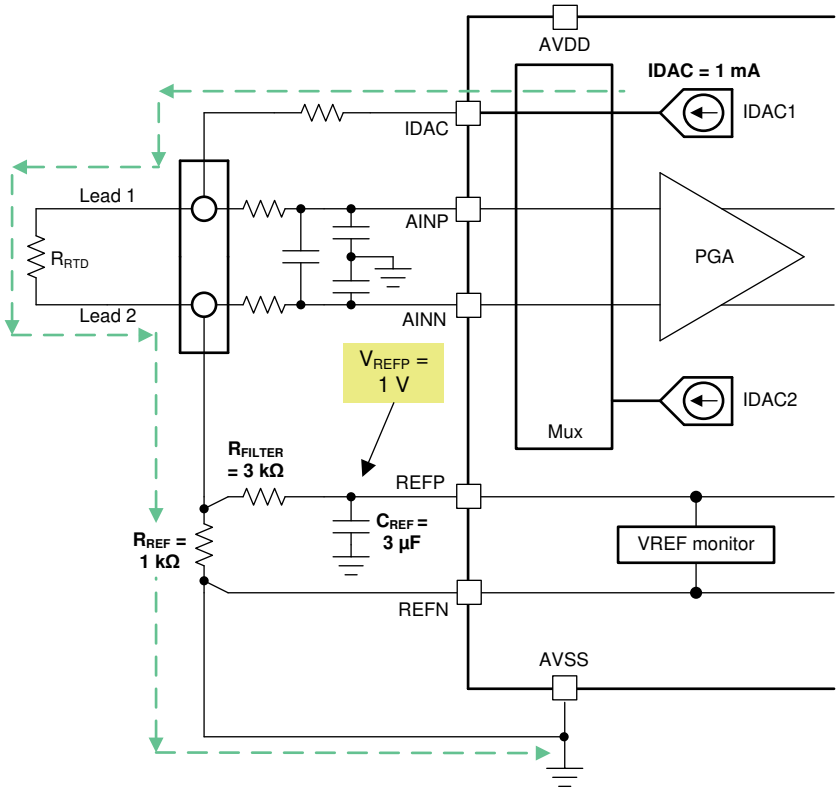


Figure 4-1. Voltage at REFP in a 2-Wire RTD During Normal Operation

Given the values shown in Figure 4-1, the voltage at REFP is equal to 1 V under normal operating conditions. When one of the RTD leads breaks, the IDAC current no longer flows through R_{REF} such that the voltage across R_{REF} is equal to 0 V, as illustrated in Figure 4-2.

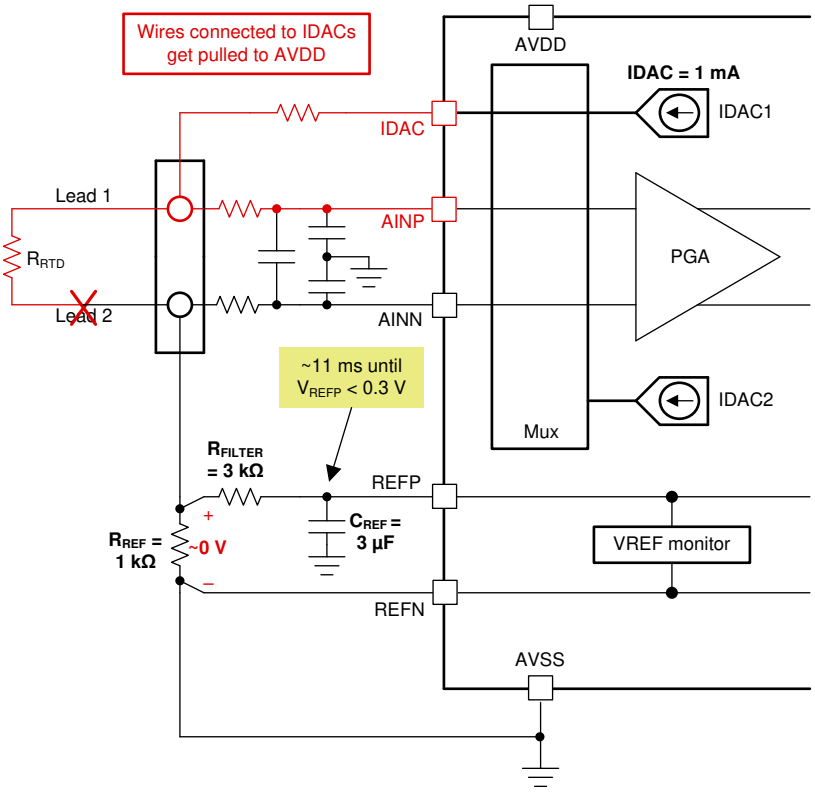


Figure 4-2. Extended Settling Time to Reach VREF Monitor Threshold Because of C_{REF} Discharge

As Figure 4-2 also shows, some time is required to discharge capacitor C_{REF} such that the voltage at REFP also drops to 0 V, or at least to a level that either trips the continuous VREF monitor or that can be accurately identified by the periodic VREF monitor. If the ADS124S08 is used in the system shown in Figure 4-2, approximately 11 milliseconds is required for V_{REFP} to drop below the 300-mV detection threshold specified by the continuous VREF monitor integrated into this ADC. If the ADC sample rate is 1 kSPS (1 ms per conversion nominal), the external analog filter cannot settle fast enough for the ADC to identify a fault within one conversion.

Although waiting multiple conversions to identify a fault may be acceptable in some cases, consider the challenges that can arise if this delay occurred during the diagnostic cycle for a 4-wire RTD using a low-side R_{REF} as described in Section 3.3.1. When switching the IDAC to lead 2 or lead 3 and checking the VREF monitor, the system can potentially have to wait ten conversions or more before a fault is identified. If the host controller is not set up to account for these delays, the system is not able to accurately and consistently detect RTD wire breaks.

Moreover, these settling time challenges can also be problematic when returning *from* a diagnostic measurement *back to* precision RTD measurements. If the IDACs are rerouted during the diagnostic cycle, large voltages can be present on the measurement and reference input capacitors that require multiple conversions to discharge. Again, if the host controller is not set up to account for these delays, the precision RTD measurement data can be invalid for several conversions.

Ultimately, consider the response time of any analog filtering on the measurement or reference inputs in order to design an effective RTD wire-break detection scheme.

5 Summary

Many ΔΣ ADCs integrate features that are useful for wire-break detection in sensing applications. This document demonstrates how to use just the integrated IDACs and VREF monitoring to detect all combinations of wire breaks for all common RTD configurations.

A How Integrated PGA Rail Detection Helps Identify Wire Breaks

Although wire-break detection can be implemented using IDACs and VREF monitoring as described throughout this document, some ADCs integrate additional features to make wire-break detection easier.

One such feature is PGA rail detection, which allows the user to detect if the PGA output (or input, in some cases) is operating too close to the supply rails. This feature can be used to identify wire breaks because AINP or AINN can be pulled to AVDD when the IDAC no longer has a path to ground, as shown in Figure A-1. This feature can be employed during a diagnostic measurement routine to more accurately determine which pin has broken.

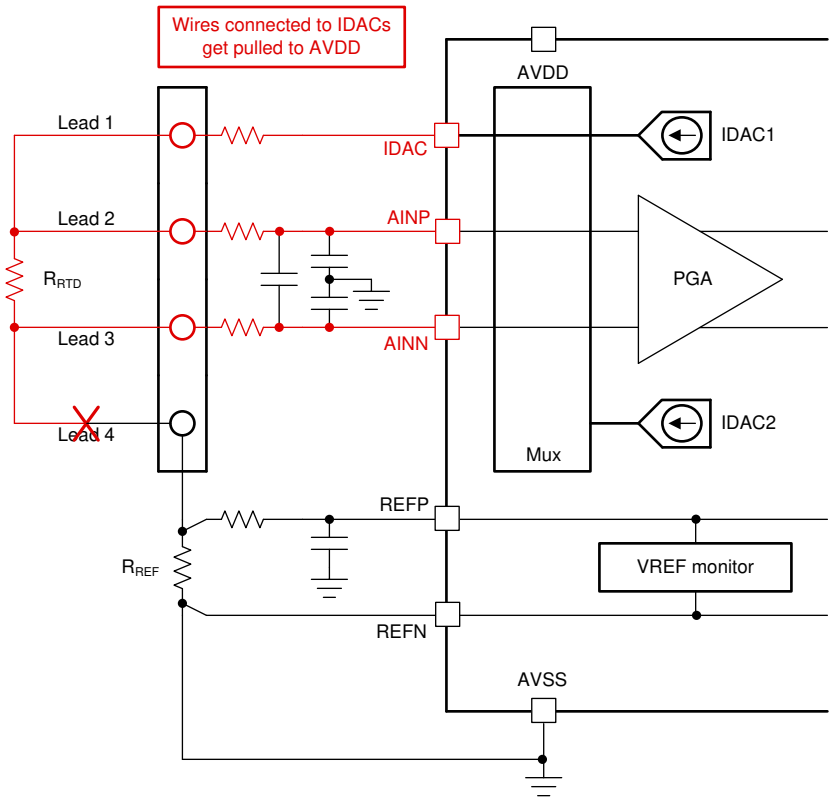


Figure A-1. PGA Rail Detection Identifies Overranged Inputs

The ADS124S08 is an example of an ADC that integrates PGA rail detection features. If the level of the ADS124S08 PGA output voltage exceeds AVDD – 0.15 V, or drops below AVSS + 0.15 V, the ADC sets a flag to indicate that the output has gone beyond the output range of the PGA. Each PGA output (OUTN and OUTP) can trigger an overvoltage or undervoltage flag, giving a total of four flags:

- FL_P_RAILP (bit 5 of the STATUS byte): V_{OUTP} has exceeded AVDD – 0.15 V
- FL_P_RAILN (bit 4 of the STATUS byte): V_{OUTP} dropped below AVSS + 0.15 V
- FL_N_RAILP (bit 3 of the STATUS byte): V_{OUTN} has exceeded AVDD – 0.15 V
- FL_N_RAILN (bit 2 of the STATUS byte): V_{OUTN} dropped below AVSS + 0.15 V

For more information about the PGA rail detection features in a specific ADC, see that ADC data sheet. Table A-1 can also be referenced for a quick comparison of available features integrated into the precision delta-sigma ADCs highlighted in Table 1-1.

Table A-1. Summary of PGA Rail Detection Features in Precision ΔΣ ADCs

Device	PGA Rail Detection Flags
ADS1120	N/A
ADS112C04	
ADS112U04	
ADS1220	
ADS122C04	
ADS122U04	
ADS114S06B	• PGA positive output (OUTP) is too close to AVDD • PGA positive output (OUTP) is too close to AVSS • PGA negative output (OUTN) is too close to AVDD • PGA negative output (OUTN) is too close to AVSS
ADS114S08B	
ADS114S06	
ADS114S08	
ADS124S06	
ADS124S08	
ADS125H02	• PGA positive input (INP) is too close to HVDD • PGA positive input (INP) is too close to HVSS • PGA negative input (INN) is too close to HVDD • PGA negative input (INN) is too close to HVSS • PGA positive output (OUTP) is too close to HVDD • PGA positive output (OUTP) is too close to HVSS • PGA negative output (OUTN) is too close to HVDD • PGA negative output (OUTN) is too close to HVSS
ADS1260	• PGA positive/negative output (OUTx) is too close to AVDD • PGA positive/negative output (OUTx) is too close to AVSS
ADS1261	
ADS1262	• PGA positive/negative output (OUTx) is too close to AVDD • PGA positive/negative output (OUTx) is too close to AVSS • PGA differential output > FS
ADS1263	

B Pseudo-Code for RTD Wire-Break Detection

The following sections include high-level code for determining a wire break in each different RTD configuration. In each case, VREF_MON = 1 indicates a fault detected by a continuous VREF monitor and CONV_RESULT indicates a data read of the inputs connected to AINx. By using a continuous VREF monitor, the code assumes that checking the VREF monitor status is not part of the diagnostic routine (unless explicitly mentioned). If a periodic VREF monitor is used instead, check the monitor status and run the diagnostic routine in the same cycle because the RTD measurement process must be interrupted either way.

B.1 Pseudo-Code for a 2-Wire RTD System (Low-Side or High-Side R_{REF})

```
Check STATUS byte

     If VREF_MON = 1     // Lead 1 OR Lead 2 OR both leads are broken
     Else                // No leads are broken
```

B.2 Pseudo-Code for a One-IDAC, 3-Wire RTD System (Low-Side or High-Side R_{REF})

```
Check STATUS byte

     If VREF_MON = 1          // Lead 1 AND/OR Lead 3 break, Lead 2 could also be broken
     Else                     // Lead 2 could be broken, run a diagnostic measurement

          // Diagnostic measurement routine:
          Set IDAC1 to Lead 2
          If RREF = HIGH_SIDE

               Set IDAC2 to Lead 3
               Select internal VREF
               Change config settings          // If necessary

                    If CONV_RESULT >> 0 V      // Lead 2 is broken
                    Else                       // Lead 2 is not broken

          Else If VREF_MON = 1                 // Lead 2 is broken
          Else                                 // Lead 2 is not broken
```

B.3 Pseudo-Code for a Two-IDAC, 3-Wire RTD System (Low-Side or High-Side R_{REF})

```
Check STATUS byte AND CONV_RESULT

     // Detects --> (Lead 3 breaks) OR (Lead 1 AND Lead 2 break) OR (Lead 1 breaks AND
     // RREF = HIGH_SIDE) OR (Lead 2 breaks AND RREF = HIGH_SIDE)
     If VREF_MON = 1 OR (CONV_RESULT < 0 V AND RREF = HIGH_SIDE)

     // Lead 1 OR 2 could be broken, run a diagnostic measurement
     Else

          // Diagnostic measurement routine - Step 1
          Disable IDAC connected to Lead 1
          If VREF_MON = 1                      // Lead 2 is broken
          Else                                 // Lead 2 is not broken

          // Diagnostic measurement routine - Step 2
          Disable IDAC connected to Lead 2
          If VREF_MON = 1                      // Lead 1 is broken
          Else                                 // Lead 1 is not broken
```

B.4 Pseudo-Code for a 4-Wire RTD System (Low-Side or High-Side R_{REF})

```
Check STATUS byte

     // Detects if ≥1x lead breaks except if only Lead 2 AND/OR Lead 3 break
     If VREF_MON = 1

     // Lead 2 AND/OR Lead 3 could be broken, run a diagnostic measurement
     Else

          // Diagnostic measurement routine:
          Connect IDAC1 to Lead 2 AND connect IDAC2 to Lead 3

          If CONV_RESULT = 0                    // Lead 2 AND Lead 3 are broken
          Else If CONV_RESULT >> RTD*IDAC

               If CONV_RESULT > 0               // Lead 2 is broken
               If CONV_RESULT < 0               // Lead 3 is broken

          Else                                  // Lead 2 AND Lead 3 are not broken
```

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