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APPLICATION BULLETIN
Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706
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MULTI-DDC112 BOARD DESIGN

By Jim Todsen and Dave Milligan

The DDC112 is capable of being daisy chained for use in systems with a large number of channels. To help in designing such a system, this application note describes the design of a multi-DDC112 DUT board that can be used with the standard evaluation fixture DEM-DDC112U-C. This DUT board contains eight DDC112s daisy chained together, creating a 16-channel DUT board. It connects to the PC Interface Board in the same way as the original single DDC112 DUT board included with the evaluation fixture. The standard software that ships with the evaluation board can then be used to collect data from all eight DDC112s by a simple modification to the setup configuration.

The multi-DDC112 DUT board described in this application note was built and tested to verify the design and PCB layout. However, it is currently not available as a standard product. The following discussions about this specific board can provide general guidelines for designing a multi-DDC112 system. The basic operation of the evaluation fixture is covered in detail in its own data sheet (LI-500) and in Application Bulletin AB-125, "Customizing the DDC112's Evaluation Fixture."

SCHEMATIC

Figure 1 shows the schematic diagram of the 8-DDC112 DUT board. It is a straightforward extension of the single-DDC112 DUT board. The same V_{REF} and digital buffering circuits are used. The daisy chain is built by connecting one DDC112's DOUT pin to the next DDC112's DIN pin. Pull-up resistors to V_{DD} should be used on DOUT. Bypass capacitors are used at every IC to help insure clean supplies and V_{REF}. As with the original DUT board, there are socket pins for resistors to be placed in series with the DDC112's inputs. Voltage sources can then be connected to these resistors using P2 and P4 to effectively generate input current signals. When using the series resistors, make sure to keep the resistor values high (typically 10MΩ or greater) and to also use high quality resistors such as Caddocks' MK632 family. Standard metal-film, especially carbon resistors, can introduce noise and non-linearities.

PCB LAYOUT

Table I summarizes the six layers used in the PCB. The artwork for each of the layers is shown at a 1:1 scale in Figures 2 through 7. The shields, layers 2 and 4, are identical and, therefore, only shown once (see Figure 4). All of the components are located on the top side.

LAYER	FIGURE	PURPOSE
Silk Screen	2	
1	3	Ground Plane
2	4	Shield
3	5	Input Traces
4	4	Shield
5	6	Analog and Digital Power, V_{REF}
6	7	Digital Traces

Table I. PCB Layer Map.

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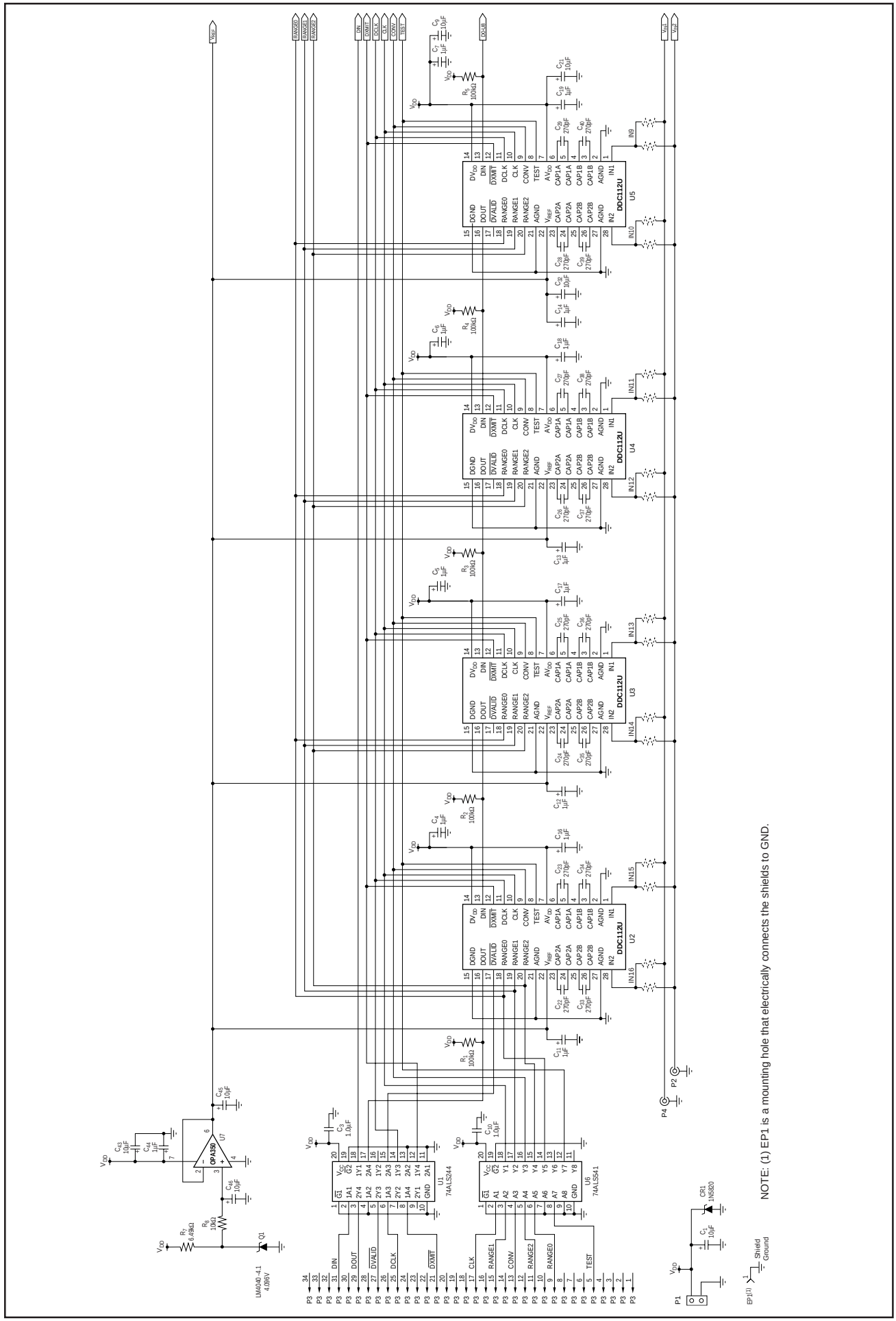

FIGURE 1a. Schematic Diagram.

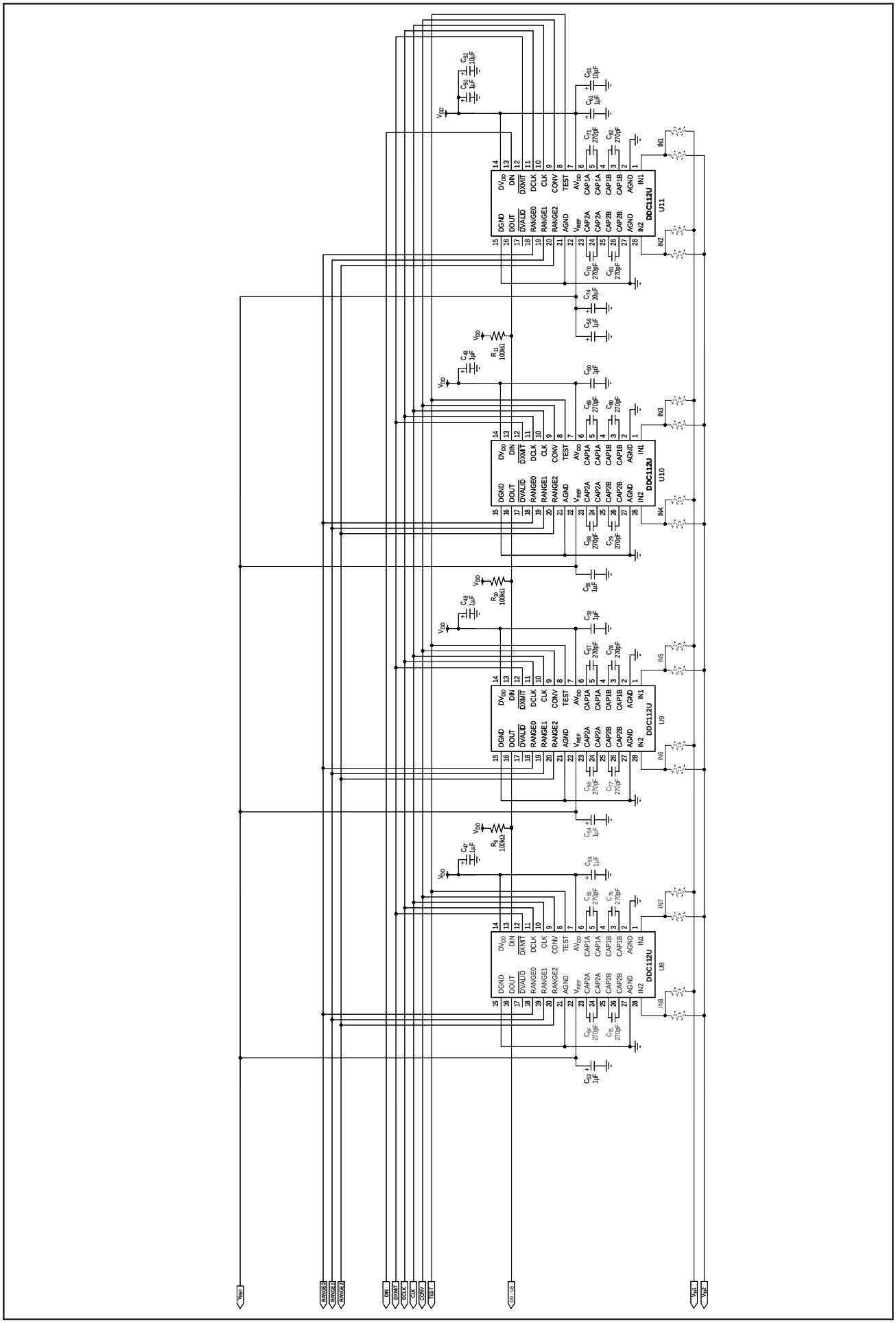

FIGURE 1b. Schematic Diagram (cont).

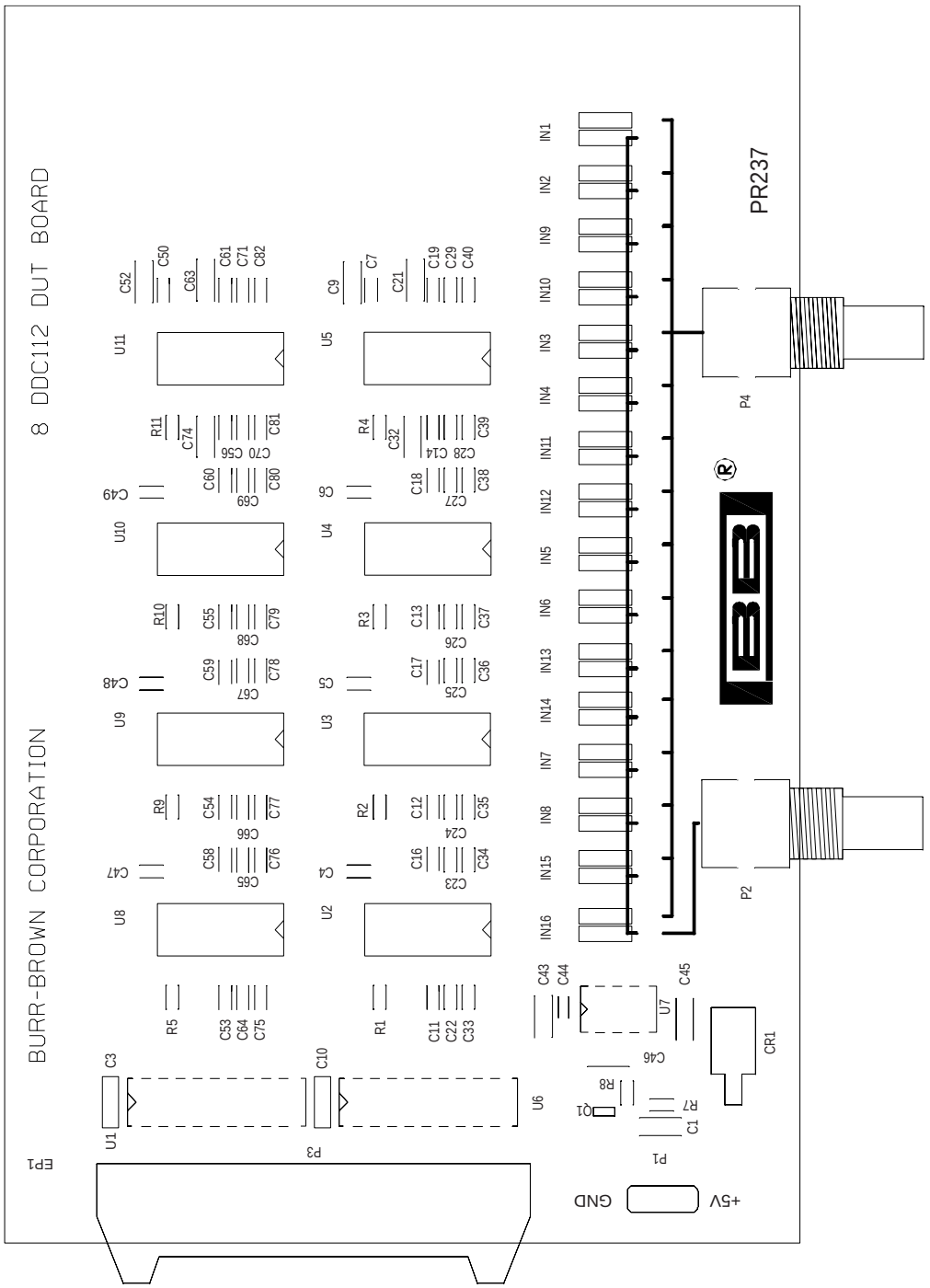

FIGURE 2. Top Side Silk Screen.

Layer 1: Ground Plane

A single ground plane is used. Placing this plane on top allows the DDC112's ground pins and bypass capacitors to tie directly to ground without the need for vias. In the evaluation fixture, all of the digital signals are synchronous with CLK (the system clock) and CONV and are much less likely to introduce noise into the DDC112's front-end integrators. For systems with asynchronous digital signals, a split ground plane for the DDC112 may better isolate these digital signals from the DDC112's front-end integrators.

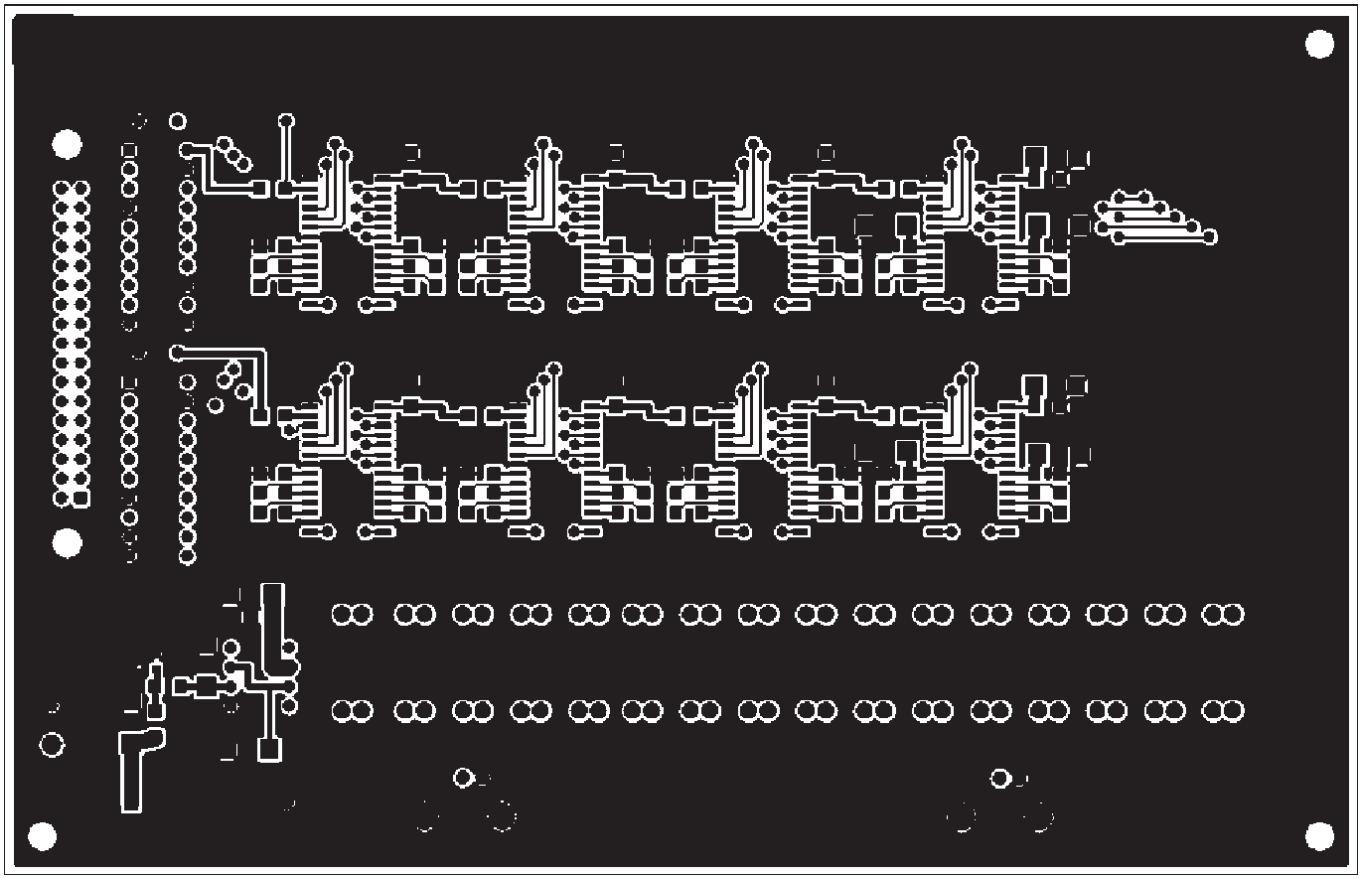

FIGURE 3. Layer 1: Ground Plane.

Layers 2 and 4: Shields

Shields tied to ground used both above and below the input traces help protect these critical lines. The top shield on layer 2 may not always be needed as layer 1's ground plane does provide some shielding, however, the top ground plane is broken by components and pads. If the top shield is not used, the input traces must be carefully routed to avoid running underneath the DDC112's digital pins, bypass caps, etc. Using a separate, more complete shield on layer 2 makes routing the input traces much easier. Both shields are tied to ground at only one place to prevent ground currents flowing through them.

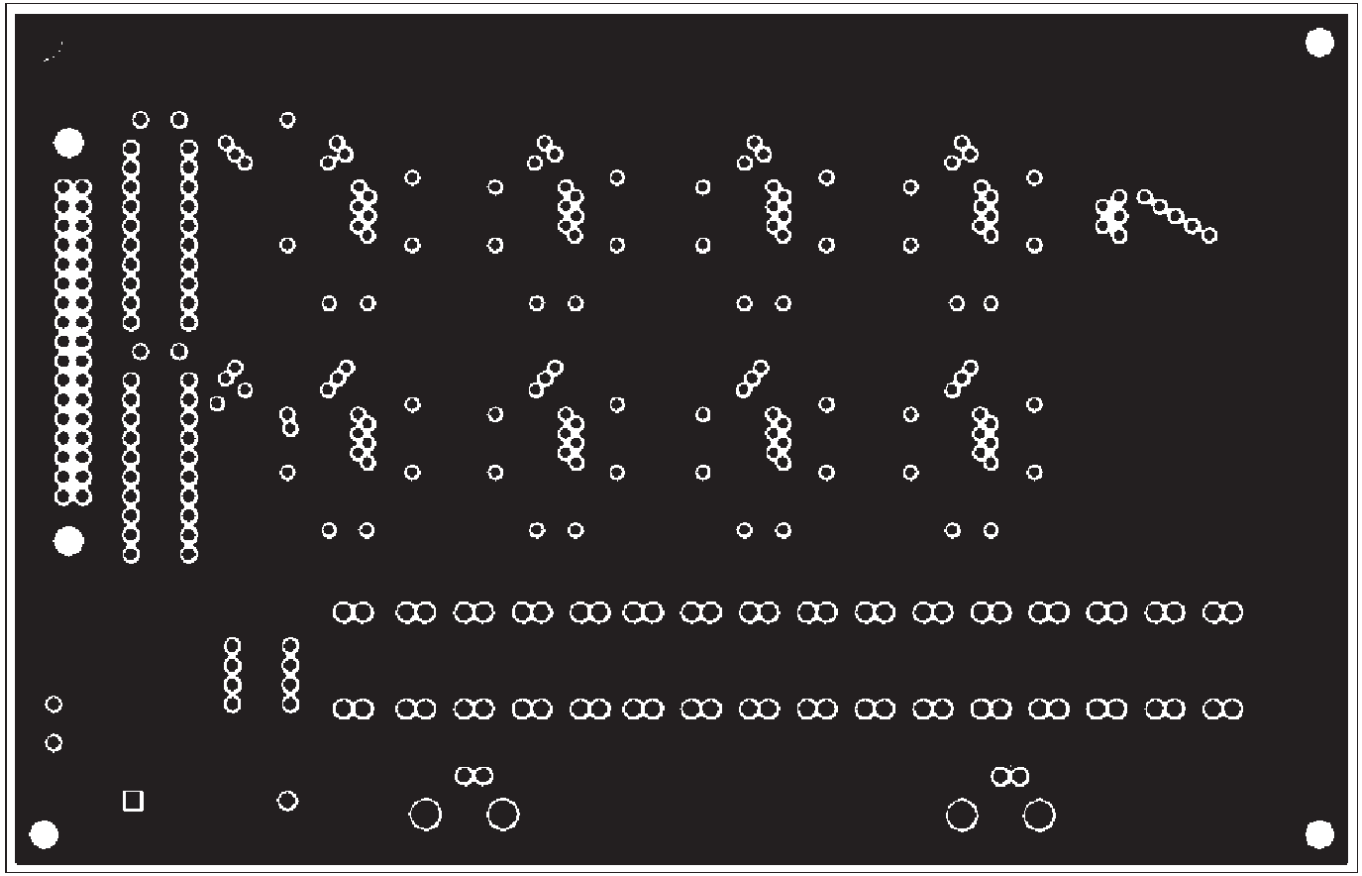

FIGURE 4. Layers 2 and 4: Shields.

Layer 3: Input Traces

The input traces are extremely sensitive as the input impedance of the DDC112 is very high. Careful routing of these traces is recommended to prevent coupling, especially from 60Hz sources. Placing these traces on a separate layer usually allows for better shielding. Keep them as short as possible and ground the unused metal around the inputs. Watch that the inputs do not pass close to noisy vias. If the sensors are on a different PCB board, consider using a shielded connector for the input traces to maintain the shielding from board-to-board.

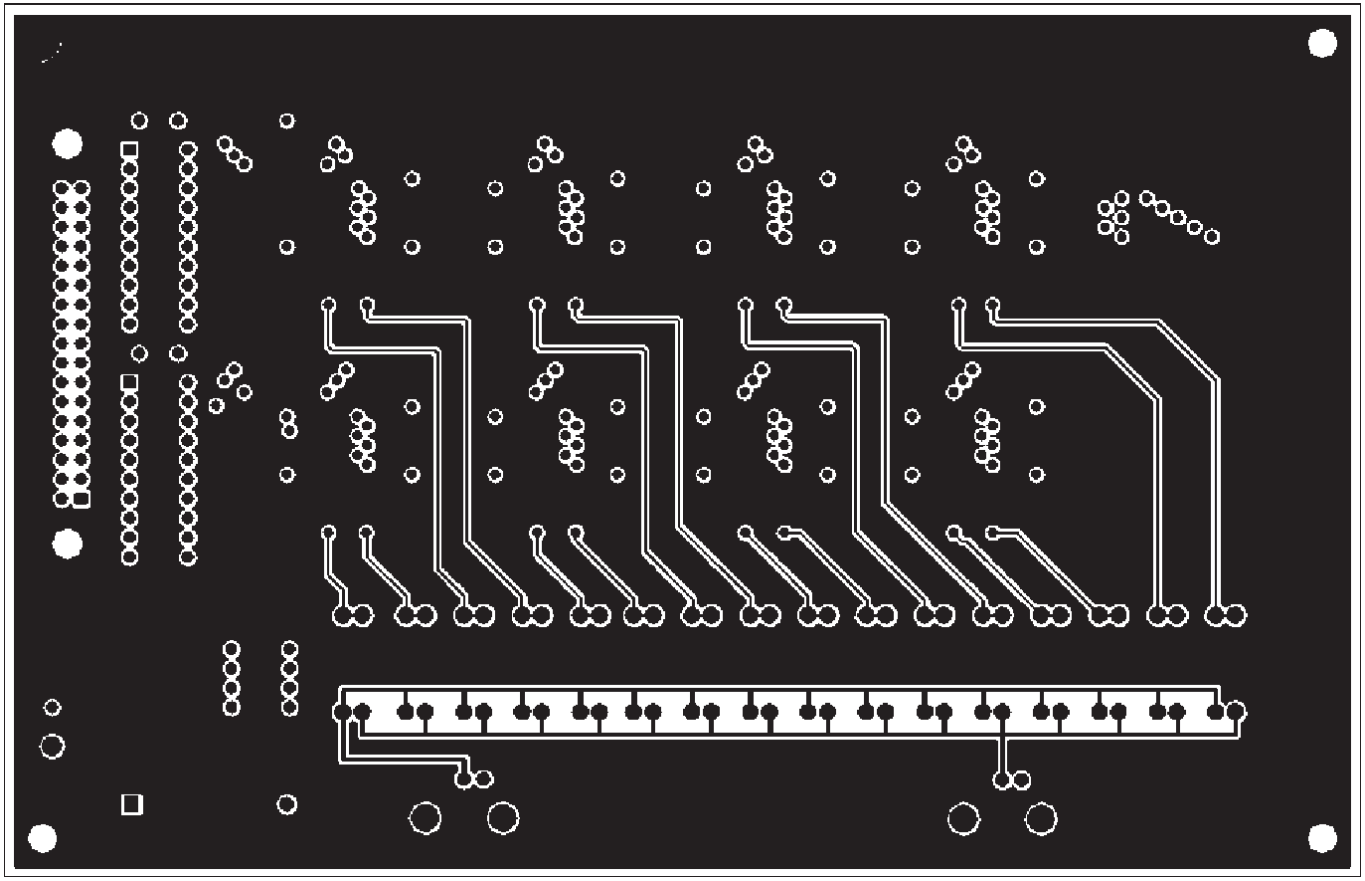

FIGURE 5. Layer 3: Input Traces.

Layer 5: Analog and Digital Power and V_{REF}

The routing of the power and V_{REF} lines is rather straightforward, however, be certain to use wide enough traces so IR drops are not an issue. Keep the vias for these traces away from the input lines. As with the ground, a single +5V supply was used for both analog and digital power since all of the digital signals are synchronous on this board.

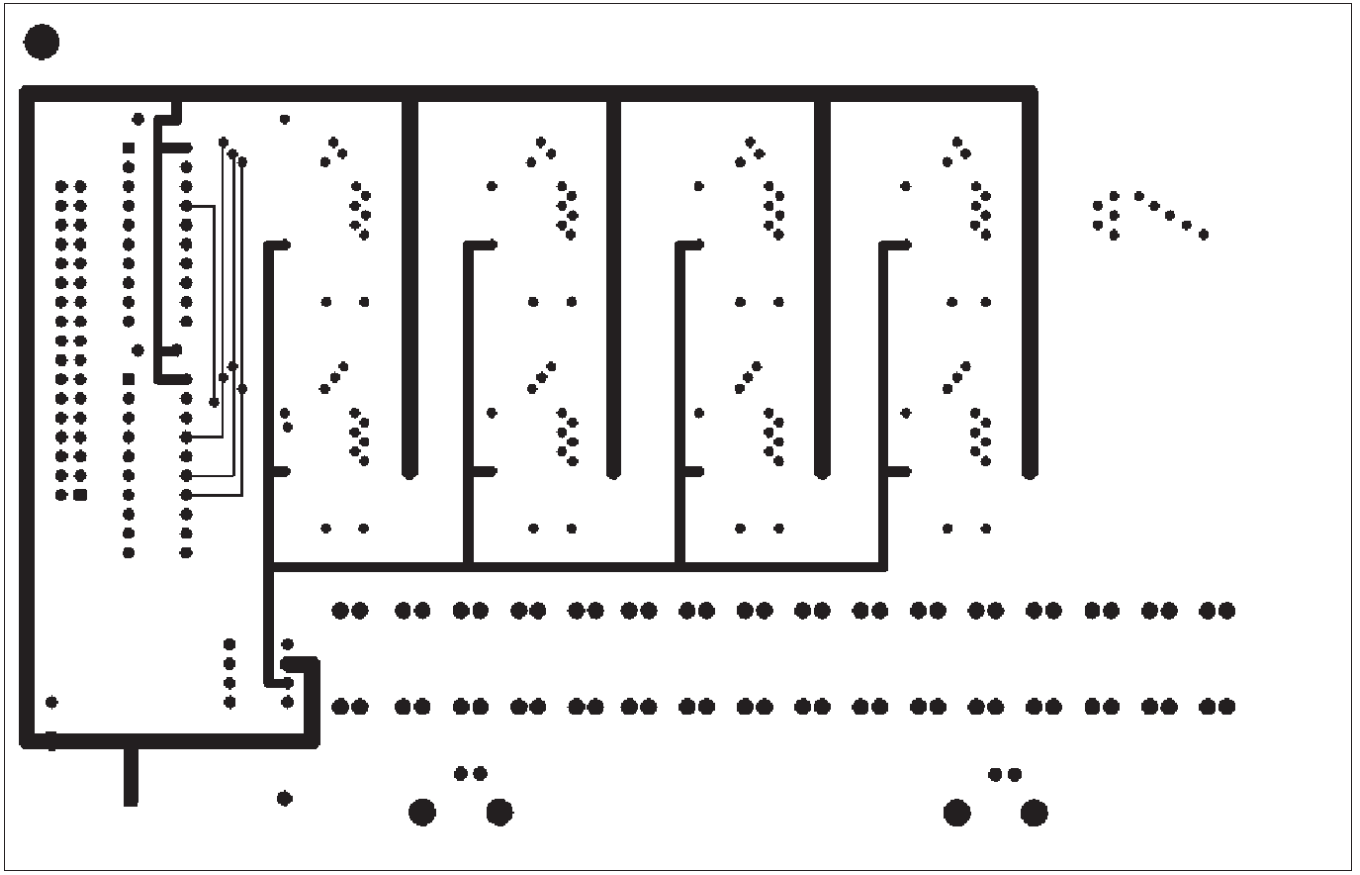

FIGURE 6. Layer 5: Analog and Digital Power and V_{REF}.

Layer 6: Digital Traces

The main concern with digital traces on multi-DDC112 boards is transmission line effects. Reflections become more of a problem on these boards due to the longer trace lengths and higher capacitance from the additional DDC112s, especially on DCLK. Glitches on this trace can cause accidental shifting of data resulting in data readback errors. In general, experiments have shown that using 8 DDC112s placed close together with a local digital buffer is usually sufficient to avoid these problems. For higher numbers of DDC112s, it may become necessary to use termination on the traces or to split a trace into multiple branches, each driven with its own digital buffer. As with the power and V_{REF} lines, make sure that vias on the digital traces keep clear of the input traces.

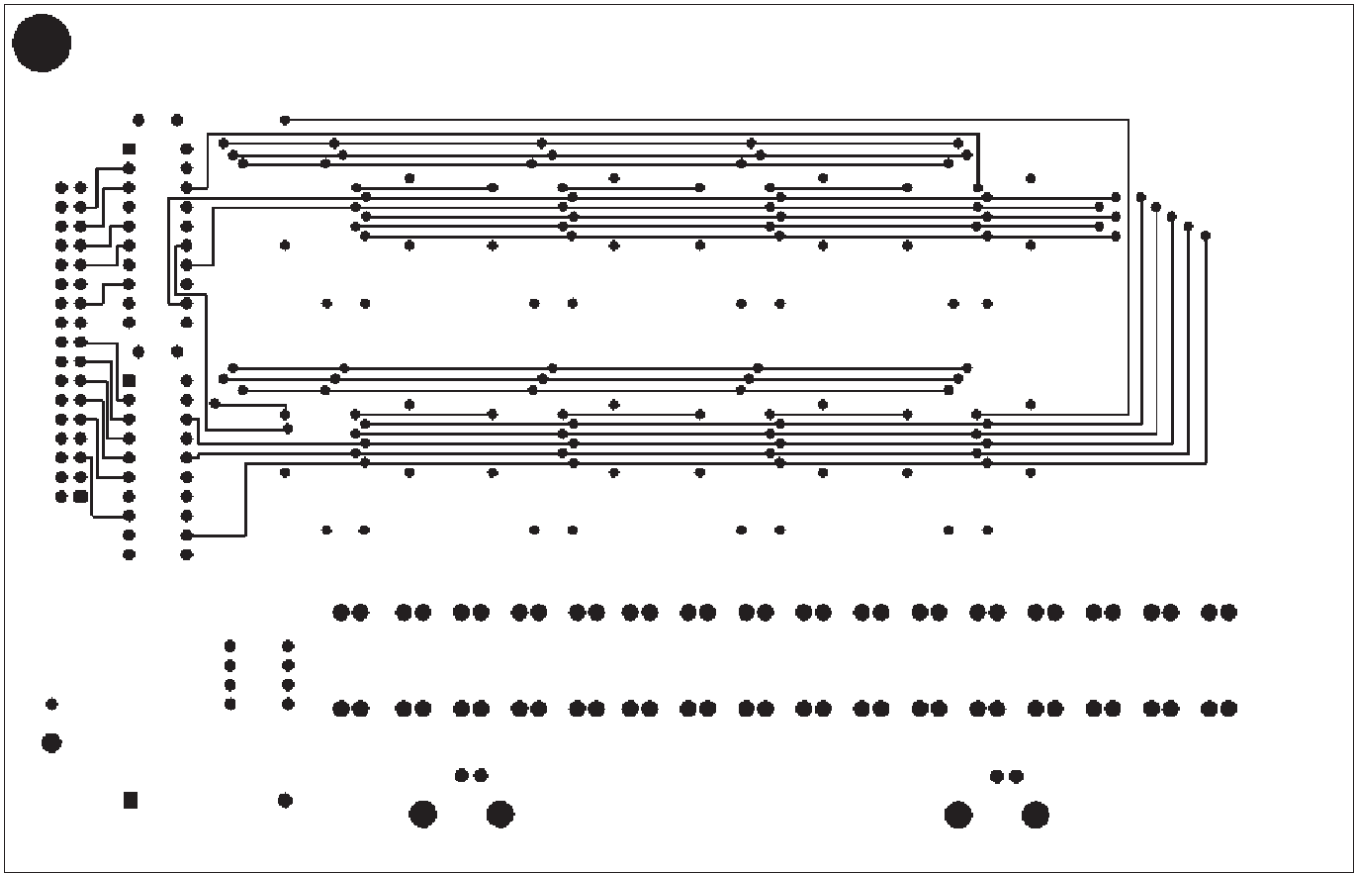

FIGURE 7. Layer 6: Digital Traces.

EVALUATION SOFTWARE

The standard evaluation software that ships with the evaluation fixture can run a multi-DDC112 DUT board. In the **S**etup/**D**ata Transfer window, enter the number of DDC112s on the DUT board as shown in Figure 8. The software can read up to 48 DDC112s, however, a smaller number of DDC112s than actually used on the DUT board could also entered. For example, just one DDC112 may be specified in the software when using the 8-DDC112 DUT board. In this case, only data from the first DDC112 will be retrieved and displayed by the software.

The PC Interface Board stores a maximum of 32,768 data points. Each DDC112 has two inputs and each input has two sides, "A" and "B". Choosing the "Retrieve Sides Separately" option in the software displays data from each side of each input separately. A single DDC112 then has four groups of data: 1A, 2A, 1B and 2B. The maximum number of data points that can be retrieved for each group is 32,768/4 = 8,192. For multi-DDC112 DUT boards, the maximum number of data points per group is even less. For example, retrieving data from all 8 DDC112s on the 8-DDC112 DUT board limits the maximum number of data points per group to 32,768/(4 • 8) = 1024. To read more data points, reduce the number of DDC112s being read.

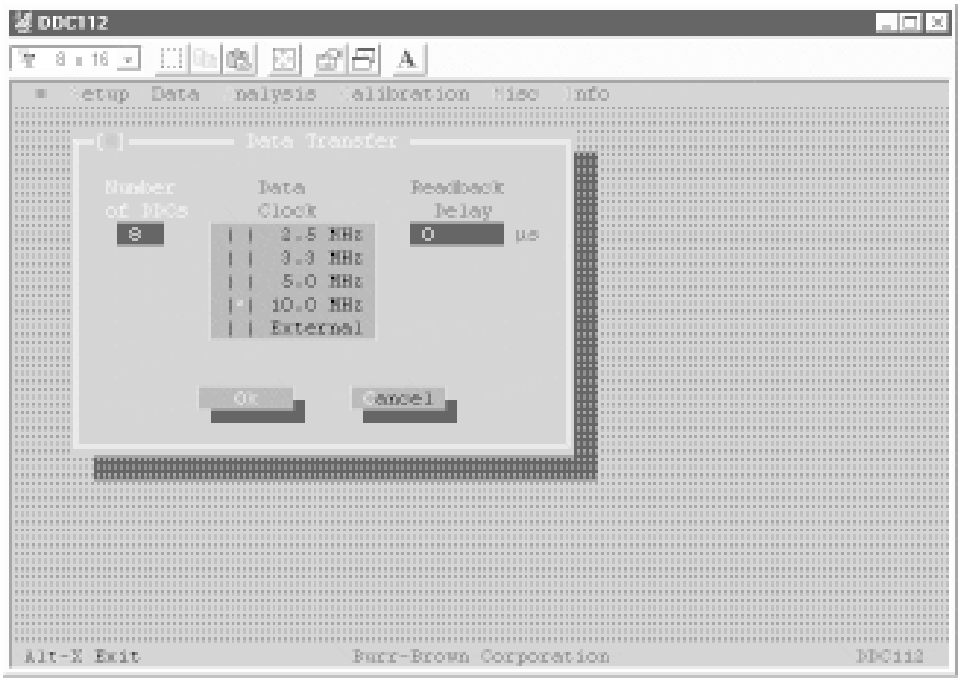

FIGURE 8. Setup for 8-DDC112 DUT Board.

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