

USING EXTERNAL INTEGRATION CAPACITORS ON THE DDC112

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This application bulletin discusses issues that arise when using external integration capacitors on the DDC112. It expands on the explanation given in the data sheet and provides some new data to help you select and use the capacitors. It does assume a basic understanding of the DDC112's operation. For a good introduction to the DDC112, please see the DDC112's data sheet.

Digital input pins RANGE0, RANGE1 and RANGE2 of the DDC112 set the full-scale range. Table I lists the corresponding range for each combination. Ranges 1 through 7 provide full-scale ranges starting at 50pC and increasing in

steps of 50pC. These ranges use capacitors internal to the DDC112. For applications requiring other ranges, Range0 allows the user to choose the full-scale range by disabling the internal capacitors and using external ones. Figure 1 shows a simplified block diagram of the front-end integrators using external integration capacitors. The integration capacitors connect to the operational amplifiers via pins 3-6 and 23-26. Notice how pins 3, 5, 24 and 26 internally connect directly to the inputs 1 and 2. These pins are extremely sensitive and must be treated very carefully. Table II summarizes the connections. When external capacitors are not being used, leave pins 3-6 and 23-26 disconnected. The DDC112 ties them internally to analog ground.

RANGE2	RANGE1	RANGE0	FULL-SCALE RANGE
0	0	0	0.96 C _{EXT} V _{REF}
0	0	1	50pC
0	1	0	100pC
0	1	1	150pC
1	0	0	200pC
1	0	1	250pC
1	1	0	300pC
1	1	1	350pC

Table I. Full-Scale Range Selection.

SIDE	PIN TO OP AMP'S NEGATIVE INPUT (VERY SENSITIVE)	PIN TO OP AMP'S OUTPUT
1A	5	6
1B	3	4
2B	26	25
2A	24	23

Table II. External Capacitor Pin Connections.

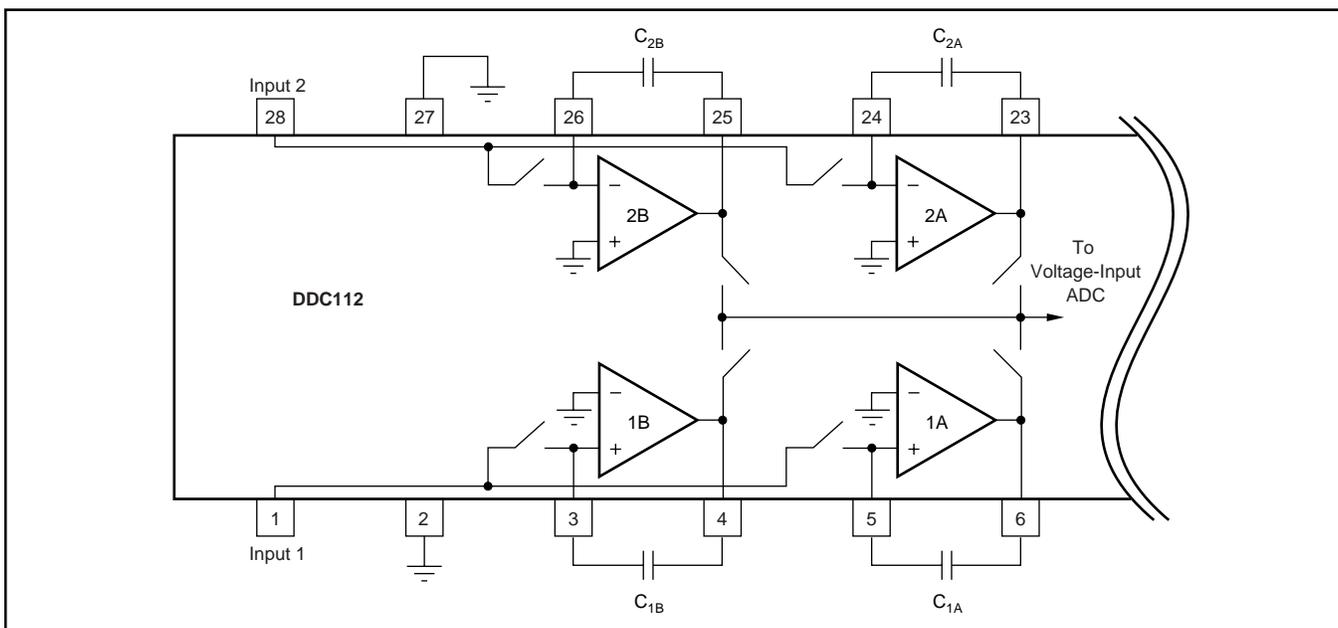


FIGURE 1. Simplified Block Diagram of Front-End Integrators Using External Integration Capacitors.

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The DDC112 operates the same with internal or external integration capacitors. First, the integration capacitor precharges to V_{REF} . As the integration begins, the input signal removes charge from the capacitor, driving the voltage at the op amp's output lower. At the end of the integration, the input signal switches to the other side, while the voltage-input ADC measures the held value against V_{REF} . This cycle continues on and on (see the data sheet for more information) effectively allowing continuous integration of the input signal. The following sections help in selecting the external capacitor, show performance data and discuss layout issues.

SELECTING THE CAPACITOR VALUE

The value of the integration capacitor and V_{REF} set the full-scale range. As shown in Table I, the full-scale range when using external integration capacitors is:

$$Q_{FS} \approx 0.96 V_{REF} C_{EXT}$$

The average current to reach full-scale is then:

$$I_{FS} = \frac{Q_{FS}}{T_{INT}} \approx \frac{0.96 V_{REF} C_{EXT}}{T_{INT}}$$

The external capacitors allow you to select the full-scale range you desire. The external range should be larger than what is available internally. While small external capacitors can be used, for ranges less than 350pC it's best to use the internal capacitors. These capacitors tend to be more linear and the integrator has slightly better noise performance using the internal ranges. Plus, using the internal capacitors saves on components and printed circuit board (PCB) floor space.

In general, the same value capacitor should be used on the A and B sides of an input. Doing so helps match the offset and gain between the sides. If for some reason you want different value capacitors for the A and B sides, you will be limited to the full-scale range of the smaller capacitor. Here's why: input signals exceeding the full-scale range of an integrator rail the output of the op amp to ground. The op amp no longer provides a virtual ground at the input and additional input current forces the input node to rise above ground until the ESD diode at the input (not shown in Figure 1) turns on. The voltage across the input creates a charge buildup. When the integration switches to the other side, the charge is then dumped onto that side's integration capacitor causing an error. This error is usually large enough to make the data from the larger capacitor's side unusable.

For example, assume sides A and B use 100pF and 200pF capacitors, respectively, $V_{REF} = 4.096V$ and the total charge supplied by the input signal during the integration time is 500pC. This signal exceeds side A's full-scale range (393pC) but not side B's (786pC). During integration on side A, that side's op amp rails causing the input to rise above ground.

Charge builds up at the input and is dumped to side B when the integration switches sides. This charge produces an error which corrupts side B's readings even though the input signal is below side B's full-scale range. The input signal must be kept below the smaller full-scale range of side A for valid side B data. There is no similar restriction between inputs 1 and 2 and different value capacitors for the two inputs can be used.

The specified maximum integration capacitor is 250pF. For $V_{REF} = 4.096V$, this corresponds roughly to a full-scale range of 1000pC. This is a conservative specification. For many applications, much larger capacitors can be used. Experiments have shown good results at room temperature even with capacitors exceeding 2nF ($\approx 7800pC$) for $CLK = 10MHz$. Slowing down CLK allows even larger value capacitors to be used as there will be more time for the integration capacitor to precharge to V_{REF} .

The DDC112 was designed to handle a maximum input current of 750 μA . Be careful not to exceed this limit when using large external capacitors. The DDC112 will work with very high input currents, but running it this way places stress on internal metal lines which can cause premature device failure.

SELECTING THE CAPACITOR DIELECTRIC

The quality of the external integration capacitor strongly affects performance.

Some of the more critical parameters include: voltage coefficient, temperature coefficient and dielectric absorption. The voltage coefficient of the capacitor introduces non-linearities which degrade INL. The temperature coefficient produces gain error drift over temperature. Dielectric absorption can degrade performance for higher frequency input signals and also affect linearity.

Suitable dielectrics for the capacitors include high-quality multilayer ceramics, mica, and polystyrene. The capacitors should be physically small to allow them to be placed as close as possible to the pins on the DDC112. In general, we have found ceramic C0G (or NPO) capacitors in surface-mount packages to be a good choice. They are small, inexpensive, stable and available in a wide range of values. Be sure to avoid the X7R and Z5U ceramics. These capacitors often have very poor linearity performance.

PERFORMANCE

Noise

The two main contributors of noise in the DDC112 are the front-end integrators and the voltage-input ADC. For the internal ranges, particularly the lower ones, the noise of the integrators dominates. Its noise is inversely proportional to the integration capacitor and proportional to the sensor capacitance, C_{SENSOR} . Since external capacitors are typically much larger in value than the internal capacitors, when they are used the integrator usually contributes less noise. This in

turn reduces the sensitivity of the noise to C_{SENSOR} . Figure 2 illustrates typical noise (with a low-level input signal) versus C_{SENSOR} for different values of the external capacitor, C_{EXT} . Notice how the slope of the noise vs C_{SENSOR} plot decreases for the larger external capacitors as a result of the decreased sensitivity in the front-end integrators.

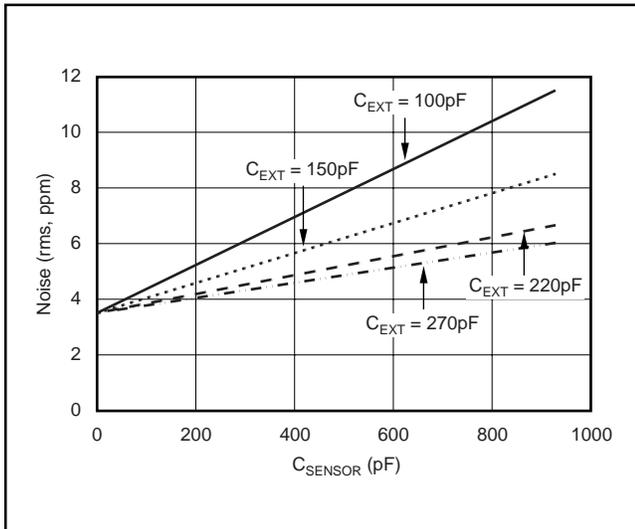


FIGURE 2. Noise vs C_{SENSOR} for Different Values of C_{EXT} .

Linearity

The front-end integrators set the linearity performance of the DDC112 and in the integrators the voltage coefficient of the integration capacitor ultimately limits the linearity. As the input signal increases, the voltage across the integration capacitor increases. This in turn changes the value of the integration capacitor due to the capacitor's non-zero voltage coefficient and causes the transfer function to deviate from an ideal linear integrator.

Fortunately, the internal capacitors of the DDC112 have a low voltage coefficient and provide good performance. To keep the same level of performance with external capacitors, it's important to choose capacitors with low voltage coefficients. Figure 3 shows a plot of integral non-linearity (INL)

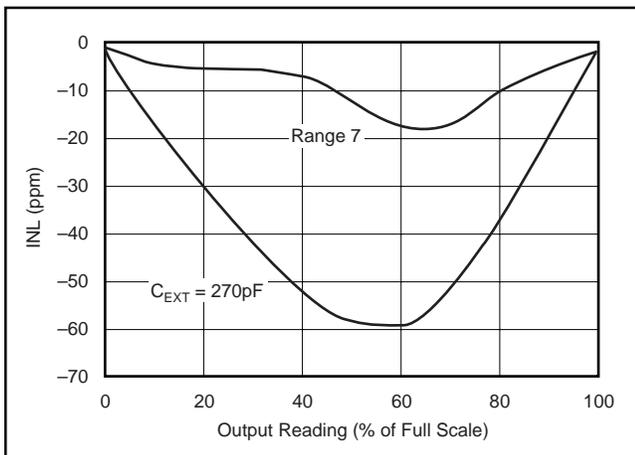


FIGURE 3. INL vs Output Reading Using an External Integration Capacitor.

versus DDC112 output reading with ceramic COG capacitors. An endpoint fit was used to calculate INL. The external capacitors were approximately 270pF and the integration time was 500 μ s. For comparison, the INL of the largest internal capacitor (Range 7) is also plotted.

PCB LAYOUT

The layout of the external capacitors and traces on the printed circuit board is critical. Using small surface-mount packages like the "0805" for the capacitors allows for compact layouts without the need for vias in the PCB. Figure 4 shows an enlarged layout with only the external capacitors included for simplicity. As discussed earlier, pins 3, 5, 24 and 26 connect internally to the inputs and should be kept as short as possible to reduce pickup and leakage. Consider using the top-side metal for a ground plane and make sure the ground plane surrounds the capacitors and traces to provide shielding. If a different layer is used for the ground plane, then tie the unused metal near the external capacitors to ground to form a shield. And remember, if the external capacitors are not being used, leave pins 3-6 and 23-26 floating.

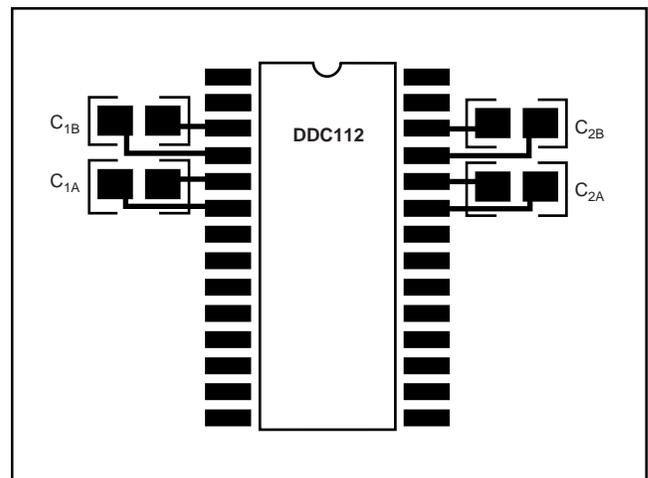


FIGURE 4. Layout Example Using External Integration Capacitors.

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