

5 Converter Topologies for Integrating Solar Energy and Energy Storage Systems



Harald Parzhuber

With energy storage systems prices becoming more affordable and electricity prices going up, the demand for renewable energy sources is increasing. Many residences now use a combined solar energy generation and battery energy storage system to make energy available when solar power is not sufficient to support demand. [Figure 1](#) illustrates a residential use case and [Figure 2](#) shows how a typical solar inverter system can be integrated with an energy storage system.

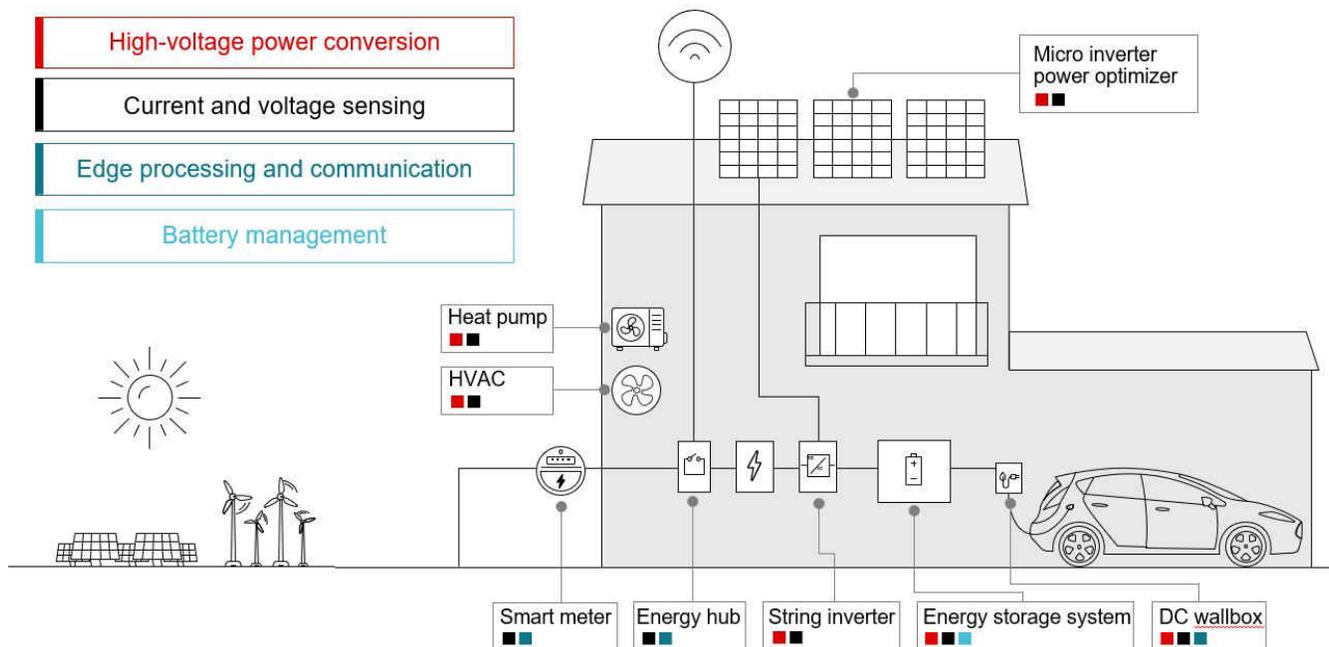


Figure 1. A Residential Solar Energy Generation and Energy Storage System Installation

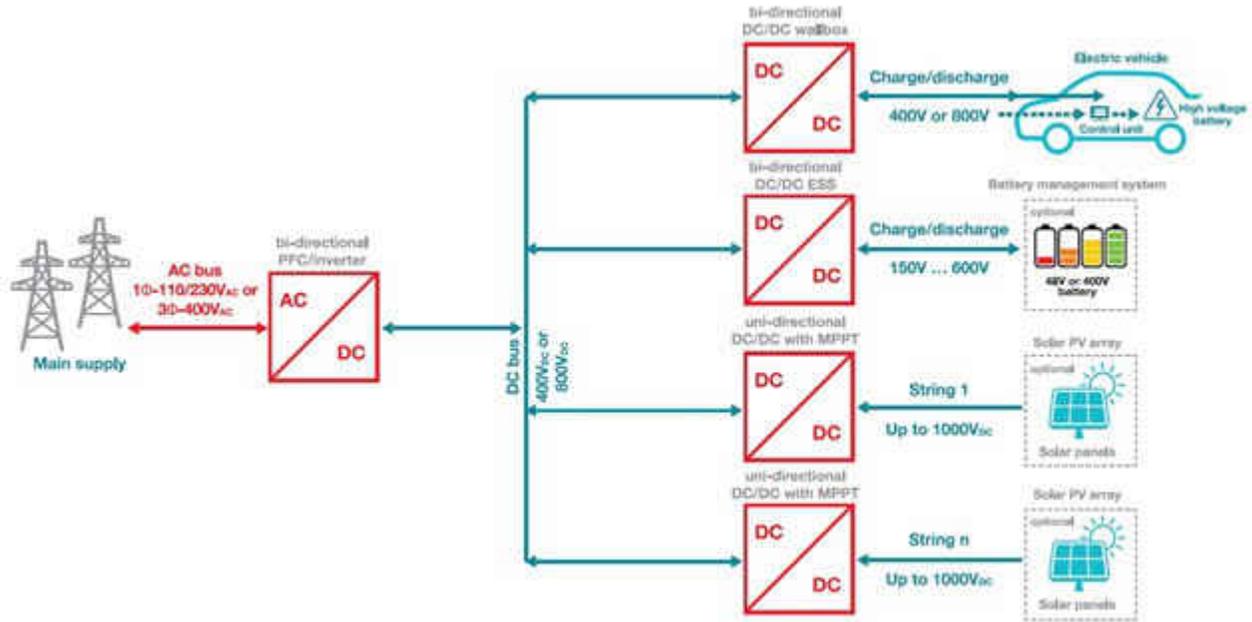


Figure 2. A Typical Solar Inverter System With an Energy Storage System

In the best-case scenario, this type of system has highly efficient power management components for AC/DC and DC/DC conversion and high power density (with the smallest possible solution size) that are highly reliable (with the lowest losses) and enable fast time to market. Those requirements are not always achievable at the same time, however, and you will need to make trade-offs on the best power-conversion topologies for these subblocks.

What existing power topologies for AC/DC and DC/DC buck and boost power converters have in common are half bridges or converter branches that run interleaved, either to increase power levels in a DC/DC converter or to achieve three-phase operation in an AC/DC inverter or power factor correction stage by placing three branches running in 120-degree phase shifts. Figure 3 shows simplified schematics of five power topologies.

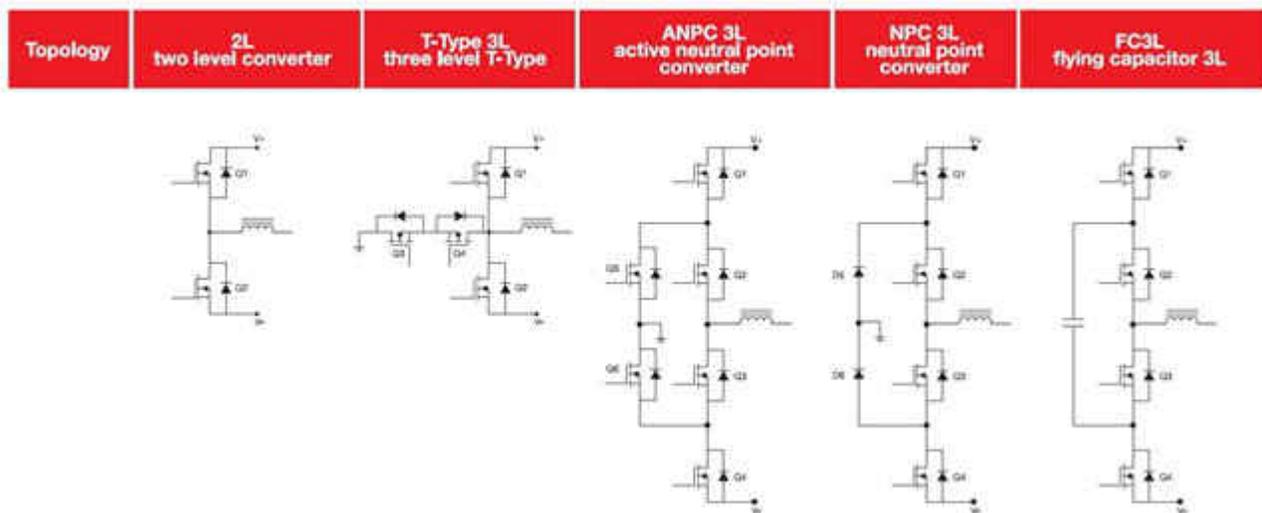


Figure 3. Power Topologies for Half-bridge and Branch Equivalent

- **Topology No. 1:** In the **two-level converter topology**, pulse-width modulation (PWM) signals are applied complementary (with a dead-time delay to avoid shoot-through because of overlapping switching signals) to power devices Q1 and Q2. For the positive sine wave at the output, the duty cycle applied is >50% at Q1. For the negative sine wave at the output, Q2 has a >50% duty cycle. It is a simple concept to control the output power, but output signals before the line filter have a full bus voltage swing, which requires a larger filter to reduce electromagnetic interference. The ripple frequency into the filter is the PWM frequency, which affects the size of the filter.

Three-level topologies allow the use of smaller passive components and have lower EMI compared to two-level converters. There are four three-level topologies:

- **Topology No. 2:** The **T-type topology** is named for the way that the transistors are arranged around the neutral point (V_N). Q1 and Q2 connect between the DC link, and Q3 and Q4 are in series with V_N . The ripple frequency seen by the filter is equal to the PWM frequency applied to switches Q1 through Q4. This defines the size of the filter components to achieve the required low total harmonic distortion at the AC line frequency. Q1 and Q2 see the full bus voltage and need to be rated at 1,200 V for an 800-V DC-link voltage in the system. Since Q3 and Q4 connect to V_N , they see only half the bus voltage and can be rated at 600 V in an 800-V DC-link voltage system, which saves costs on this converter type. See the [10-kW, Bidirectional Three-Phase Three-Level \(T-Type\) Inverter and PFC Reference Design](#).
- **Topology No. 3:** In the **active neutral point clamped (ANPC) converter topology**, V_N connects with active switches Q5 and Q6 and sets V_N in the middle between the DC-link voltage. Like the T-type converter, the ripple frequency seen by the filter is equal to the PWM frequency defining the size of the AC line filter. What's nice about this architecture is that all switches can be rated at half the maximum DC-link voltage; in an 800-V system, you can use 600-V rated switches, which positively impacts cost. When turning off this converter, it's important to limit all voltages across each switch to half the DC-link voltage. In other words, the control microcontroller (MCU) needs to handle the shutdown sequencing. TI's [TMS320F280049C](#) and other devices in the C2000™ product family have configurable logic that allows the realization of shutdown logic in hardware to offload software tasks for the MCU. See the [11-kW, Bidirectional, Three-Phase ANPC Based on GaN Reference Design](#).
- **Topology No. 4:** The **neutral point clamped (NPC) converter topology** is derived from the ANPC topology. Here, V_N connects through diodes D5 and D6 and sets V_N in the middle between the DC-link voltage. The output ripple frequency seen by the filter is equal to the PWM frequency defining the size of the AC line filter. Like the ANPC topology, all switches can be rated at half the maximum DC-link voltage, but instead of two more switches, there are two fast diodes. The NPC topology's slightly lower cost compared to the ANPC topology comes at the expense of slightly lower efficiency. The requirements for shutdown sequencing are also identical to the ANPC topology. It is easy to derive an NPC topology from the ANPC reference design mentioned above.
- **Topology No. 5:** The **flying capacitor topology** already tells you what's happening in this converter; a capacitor connects to the switch nodes of the stacked half bridges realized by Q1 and Q2 and Q3 and Q4. The voltage across the capacitor is limited to half the DC-link voltage and shifts periodically between $V+/V-$; power transfers when shifted. This topology uses all switches during the positive and negative sine wave. In this topology, the output ripple frequency seen by the filter is twice the PWM frequency given each cycle shift of the flying capacitor, resulting in a smaller-sized AC line filter. Again, all switches can be rated at half the maximum DC-link voltage, which positively impacts cost.

Table 1 lists the benefits and challenges of the different topologies.

Table 1. The Benefits and Challenges of Different Converter Topologies

	2L TIDA-01606 in 2L	T-Type 3L TIDA-01606	ANPC TIDA-010210	NPC 3L derived from ANPC	FC3L Flying capacitor 3L
Benefits	<ul style="list-style-type: none"> Simple control scheme 2 switches only 2 PWM 	<ul style="list-style-type: none"> Easy control scheme Q3/Q4 see $1/2 V_{DC}$ Better EMI than 2L $f_{RIPPLE} = f_{PWM}$ 	<ul style="list-style-type: none"> Good efficiency All switches see $1/2 V_{DC}$ Better EMI than 2L 	<ul style="list-style-type: none"> Lower cost than ANPC All switches see $1/2 V_{DC}$ Better EMI than 2L $f_{RIPPLE} = f_{PWM}$ 4 PWM 	<ul style="list-style-type: none"> Highest efficiency Only 4 HF FETs (& 1Cap) $f_{RIPPLE} = 2 \times f_{PWM}$ Smallest magnetics Lowest EMI
Challenges	<ul style="list-style-type: none"> Q1/Q2 see full V_{DC} High EMI for bigger f_{PWM} Passives are biggest 	<ul style="list-style-type: none"> Q1/Q2 see full V_{DC} 4 PWM 	<ul style="list-style-type: none"> More complex control scheme Shutdown sequencing critical 6 PWM 	<ul style="list-style-type: none"> Lower efficiency than ANPC More complex control Shutdown sequencing critical 	<ul style="list-style-type: none"> Initial charging of flying capacitor Shutdown sequencing critical

All four three-level topologies have clear advantages on power density (with the smallest possible solution size), highly reliable operation, and fast time to market over traditional two-level converters. Using wide band-gap devices and high-performance MCUs increase these advantages even further, at a comparable cost.

Additional Resources

- Learn more about how you can accelerate your development of [solar energy systems](#).
- Check out the [Bidirectional, Dual Active Bridge Reference Design for Level 3 Electric Vehicle Charging Stations](#).
- Discover our battery management and power conversion technology for [energy storage systems](#).

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated