SPAY025 —May 2006
White Paper

Semiconductor IC Packaging Technology Challenges: The Next Five Years

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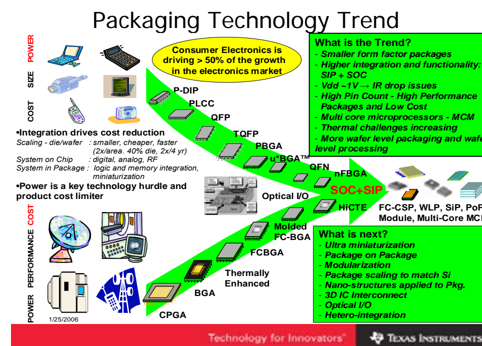
In the era of communications and entertainment, growth of consumer electronics is exploding. Consumer demand for increased mobility, wireless connectivity and advanced features have paved the way for a variety of new products, including advanced mobile handsets, PDAs, digital still cameras and camcorders, portable music players and many others. The silicon solutions driving these products are more highly integrated than ever before, as advancements in process technology are delivering system-on-a-chip (SoC) solutions that are smaller, faster and lower cost. Users of portable products also want longer battery life, and a heightened emphasis on low power is key.

These trends, along with the broad range of end equipments emerging, require a large diversity of new IC package types to meet specific applications or markets. Increased device complexity will generate an explosion of new creative and disruptive technology packaging solutions, and in some markets and applications, packaging technology will become a key differentiator when making purchasing decisions.



To that end, there are a number of general packaging technology challenges the industry must address in the next five years. Addressing the below issues will take the packaging technology roadmap to a new level, including migration toward ultra miniaturization; growth of package on package; modularization; package scaling to match silicon scaling; nanostructures; 3D IC interconnect; optical input/interconnect and heterogeneous integration.

Packaging Advanced CMOS Technology with Copper and Ultra Low K Dielectrics

The biggest challenge impacting packaging in the next five years is the industry's ability to develop solutions packaging both advanced CMOS with copper and ultra-low k dielectrics. The fast adoption and high volume ramp of advanced CMOS silicon with copper interconnect and low k dielectrics have had a major impact on packaging. Packaging must move toward compliant chip-to-chip substrate interconnects and low stress packaging solutions, along with mechanical reinforcements under pads. The ability to perform better characterization is essential, along with development of interconnect ILD materials to address interfacial adhesion and improve fracture toughness. Thermal connectivity with strained silicon is potentially 4 to 5X worse than bulk silicon. The industry needs to better understand this issue and address potential problems. Developing wafer thinning and dicing solutions for wafers with copper and ultra-low k dielectrics will also be required.

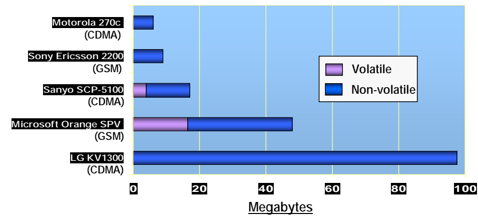
Scaling for More Die Per Wafer and New Interconnect Technology

Disruptive packaging solutions will be necessary to continue to scale down size and area for product input/output, and pad ring in CMOS nodes beyond the 45-nm process. As metal systems continue to thin, IR drop and EM issues will grow and new interconnect alternatives will be considered. Techniques such as stud bumping, dual bonding on same pad, thinner aluminum wire, copper wire, Bond on PO, copper over anything and bond wire jumpers are potential solutions.

In addition, ultra fine pitch and compliant interconnect solutions such as micro bumps, coated-wire bonding process, fine pitch less than 50 um wire bonding and Au stud bumping to thinned dies will also be needed in this time frame. Some may consider whether the industry will see the end of solder bump for ultra fine flip chip interconnect applications. Other technologies that will be explored are room temperature Cu-Cu interconnection and fine pitch pad alignment; 3D IC Interconnect; wafer-to-wafer; die-to-wafer, through silicon vias; and Cu nails.

SoC and SiP Integration and Functionality, Automated System Level Co-Design Tools

Product designers are continuously facing the question of whether they should design new products using SoC or system in package (SiP) or both. This is especially true in the mobile handset market where consumers are increasing their reliance on the handset to listen to music, take and send pictures, record and watch video, play games and more. Operating multiple applications places an increased strain on system memory requirements, and is driving the need for SiP solutions. Functionality increases with time for SiP and SoCs, and cost is typically the deciding factor for SoC vs. SiP at a given time.



Another critical gap the industry must close is faster development and availability of 3D Chip-Package-System Co-Design Automation for electrical, thermal and mechanical compatibility. Development of cost-effective package on package modules is also critical, along with the impact to manufacturing business models and testability.

The industry is also experiencing challenges in rolling out complex SoC products that include RF and analog integration around digital cores. Digital and RF integration into smaller modules requires closer placement of the digital and RF dies. This has raised interference issues between the digital and RF signals that must be resolved, and integrated shielding and flip chip solutions could help address the issues. Modeling tools with more predictable results are essential, with the ability to allow virtual packaging of advanced silicon and systems. System and component level reliability failure modes and acceleration factors must be well understood, and there will be an increased need for modeling and design tools to predict manufacturability and reliability performance.

Higher Performance and Higher Thermal Density

A change from the use of wide/slow busses to high speed serial I/O will drive the need for low cost, matched transmission line characteristic packages, and new thermal management techniques will be implemented to address cooling. We are currently exploring methods such as RF shields, and expect those to become an integral part of packaging for future consumer electronics and portable products. Techniques such as the use of heat pipes and vents will ultimately migrate toward use in these systems and move heat to the system enclosure. Additionally, Multi-Core Micro Processors will drive die size up and increase demands for high performance multi-chip modules. Non-traditional thermal management solutions, such as liquid cooling, compact and solid state refrigeration will be needed but at significantly lower cost.

The industry is experiencing increased demand for low-cost, high-performance packages, and development of high-performance wire bond and low-cost flip chip packaging is essential. A better understanding of fundamental issues related with lead-free packaging, for example; metallurgical life prediction models, will aid on this front. In addition, hot spot minimization will drive a need for a high thermal conductivity die attach directly to

Cu spreading plates in organic substrate BGA packages. As a result, flip chip packaging portfolios and volumes will grow significantly.

New Packaging Materials

In the next five years, development of several new packaging materials is critical. Some examples include low stress under fill to support large die sizes, ultra fine pitch bump and more than 10 K bumps/die. Pressurized under fill is one technique showing strong promise. Vacuum under fill solutions for smaller die are also under evaluation, and there is potential for extended use for larger dies. These solutions, however, do not do much to enhance current technology-capillary fill. No flow and wafer-level fill do not hold much promise for larger, high bump count devices, so some additional driving force is necessary for successful fill-vacuum and/or pressure.

Thermal stability is a key issue, especially in the automotive environment, and the current material set, and perhaps the fundamental epoxy chemistry will not meet requirements for 180 C continuous operations. Exploration of high junction temperature, >150 C, mold compound and die attach materials is underway as a solution to the challenge. This issue extends to RF modules as power density in RF devices is expected to increase dramatically over the next five years while the size continues to shrink. Highly conductive mold compounds and encapsulates to support RF modules have potential to help maintain thermal conductivity despite these changes.

Package substrates will also require considerable development and improvement, especially in high speed electrical transmission applications. For example, silicon substrate can reduce the size of transmission line and line width through the use of lithography technology, and a minimum size transmission line can reduce resistance leading to high speed applications. Some other techniques that may prove successful include coreless thin substrates (wire bond and flip chip) with reduced metal layers to support thin packages and stacked die packages. Substrates with selected solder pre-coating and thin NiAu plating areas are another alternative.

Large format substrates are still experiencing manufacturability, warpage and board attach issues, and these need to be addressed. A very critical requirement is development of low-cost fine pitch flip chip substrates to achieve cost parity with wire bonded packages. This could be achieved by increasing wiring density per layer and reducing layer count.

There is also an emergence of lead-free and RoHS-compliant packaging and use of lead-free solders and 'green materials.' To address thermal requirements, new and exotic lid and lid attach materials will be developed. Solder lid attach, high k lids, micro-channels in the Si or lids and other solutions must have low resistance and excellent reliability for adoption in future packages.

New Assembly Processes

Many new assembly processes will be developed and implemented during the next five years, including ultra thinning of wafers < 50um to enable stacked die, package on package, and ultra thin package. New technology such as laser dicing may be needed, and one example is dicing of advanced Si wafers with low k dielectrics. Wafer level packaging to improve reliability and pin count, ball pitch and routability are also imperative. New under bump metallurgy, bump structure, pre-applied under fill are potential alternatives to improve reliability.

Also important is an understanding of the limitations of wire bond technology in high junction temperature type of applications. For example, 150 C Tj is likely the limit for gold wire on aluminum bond pads. New solutions, including different wire alloys and bond pad metal system, need to be explored along with new encapsulation processes. Liquid compound, compression molding, wafer level molding and low stress thin package encapsulation technologies are examples of low stress assembly processes that combined with low force wire bond and no damage multi probing may be needed to support the assembly and packaging of new CMOS copper and ultra low k silicon processes.

In conclusion, advanced CMOS technology and scaling are enabling a multitude of new and innovative products across many end equipment markets -- including consumer electronics, mobile handsets, the automotive segment and many others. Advanced process technology is delivering highly differentiated and integrated SoC solutions with higher performance, high thermal density, lower power and lower cost. For packaging, the industry must address technical challenges to keep pace. Development of packaging solutions with a cost structure that follows and matches the silicon cost reduction learning curve is the key to success.

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