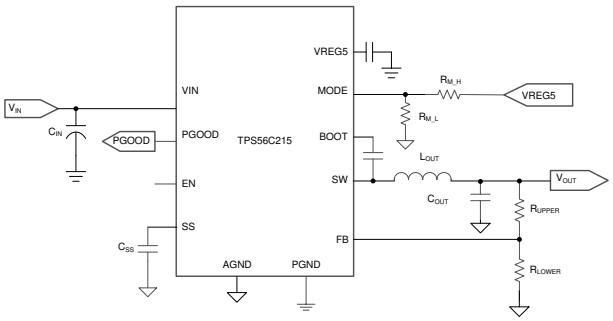
TPS56C215 3.8V 至 17V 输入、12A 同步降压 SWIFT™ 转换器

1 特性

- 集成式 13.5mΩ 和 4.5mΩ MOSFET
- 支持 12A 持续 I_{OUT}
- 4.5V 启动（没有 5.0V 外部偏置）
- 整个温度范围内的基准电压为 0.6V ±1%
- 0.6V 至 5.5V 输出电压范围
- 支持陶瓷输出电容器
- D-CAP3™ 控制模式，用于快速瞬态响应
- 可选强制持续导通模式 (FCCM)，用于实现窄输出电压纹波，或自动跳跃 Eco-Mode，用于实现高轻负载效率
- 400kHz、800kHz 和 1.2MHz 的可选 F_{SW}
- 单调启动至预偏置输出
- 具有断续重启功能的两个可调节电流限制设置
- 可选 5V 外部偏置，可提升效率
- 可调节软启动，默认软启动时间为 1ms
- –40°C 至 150°C 的工作结温范围
- 小型 3.5mm × 3.5mm HotRod™ QFN 封装
- 与 12A TPS56C231 和 8A TPS568231 和 TPS568215 引脚对引脚兼容
- 在 WEBENCH® 设计工具中受支持



典型应用

2 应用

- 服务器、云计算、存储
- 电信和网络、负载点 (POL)
- IPC、工厂自动化、PLC、测试测量
- 高端 DTV

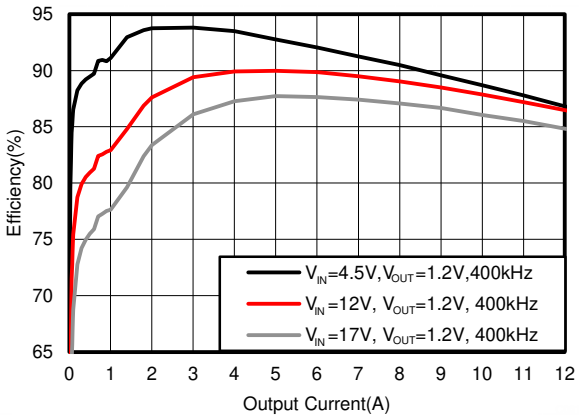
3 说明

TPS56C215 是 TI 最小的一款单片 12A 同步降压转换器，具有自适应导通时间 D-CAP3 控制模式。该器件集成了低 R_{DS}(on) 功率 MOSFET，简单易用且高效，只需极少的外部组件，适合空间受限的电源系统。具有竞争力的特性包括非常精确的基准电压、快速负载瞬态响应、自动跳跃模式运行以实现轻负载效率、可调节的电流限制和无需外部补偿。强制持续导通模式有助于满足高性能 DSP 和 FPGA 的严格电压调节精度要求。TPS56C215 采用热增强型 18 引脚 HotRod QFN 封装，并且设计为在 -40°C 至 150°C 的结温范围内运行。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
TPS56C215	RNN（VQFN，18）	3.5mm x 3.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



效率与输出电流之间的关系

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Revision History 2
5 Pin Configuration and Functions 3
6 Specifications 4
6.1 Absolute Maximum Ratings 4
6.2 ESD Ratings 4
6.3 Recommended Operating Conditions 4
6.4 Thermal Information 5
6.5 Electrical Characteristics 5
6.6 Timing Requirements 6
6.7 Typical Characteristics 7
7 Detailed Description 12
7.1 Overview 12
7.2 Functional Block Diagram 13
7.3 Feature Description 13
7.4 Device Functional Modes 19
8 Application and Implementation 20
8.1 Application Information 20
8.2 Typical Application 20
8.3 Power Supply Recommendations 25
8.4 Layout 26
9 Device and Documentation Support 29
9.1 Device Support 29
9.2 接收文档更新通知 30
9.3 支持资源 30
9.4 Trademarks 30
9.5 静电放电警告 30
9.6 术语表 30
10 Mechanical, Packaging, and Orderable Information 31
10.1 Package Marking 31

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (August 2023) to Revision F (August 2023) — **Page**

- 向 *特性* 列表中添加了引脚兼容数据表链接 1

Changes from Revision D (February 2021) to Revision E (August 2023) — **Page**

- 更新了 *特性* 列表中的引脚兼容器件 1

Changes from Revision C (November 2017) to Revision D (February 2021) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 更正了整个文档中的拼写和语法错误 1
- Added V_{IN}-SW, V_{IN}-SW, and BOOT – SW (10-ns transient) 4
- Changed SW (10-ns transient) min value from -3 V to -5 V 4

Changes from Revision B (July 2016) to Revision C (November 2017) — **Page**

- 添加了特性项“4.5V 启动（没有 5.0V 外部偏置）” 1
- 添加了特性项“4.5V 启动（没有 5.0V 外部偏置）” 1
- 更改了 图 3-1 图像中的 VREG5 引脚处的接地符号。 1
- Changed from "5% resistors" to "1% resistors" in the 节 7.3.4 description 15
- Changed Power-Up Sequence image for 图 7-2 15
- Changed Adjustable VIN Undervoltage Lock Out image for 图 7-3. 17
- Added I_h term to 方程式 5 Definition List 17
- Added 节 10.1 information 31

Changes from Revision A (March 2016) to Revision B (May 2016) — **Page**

- 将 *节 1* 从“支持 14A 持续 I_{OUT}”更改为“支持 12A 持续 I_{OUT}” 1
- 向典型应用原理图添加了元件名称 1
- Deleted I_{OCL} spec for "ILIM+1 option, Valley Current" condition 5
- Changed From: "...up to 14 A" To: "...up to 12 A" in first sentence of *节 7.1* 12
- Deleted four rows in Mode Pin Resistor Settings table for I_{OUT} of 14 A 15

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Changes from Revision * (March 2016) to Revision A (March 2016) **Page**

- 添加了完整量产数据表的内容.....1

5 Pin Configuration and Functions

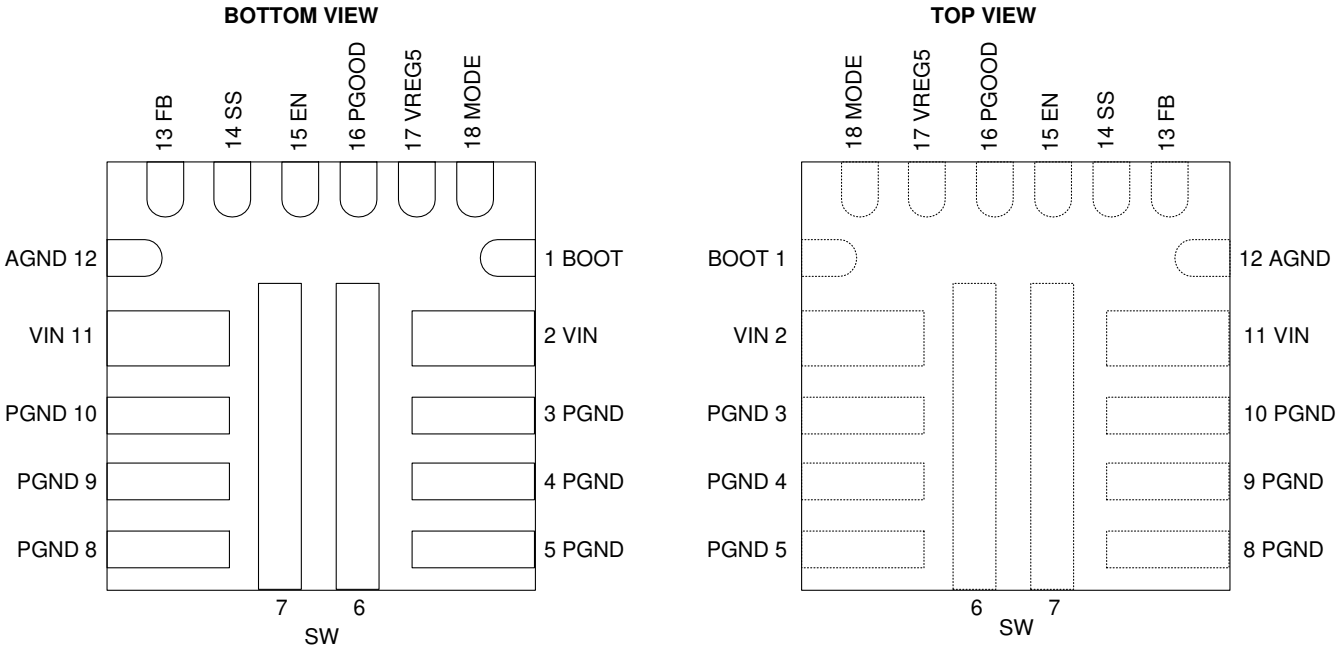


图 5-1. RNN Package 18-Pin VQFN

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between BOOT and SW.
VIN	2,11	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
PGND	3, 4, 5, 8, 9, 10	G	Power GND terminal for the controller circuit and the internal circuitry. Connect to AGND with a short trace.
SW	6, 7	O	Switch node terminal. Connect the output inductor to this pin.
AGND	12	G	Ground of internal analog circuitry. Connect AGND to PGND plane with a short trace.
FB	13	I	Converter feedback input. Connect to the center tap of the resistor divider between output voltage and AGND.
SS	14	O	Soft-Start time selection pin. Connecting an external capacitor sets the soft-start time and if no external capacitor is connected, the converter starts up in 1 ms.
EN	15	I	Enable input control, leaving this pin floating enables the converter. It can also be used to adjust the input UVLO by connecting to the center tap of the resistor divider between VIN and EN.
PGOOD	16	O	Open-drain power good indicator, it is asserted low if output voltage is out of PGOOD threshold, overvoltage, or if the device is under thermal shutdown, EN shutdown or during soft start.
VREG5	17	I/O	4.7-V internal LDO output which can also be driven externally with a 5-V input. This pin supplies voltage to the internal circuitry and gate driver. Bypass this pin with a 4.7-µF capacitor.
MODE	18	I	Switching frequency, current limit selection and light load operation mode selection pin. Connect this pin to a resistor divider from VREG5 and AGND for different MODE options shown in 表 7-3.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input Voltage	V_{IN}	–0.3	20	V
	SW	–2	19	
	SW (10-ns transient)	–5	25	
	V_{IN}-SW		22	
	V_{IN}-SW (10-ns transient)		25	
	EN	–0.3	6.5	
	BOOT – SW	–0.3	6.5	
	BOOT – SW (10 ns transient)	–0.3	7.5	
	BOOT	–0.3	25.5	
	SS, MODE, FB	–0.3	6.5	
	VREG5	–0.3	6	
Output Voltage	PGOOD	–0.3	6.5	V
Output Current(2)	I_{OUT}		14	A
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) to be consistent with the TI reliability requirement of 100k Power-On-Hours at 105°C junction temperature, the output current must not exceed 14A continuously under 100% duty operation as to prevent electromigration failure in the solder. Higher junction temperature or longer power-on hours are achievable at lower than 14A continuos output current.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input Voltage	V_{IN}	3.8		17	V
	SW	–1.8		17	V
	BOOT	–0.1		23.5	V
	VREG5	–0.1		5.2	V
Output Current	I_{LOAD}	0		12	A
Operating junction temperature	T_J	-40		150	°C

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6.4 Thermal Information

THERMAL METRIC(1)		RNN PACKAGE 18 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, V_{IN}=12V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	VIN supply current	T_J = 25°C, V_{EN}=5 V, non switching		600	700	µA
I_{VINSDN}	VIN shutdown current	T_J = 25°C, V_{EN}=0 V		7		µA
LOGIC THRESHOLD						
V_{ENH}	EN H-level threshold voltage		1.175	1.225	1.3	V
V_{ENL}	EN L-level threshold voltage		1.025	1.104	1.15	V
V_{ENHYS}				0.121		V
I_{ENp1}	EN pull-up current	V_{EN} = 1.0 V	0.35	1.91	2.95	µA
I_{ENp2}		V_{EN} = 1.3 V	3	4.197	5.5	µA
FEEDBACK VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C	598	600	602	mV
		T_J = 0°C to 85°C	597.5	600	602.5	mV
		T_J = –40°C to 85°C	594	600	602.5	mV
		T_J = –40°C to 150°C	594	600	606	mV
LDO VOLTAGE						
VREG5	LDO Output voltage	T_J = –40°C to 150°C	4.58	4.7	4.83	V
ILIM5	LDO Output Current limit	T_J = –40°C to 150°C	100	150	200	mA
MOSFET						
$R_{DS(on)H}$	High side switch resistance	T_J = 25°C, V_{VREG5} = 4.7 V		13.5		mΩ
$R_{DS(on)L}$	Low side switch resistance	T_J = 25°C, V_{VREG5} = 4.7 V		4.5		mΩ
SOFT START						
I_{ss}	Soft start charge current	T_J = -40°C to 150°C	4.9	6	7.1	µA
CURRENT LIMIT						
I_{OCL}	Current Limit (Low side sourcing)	ILIM-1 option, Valley Current	9.775	11.5	13.225	A
		ILIM option, Valley Current	11.73	13.8	15.87	A
	Current Limit (Low side negative)	Valley Current		4		A
POWER GOOD						
$V_{PGOODTH}$	PGOOD threshold	V_{FB} falling (fault)		84%		
		V_{FB} rising (good)		93%		
		V_{FB} rising (fault)		116%		
		V_{FB} falling (good)		107%		
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						

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T_J = –40°C to 150°C, V_{IN}=12V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	Output OVP threshold	OVP detect		121% x V_{FB}		
V_{UVP}	Output UVP threshold	Hiccup detect		68% x V_{FB}		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature		160		°C
		Hysteresis		15		°C
$T_{SDN\ VREG5}$	VREG5 thermal shutdown threshold	Shutdown temperature		171		°C
		Hysteresis		18		°C
UVLO						
UVLO	UVLO threshold	VREG5 rising voltage		4.3		V
		VREG5 falling voltage		3.57		V
		VREG5 hysteresis		730		mV
UVLO, VREG5=4.7V	UVLO threshold, VREG5=4.7V	VIN rising voltage, VREG5=4.7V		3.32		V
		VIN falling voltage, VREG5=4.7V		3.26		V
		VIN hysteresis, VREG5=4.7V		60		mV

6.6 Timing Requirements

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ON}	SW On Time	V_{IN} = 12 V, V_{OUT}=3.3 V, F_{SW} = 800 kHz	310	340	380	ns
$t_{ON\ min}$	SW Minimum on time	V_{IN} = 17 V, V_{OUT}=0.6 V, F_{SW}= 1200 kHz		54		ns
t_{OFF}	SW Minimum off time	25°C, V_{FB}=0.5 V			310	ns
SOFT START						
t_{SS}	Soft start time	Internal soft-start time		1.045		ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
t_{UVPDEL}	Output Hiccup delay relative to SS time	UVP detect		1		cycle
t_{UVPEN}	Output Hiccup enable delay relative to SS time	UVP detect		7		cycle

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6.7 Typical Characteristics

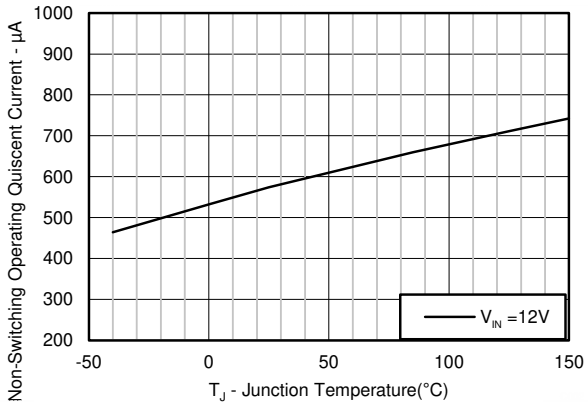


图 6-1. Quiescent Current vs Temperature

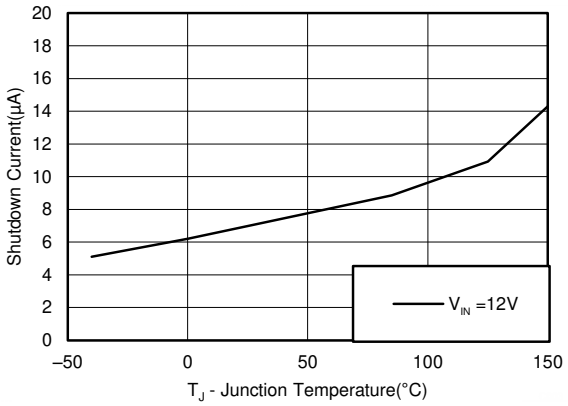


图 6-2. Shutdown Current vs Temperature

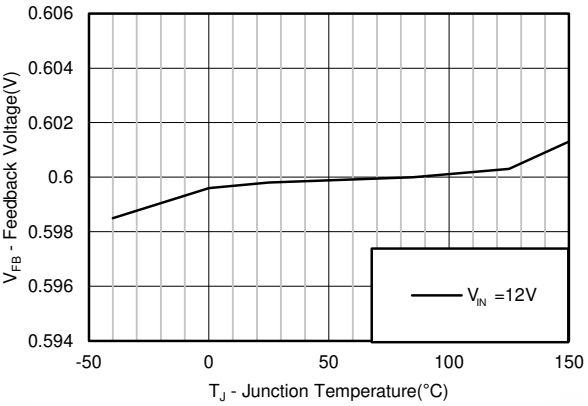


图 6-3. Feedback Voltage vs Temperature

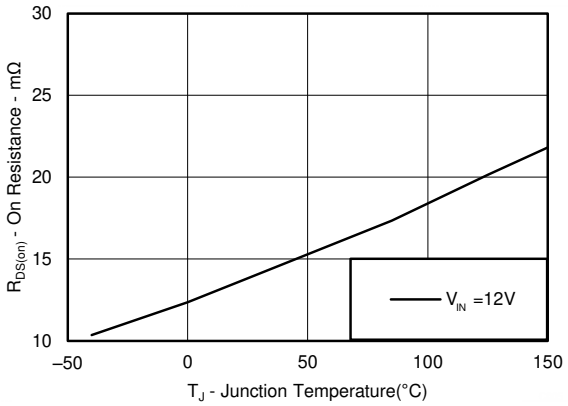


图 6-4. High-side $R_{DS(on)}$ vs Temperature

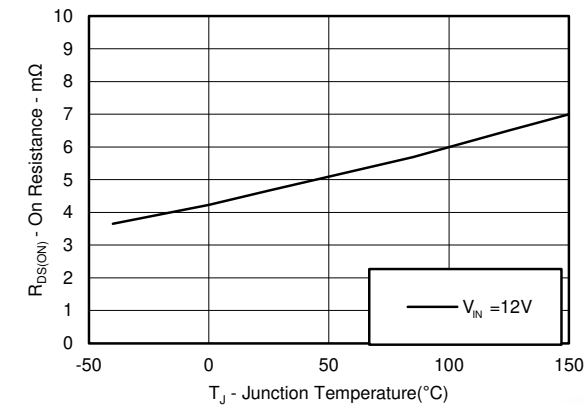


图 6-5. Low-side $R_{DS(on)}$ vs Temperature

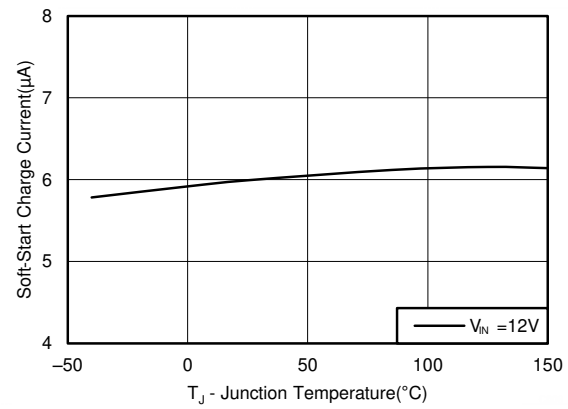


图 6-6. Soft-Start Charge Current vs Temperature

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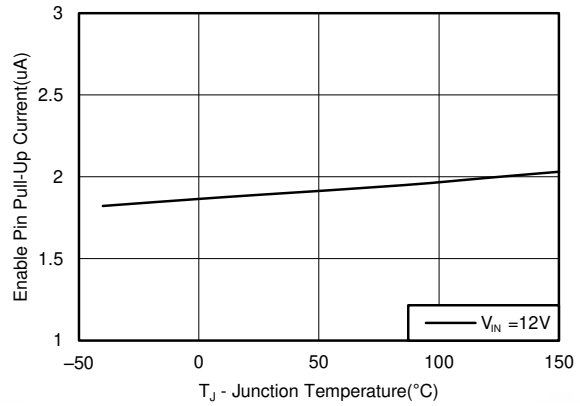


图 6-7. Enable Pullup Current, V_{EN} = 1.0 V

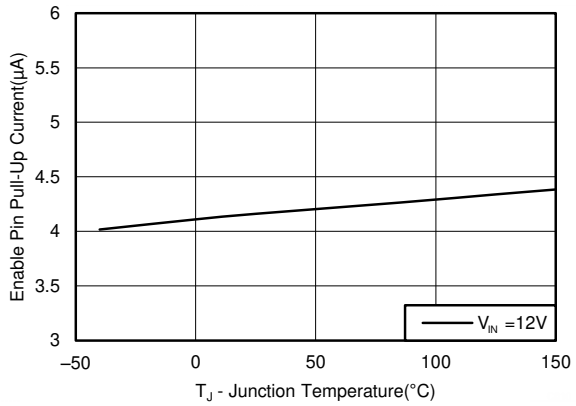


图 6-8. Enable Pullup Current, V_{EN} = 1.3 V

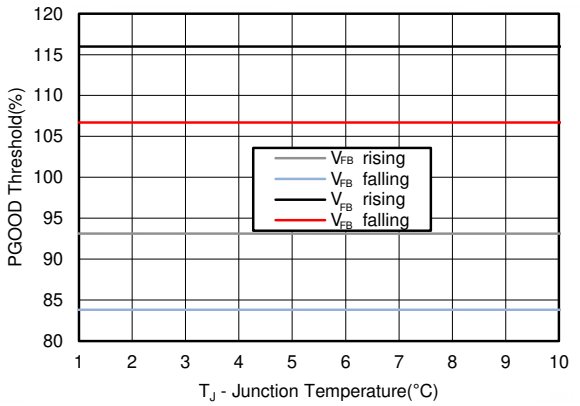


图 6-9. PGOOD Threshold vs Temperature

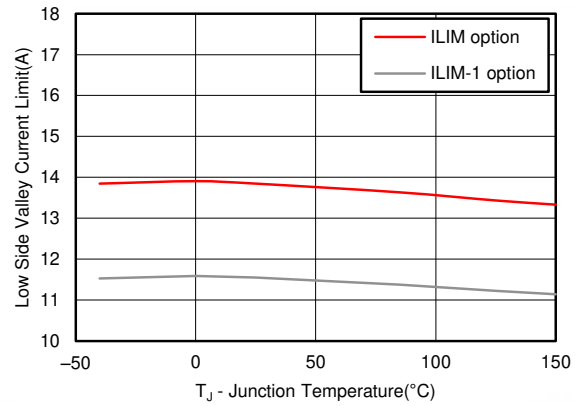


图 6-10. Current Limit vs Temperature

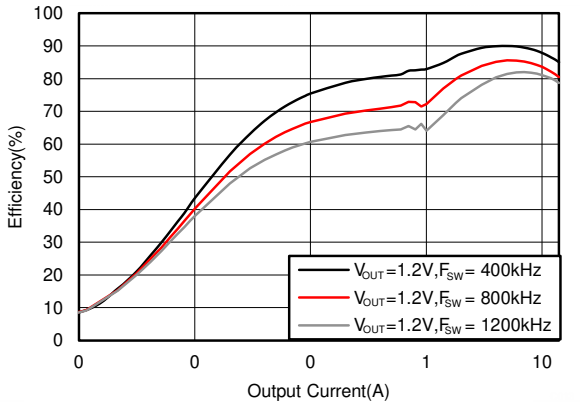


图 6-11. Efficiency with Internal VREG5 = 4.7 V, V_{IN} = 12 V

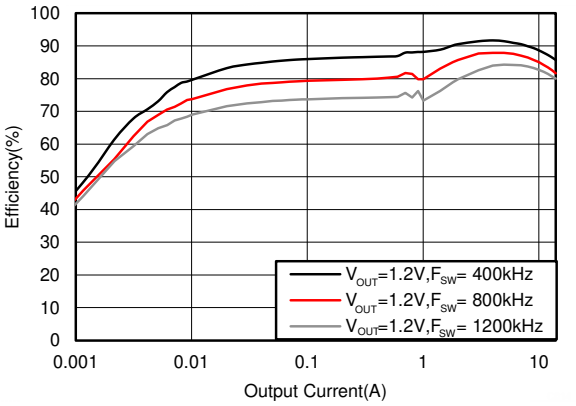


图 6-12. Efficiency with External VREG5 = 5 V, V_{IN} = 12 V

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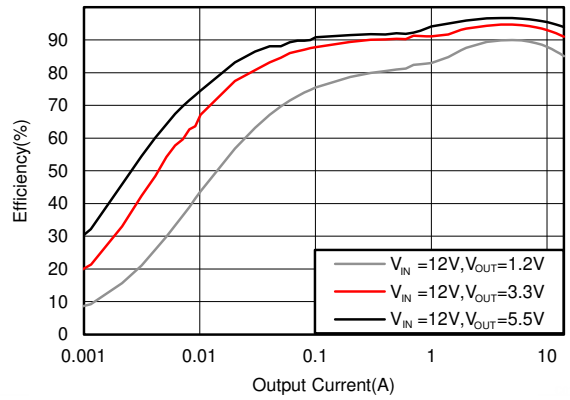


图 6-13. Efficiency, Mode = DCM, F_{SW} = 400 kHz

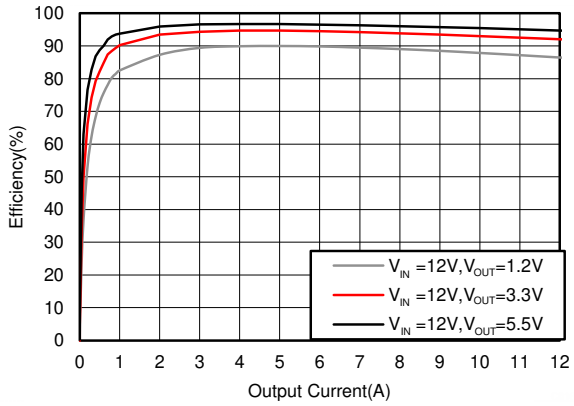


图 6-14. Efficiency, Mode = FCCM, F_{SW} = 400 kHz

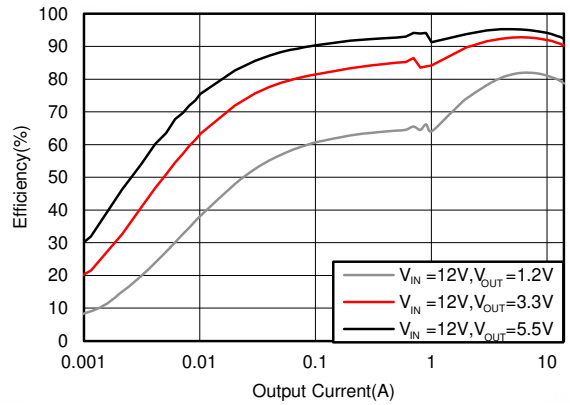


图 6-15. Efficiency, Mode = DCM, F_{SW} = 1200 kHz

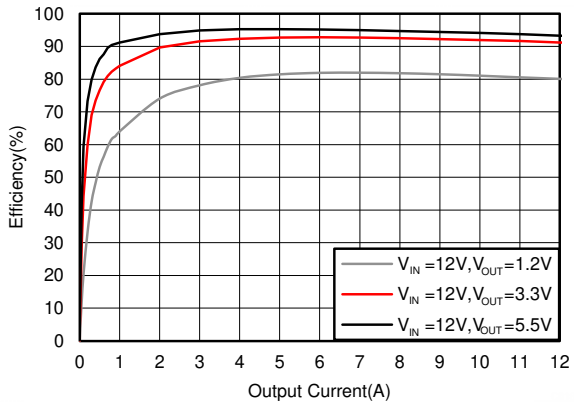


图 6-16. Efficiency, Mode = FCCM, F_{SW} = 1200 kHz

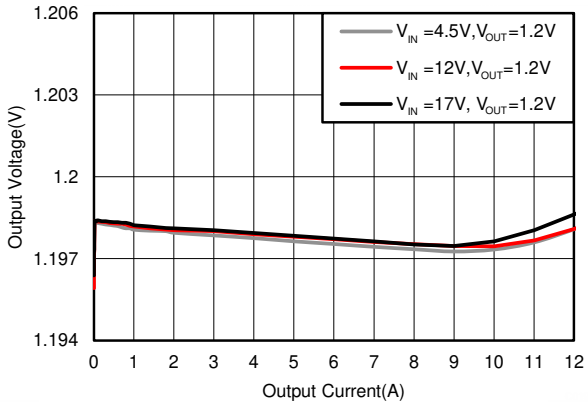


图 6-17. Load Regulation, F_{SW} = 800 kHz

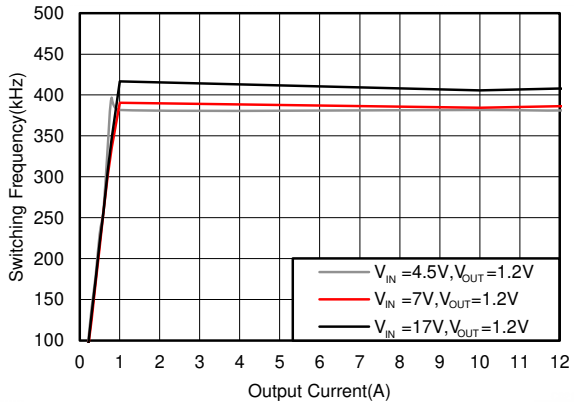


图 6-18. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 400 kHz

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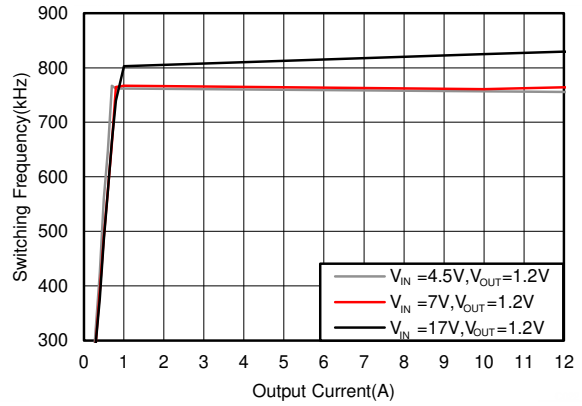


图 6-19. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 800 kHz

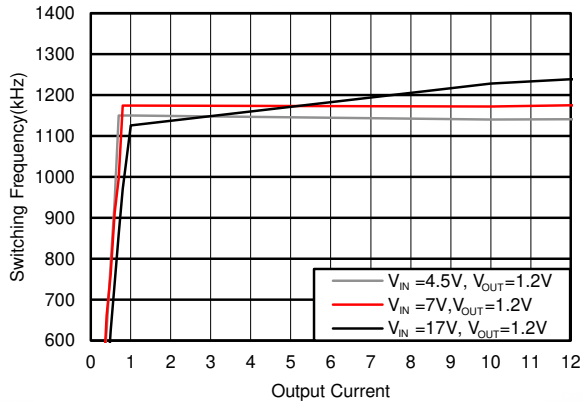


图 6-20. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 1200 kHz

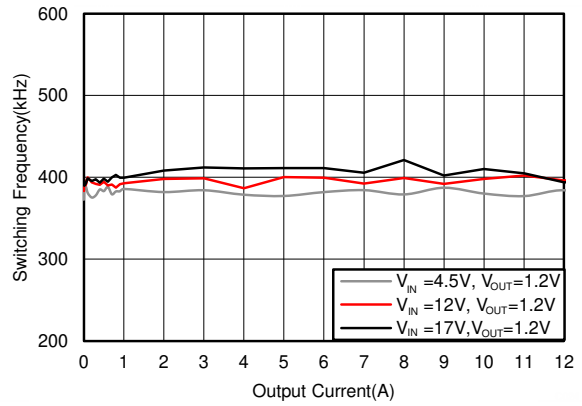


图 6-21. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 400 kHz

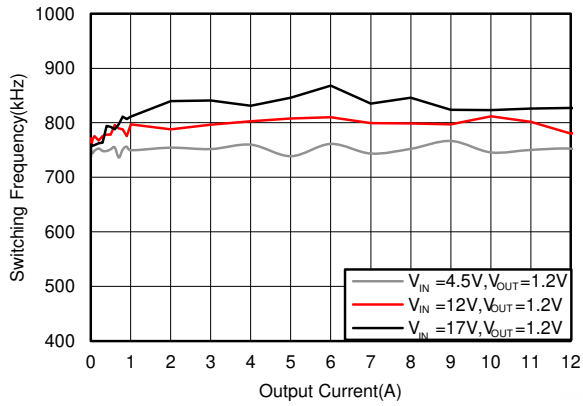


图 6-22. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 800 kHz

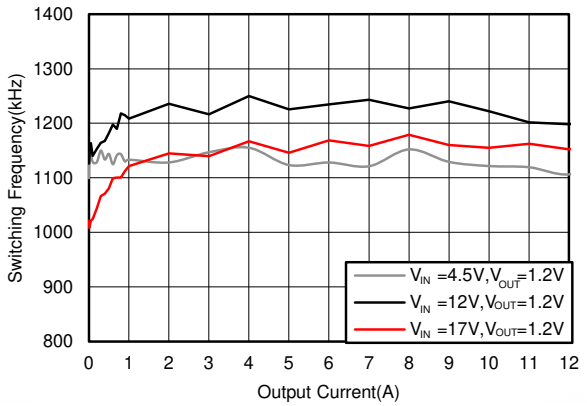


图 6-23. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 1200 kHz

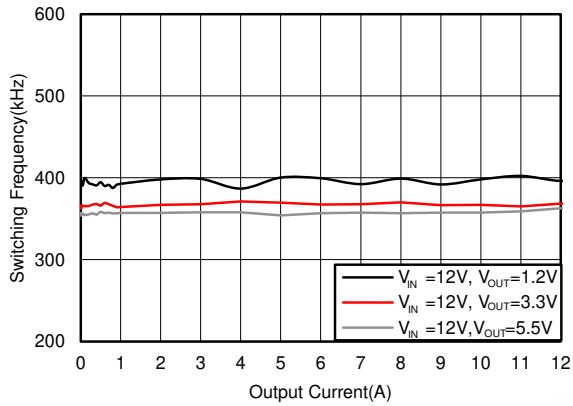


图 6-24. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 400 kHz

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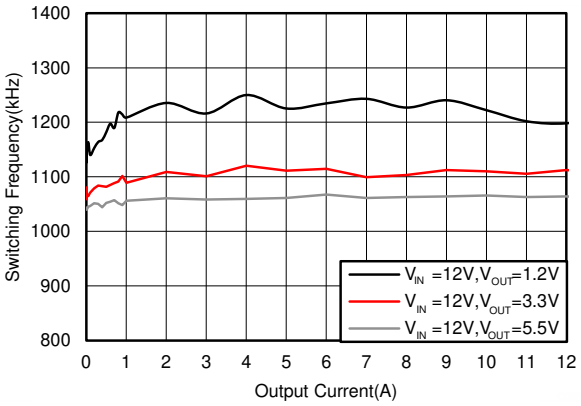


图 6-25. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 1200 kHz

7 Detailed Description

7.1 Overview

The TPS56C215 is a high-density, synchronous, step-down buck converter which can operate from 3.8-V to 17-V input voltage (V_{IN}). The device has 13.5-mΩ and 4.5-mΩ integrated MOSFETs that enable high efficiency up to 12 A. The device employs D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between FCCM operating mode at higher load condition and DCM/Eco-mode operation at lighter load condition. DCM/Eco-mode allows the TPS56C215 to maintain high efficiency at light load. The TPS56C215 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

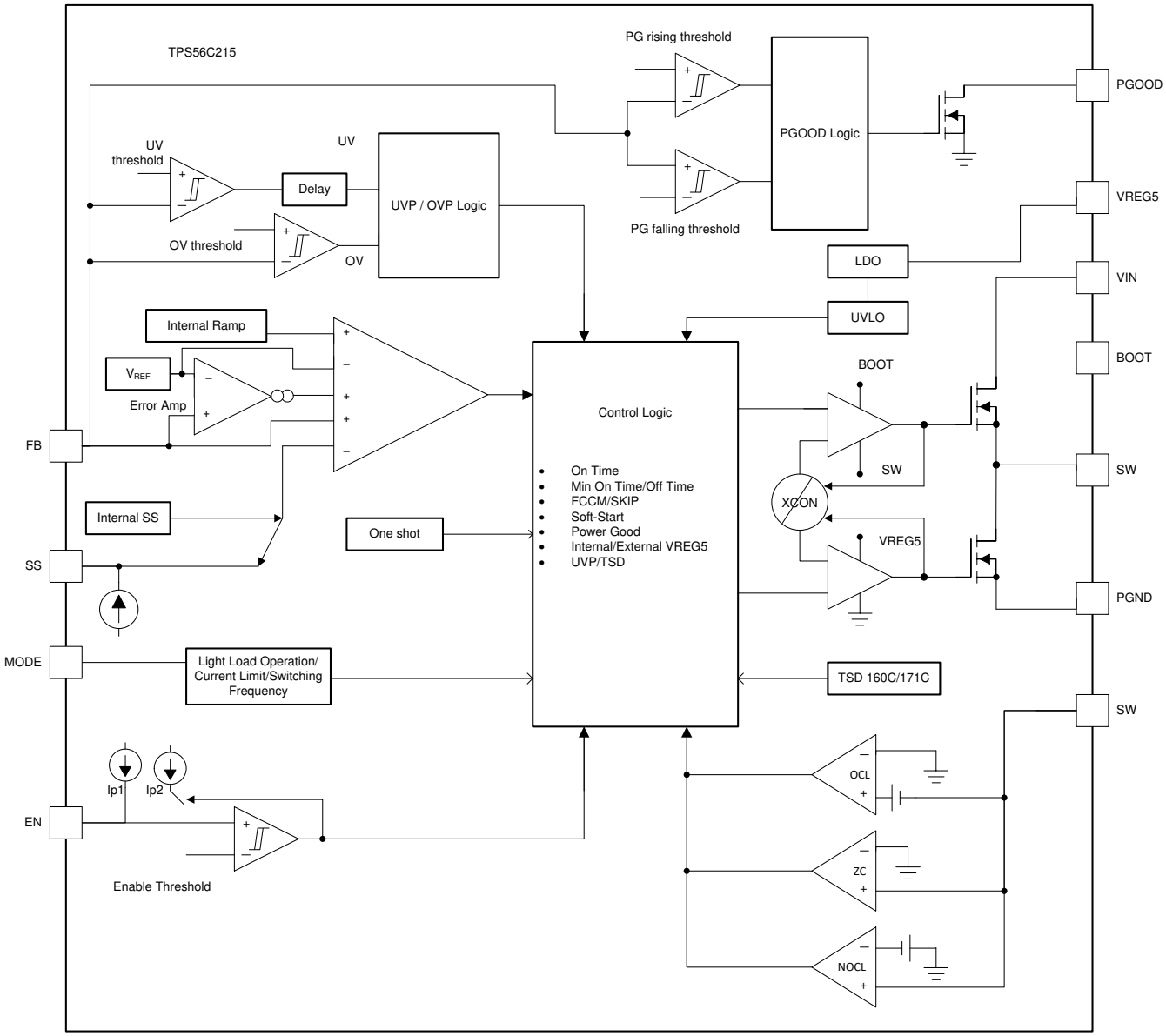
The TPS56C215 has three selectable switching frequencies (F_{SW}) (400 kHz, 800 kHz, and 1200 kHz), which gives the flexibility to optimize the design for higher efficiency or smaller size. There are two selectable current limits. All these options are configured by choosing the right voltage on the MODE pin.

The TPS56C215 has a 4.7-V internal LDO that creates bias for all internal circuitry. There is a feature to overdrive this internal LDO with an external voltage on the VREG5 pin which improves the efficiency of the converter. The undervoltage lockout (UVLO) circuit monitors the VREG5 pin voltage to protect the internal circuitry from low input voltages. The device has an internal pullup current source on the EN pin which can enable the device even with the pin floating.

Soft-start time can be selected by connecting a capacitor to the SS pin. The device is protected from output short, undervoltage, and overtemperature conditions.

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7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation and D-CAP3 Control Mode

The TPS56C215 operates using the adaptive on-time PWM control with a proprietary D-CAP3 control mode which enables low external component count with a fast load transient response while maintaining a good output voltage accuracy. At the beginning of each switching cycle, the high-side MOSFET is turned on for an on-time set by an internal one shot timer. This on-time is set based on the input voltage of the conveter, output voltage of the converter, and the pseudo-fixed frequency, hence this type of control topology is called an adaptive on-time control. The one-shot timer resets and turns on again after the feedback voltage (V_{FB}) falls below the internal reference voltage (V_{REF}). An internal ramp is generated which is fed to the FB pin to simulate the output voltage ripple. This enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3 control topology.

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The TPS56C215 includes an error amplifier that makes the output voltage very accurate. This error amplifier is absent in other flavors of DCAP3. For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS56C215 is a low-pass L-C circuit. This L-C filter has double pole that is described in 方程式 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS56C215. The low frequency L-C double pole has a 180 degree in-phase. At the output filter frequency, the gain rolls off at a –40-dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40-dB to –20-dB per decade and increases the phase to 90 degree one decade above the zero frequency. The internal ripple injection high frequency zero is changed according to the switching frequency selected as shown in 表 7-1. The inductor and capacitor selected for the output filter must be such that the double pole is located close enough to the high-frequency zero so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system must usually be targeted to be less than one-fifth of the switching frequency (F_{SW}).

表 7-1. Ripple Injection Zero

SWITCHING FREQUENCY (kHz)	ZERO LOCATION (kHz)
400	7.1
800	14.3
1200	21.4

表 7-2 lists the inductor values and part numbers that are used to plot the efficiency curves in 节 6.7.

表 7-2. Inductor Values

V_{OUT}(V)	F_{SW}(kHz)	L_{OUT}(µH)	WÜRTH PART NUMBER(1)
1.2	400	1.2	744325120
	800	0.68	744311068
	1200	0.47	744314047
3.3	400	2.4	744325240
	800	1.5	7443552150
	1200	1.2	744325120
5.5	400	3.3	744325330
	800	2.4	744325240
	1200	1.5	7443552150

(1) See Third-Party Products disclaimer.

7.3.2 Eco-mode Control

The TPS56C215 is designed with Eco-mode control to increase efficiency at light loads. This option can be chosen using the MODE pin as shown in 表 7-3. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced enough, the valley of the inductor current reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when a zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept approximately the same as it is in continuous conduction mode. The off-time increases as it takes more time to discharge the output with a smaller load current. The light load current where the transition to Eco-mode operation happens ($I_{OUT(LL)}$) can be calculated from 方程式 2.

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$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the $I_{OUT(max)}$ (peak current in the application). It is also important to size the inductor properly so that the valley current does not hit the negative low-side current limit.

7.3.3 4.7-V LDO

The VREG5 pin is the output of the internal 4.7-V linear regulator that creates the bias for all the internal circuitry and MOSFET gate drivers. The VREG5 pin needs to be bypassed with a 4.7-µF capacitor. An external voltage that is above the internal output voltage of the LDO can override the internal LDO, switching it to the external rail after a higher voltage is detected. This enhances the efficiency of the converter because the quiescent current now runs off this external rail instead of the input power supply. The UVLO circuit monitors the VREG5 pin voltage and disables the output when VREG5 falls below the UVLO threshold. When using an external bias on the VREG5 rail, any power-up and power-down sequencing can be applied but it is important to understand that if there is a discharge path on the VREG5 rail that can pull a current higher than the internal current limit of the LDO (ILIM5) from the VREG5, then the VREG5 LDO turns off thereby shutting down the output of TPS56C215. If such condition does not exist and if the external VREG5 rail is turned off, the VREG5 voltage switches over to the internal LDO voltage which is 4.7 V typically in a few nanoseconds. 图 7-1 shows this transition of the VREG5 voltage from an external bias of 5.5 V to the internal LDO output of 4.7 V when the external bias to VREG5 is disabled while the output of TPS56C215 remains unchanged.

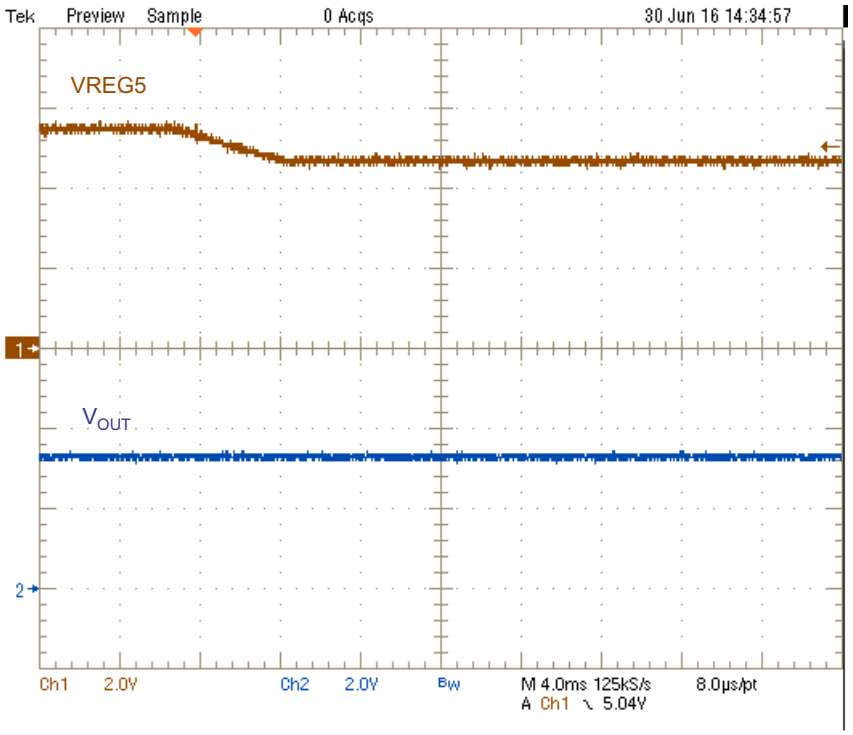


图 7-1. VREG5 Transition

7.3.4 MODE Selection

The TPS56C215 has a MODE pin that can offer 12 different states of operation as a combination of current limit, switching frequency, and light load operation. The device can operate at two different current limits ILIM-1 and ILIM to support an output continuous current of 10 A and 12 A, respectively. The TPS56C215 is designed to compare the valley current of the inductor against the current limit thresholds so understand that the output

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current is half the ripple current higher than the valley current. For example, with the ILIM current limit selection, the OCL threshold is 11.73-A minimum, which means that a pk-pk inductor ripple current of 0.54-A minimum is needed to be able to draw 12 A out of the converter without entering an overcurrent condition. The TPS56C215 can operate at three different frequencies of 400 kHz, 800 kHz, and 1200 kHz and also can choose between Eco-mode and FCCM mode. The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options listed in 表 7-3. The voltage on the MODE pin can be set by connecting this pin to the center tap of a resistor divider connected between VREG5 and AGND. A guideline for the top resistor (R_{M_H}) and the bottom resistor (R_{M_L}) in 1% resistors is shown in 表 7-3. It is important that the voltage for the MODE pin is derived from the VREG5 rail only because internally this voltage is referenced to detect the MODE option. The MODE pin setting can be reset only by a VIN power cycling.

表 7-3. MODE Pin Resistor Settings

R_{M_L} (kΩ)	R_{M_H} (kΩ)	LIGHT LOAD OPERATION	CURRENT LIMIT	FREQUENCY (kHz)
5.1	300	FCCM	ILIM-1	400
10	200	FCCM	ILIM	400
20	160	FCCM	ILIM-1	800
20	120	FCCM	ILIM	800
51	200	FCCM	ILIM-1	1200
51	180	FCCM	ILIM	1200
51	150	DCM	ILIM-1	400
51	120	DCM	ILIM	400
51	91	DCM	ILIM-1	800
51	82	DCM	ILIM	800
51	62	DCM	ILIM-1	1200
51	51	DCM	ILIM	1200

图 7-2 shows the typical start-up sequence of the device after the EN pin voltage crosses the EN turn-on threshold. After the voltage on VREG5 pin crosses the rising UVLO threshold, it takes 100 µs to read the first MODE setting and approximately 100 µs from there to finish the last MODE setting. The output voltage starts ramping after the MODE setting reading is completed.

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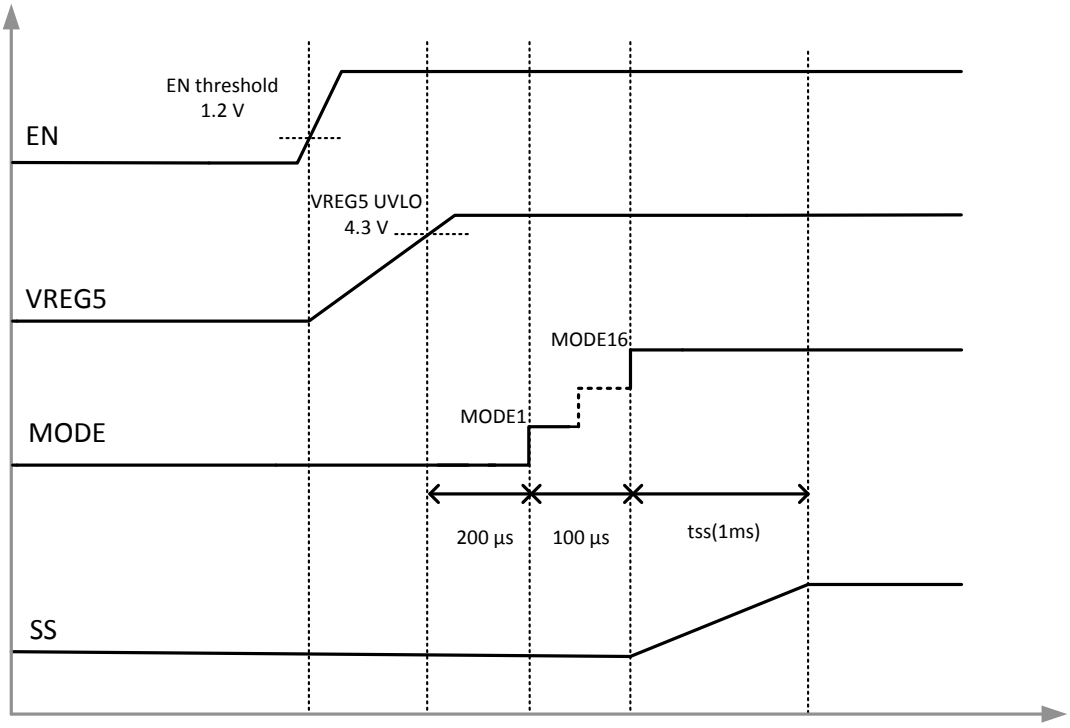


图 7-2. Power-Up Sequence

7.3.5 Soft Start and Pre-biased Soft Start

The TPS56C215 has an adjustable soft start time that can be set by connecting a capacitor on SS pin. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected between SS and AGND. The devices tracks the lower of the internal soft-start voltage or the external soft-start voltage as the reference. The equation for the soft-start time (T_{SS}) is shown in 方程式 3:

$$T_{SS(S)} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (3)$$

where

- V_{REF} is 0.6 V and I_{SS} is 6 µA

If the output capacitor is pre-biased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.6 Enable and Adjustable UVLO

The EN pin controls the turnon and turnoff of the device. When EN pin voltage is above the turnon threshold which is around 1.2 V, the device starts switching and when the EN pin voltage falls below the turnoff threshold, which is around 1.1 V, it stops switching. If the user application requires a different turnon (V_{START}) and turnoff thresholds (V_{STOP}) respectively, the EN pin can be configured as shown in 图 7-3 by connecting a resistor divider between VIN and EN. The EN pin has a pullup current I_{p1} that sets the default state of the pin when it is floating. This current increases to I_{p2} when the EN pin voltage crosses the turnon threshold. The UVLO thresholds can be set by using 方程式 4 and 方程式 5.

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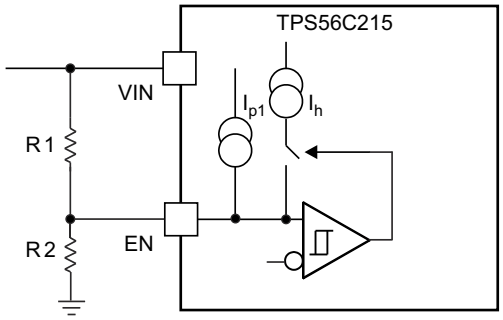


图 7-3. Adjustable VIN Undervoltage Lock Out

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_{p1}\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (4)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1\ I_{p2}} \quad (5)$$

where

- I_{p2} = 4.197 μA
- I_{p1} = 1.91 μA
- I_h = 2.287 μA
- $V_{ENRISING}$ = 1.225 V
- $V_{ENFALLING}$ = 1.104 V

7.3.7 Power Good

The Power Good (PGOOD) pin is an open-drain output. Once the FB pin voltage is between 93% and 107% of the internal reference voltage (V_{REF}), the PGOOD is de-asserted and floats after a 200-μs de-glitch time. A pullup resistor of 10 kΩ is recommended to pull it up to VREG5. The PGOOD pin is pulled low when the FB pin voltage is lower than V_{UVP} or greater than V_{OVP} threshold, in an event of thermal shutdown, or during the soft-start period

7.3.8 Overcurrent Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by input voltage, output voltage, the on-time, and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the measured drain-to-source voltage of the low-side FET is above the voltage proportional to current limit, the low-side FET stays on until the current level becomes lower than the OCL level which reduces the output current available. When the current is limited the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 68% of the target voltage, the UVP comparator detects it and shuts down the device after a wait time of 1 ms, the device re-starts after a hiccup time of 7 ms. In this type of valley detect control, the load current is higher than the OCL threshold by one half of the peak-to-peak inductor ripple current. When the overcurrent condition is removed, the output voltage returns to the regulated value. If an OCL condition happens during start-up, then the device enters hiccup-mode immediately without a wait time of 1 ms.

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7.3.9 Out-of-Bounds Operation

The device has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault. OOB protection operates as an early no-fault overvoltage protection mechanism. During the OOB operation, the controller operates in forced PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly toward the setpoint. During the operation, the cycle-by cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

7.3.10 UVLO Protection

Undervoltage lockout protection (UVLO) monitors the internal VREG5 regulator voltage. When the VREG5 voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.11 Thermal Shutdown

The device monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (T_{SDN} typically 160°C), the device shuts off. This is a non-latch protection. During start-up, if the device temperature is higher than 160°C, the device does not start switching and does not load the MODE settings. If the device temp goes higher than T_{SDN} threshold after start-up, it stops switching with SS reset to ground and an internal discharge switch turns on to quickly discharge the output voltage. The device re-starts switching when the temperature goes below the thermal shutdown threshold but the MODE settings are not re-loaded again.

There is a second higher thermal protection on the device $T_{SDN\ VREG5}$ which protects it from overtemperature conditions not caused by the switching of the device itself. This threshold is at typically 170°C. Even under non-switching condition of the device after exceeding T_{SDN} threshold, if it still continues to heat up the VREG5 output shuts off after temperature goes beyond $T_{SDN\ VREG5}$, thereby shutting down the device completely.

7.3.12 Output Voltage Discharge

The device has a 500-Ω discharge switch that discharges the output V_{OUT} through SW node during any event of fault like output overvoltage, output undervoltage, TSD, if VREG5 voltage below the UVLO and when the EN pin voltage (V_{EN}) is below the turnon threshold.

7.4 Device Functional Modes

7.4.1 Light Load Operation

When the MODE pin is selected to operate in FCCM mode, the converter operates in continuous conduction mode (FCCM) during light-load conditions. During FCCM, the switching frequency (F_{SW}) is maintained at an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load. If the MODE pin is selected to operate in DCM/Eco-mode, the device enters pulse skip mode after the valley of the inductor ripple current crosses zero. The Eco-mode maintains higher efficiency at light load with a lower switching frequency.

7.4.2 Standby Operation

The TPS56C215 can be placed in standby mode by pulling the EN pin low. The device operates with a shut-down current of 7 μA when in standby condition.

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8 Application and Implementation

备注

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8.1 Application Information

The schematic of 图 8-1 shows a typical application for TPS56C215. This design converts an input voltage range of 4.5 V to 17 V down to 1.2 V with a maximum output current of 12 A.

8.2 Typical Application

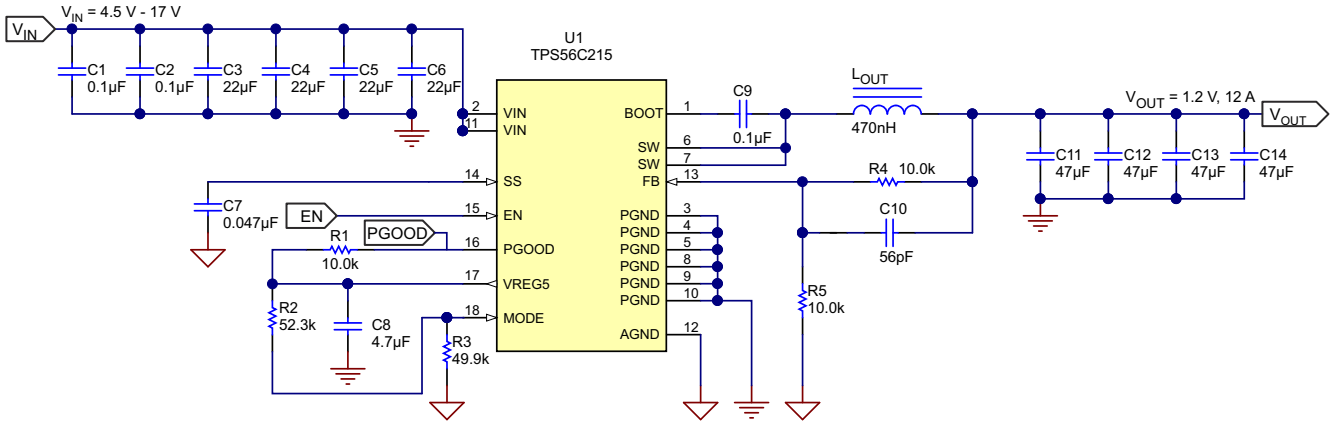


图 8-1. Application Schematic

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			1.2		V
I_{OUT}	Output current			12		A
ΔV_{OUT}	Transient response	9-A load step		40		mV
V_{IN}	Input voltage		4.5	12	17	V
$V_{OUT(ripple)}$	Output voltage ripple			20		$mV_{(P-P)}$
	Start input voltage	Input voltage rising		Internal UVLO		V
	Stop input voltage	Input voltage falling		Internal UVLO		V
F_{SW}	Switching frequency			1.2		MHz
Operating Mode				DCM		
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 External Component Selection

8.2.2.1.1 Output Voltage Set Point

To change the output voltage of the application, it is necessary to change the value of the upper feedback resistor. By changing this resistor the user can change the output voltage above 0.6 V. See 方程式 6.

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$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{UPPER}}{R_{LOWER}}\right) \quad (6)$$

8.2.2.1.2 Switching Frequency and MODE Selection

Switching Frequency, current limit, and switching mode (DCM or FCCM) are set by a voltage divider from VREG5 to GND connected to the MODE pin. See 表 7-3 for possible MODE pin configurations. Switching frequency selection is a tradeoff between higher efficiency and smaller system solution size. Lower switching frequency yields higher overall efficiency but relatively bigger external components. Higher switching frequencies cause additional switching losses which impact efficiency and thermal performance. For this design, 1.2 MHz is chosen as the switching frequency, the switching mode is DCM and the output current is 12 A.

8.2.2.1.3 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor must have a ripple current rating higher than the inductor ripple current. See 表 8-2 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using 方程式 7 and 方程式 8. It is important that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}}\right)^2} \quad (7)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (8)$$

During transient/short circuit conditions the inductor current can increase up to the current limit of the device so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

8.2.2.1.4 Output Capacitor Selection

After selecting the inductor, the output capacitor needs to be optimized. In DCAP3, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in 表 8-2

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor must be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$.

表 8-2. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	F_{SW} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	C_{FF} (pF)
0.6	10	0	400	0.68	300	500	–
			800	0.47	100	500	–
			1200	0.33	88	500	–
1.2		10	400	1.2	100	500	–
			800	0.68	88	500	–
			1200	0.47	88	500	–
3.3		45.3	400	2.4	88	500	100 – 220
			800	1.5	88	500	100 – 220
			1200	1.2	88	500	100 – 220

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表 8-2. Recommended Component Values (continued)

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	F_{SW} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	C_{FF} (pF)
5.5		82.5	400	3.3	88	500	100 – 220
			800	2.4	88	500	100 – 220
			1200	1.5	88	700	100 – 220

8.2.2.1.5 Input Capacitor Selection

The minimum input capacitance required is given in 方程式 9.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (9)$$

TI recommends using a high quality X5R or X7R input decoupling capacitors of 40 µF on the input voltage pin. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by 方程式 10:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \quad (10)$$

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8.2.3 Application Curves

图 8-2 through 图 8-18 apply to the circuit of 图 8-1. V_{IN} = 12 V. T_a = 25°C unless otherwise specified.

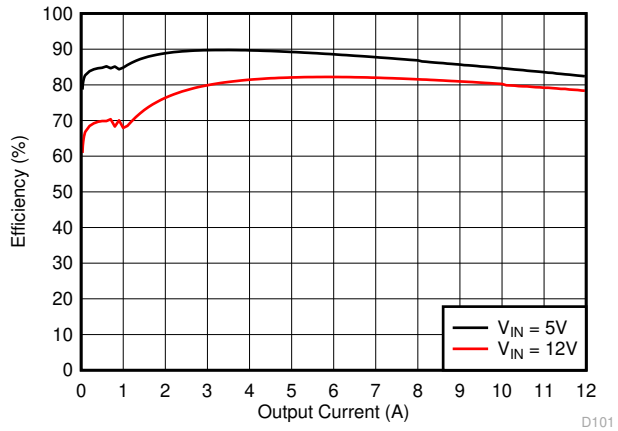


图 8-2. Efficiency

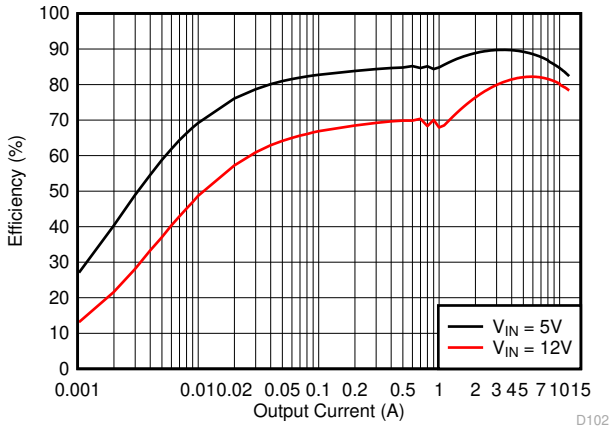


图 8-3. Light Load Efficiency

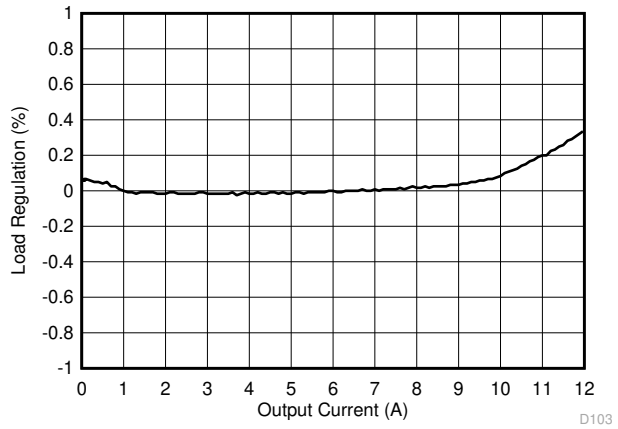


图 8-4. Load Regulation, V_{IN} = 5 V

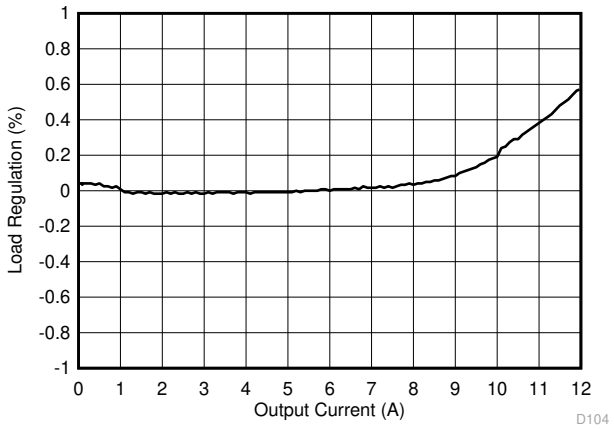


图 8-5. Load Regulation, V_{IN} = 12 V

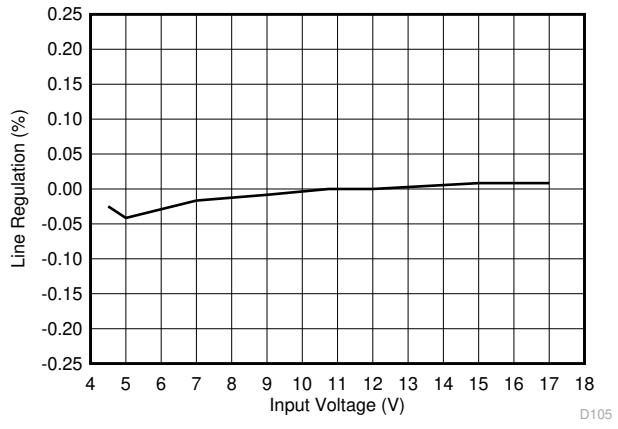


图 8-6. Line Regulation, I_{OUT} = 6 A

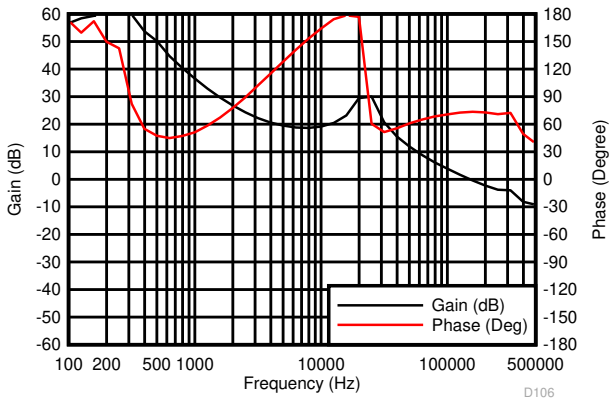


图 8-7. Loop Response, I_{OUT} = 6 A

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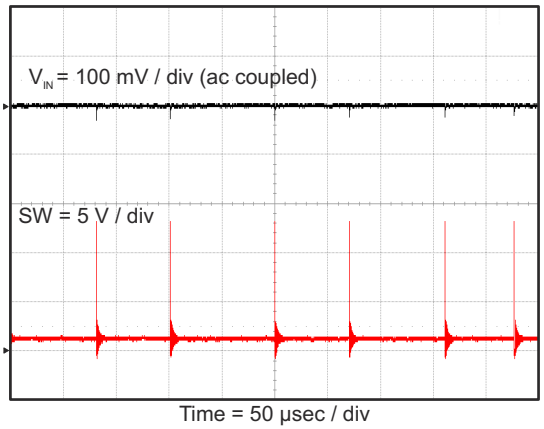


图 8-8. Input Voltage Ripple, I_{OUT} = 10 mA

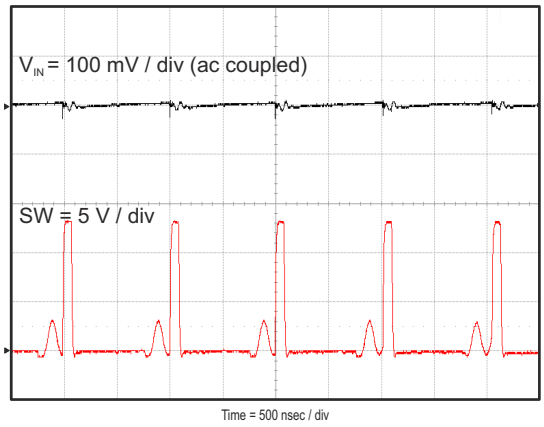


图 8-9. Input Voltage Ripple, I_{OUT} = 800 mA

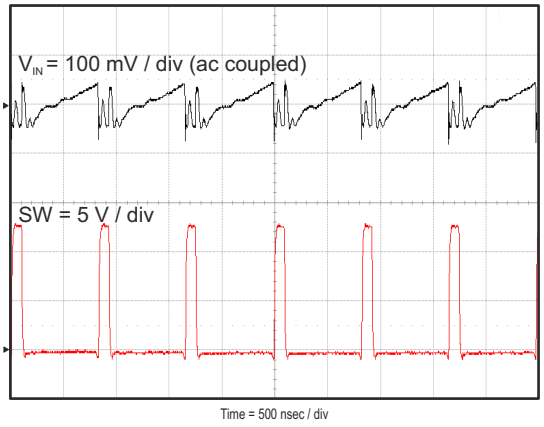


图 8-10. Input Voltage Ripple, I_{OUT} = 12 A

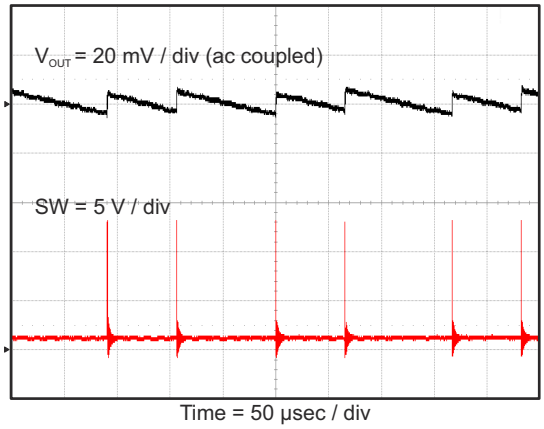


图 8-11. Output Voltage Ripple, I_{OUT} = 10 mA

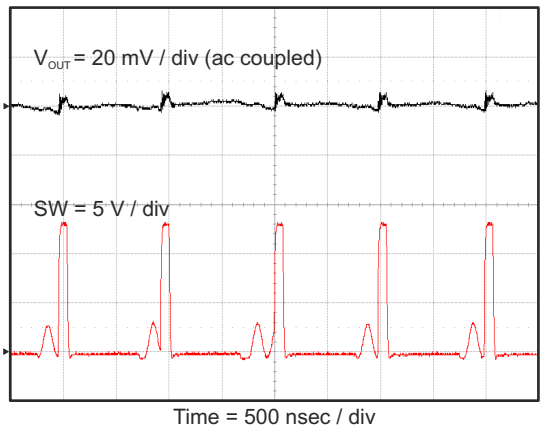


图 8-12. Output Voltage Ripple, I_{OUT} = 800 mA

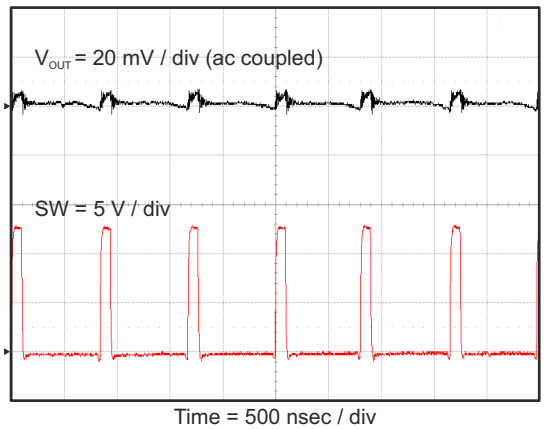


图 8-13. Output Voltage Ripple, I_{OUT} = 12 A

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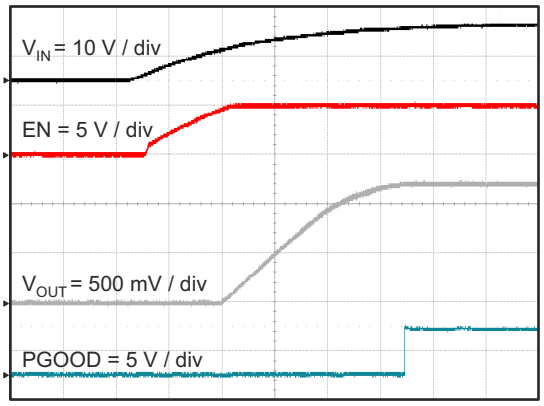


图 8-14. Start Up Relative to V_{IN} Rising

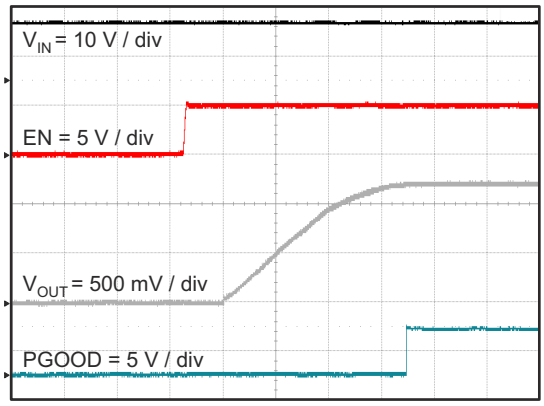


图 8-15. Start Up Relative to EN Rising

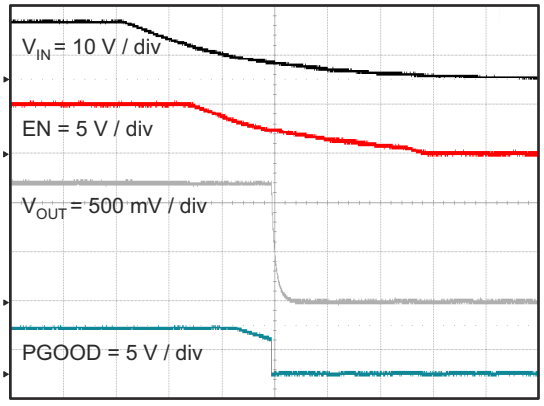


图 8-16. Shut Down Relative to V_{IN} Falling

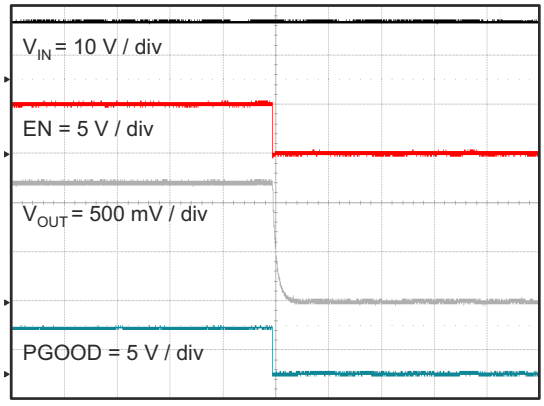


图 8-17. Shut Down Relative to EN Falling

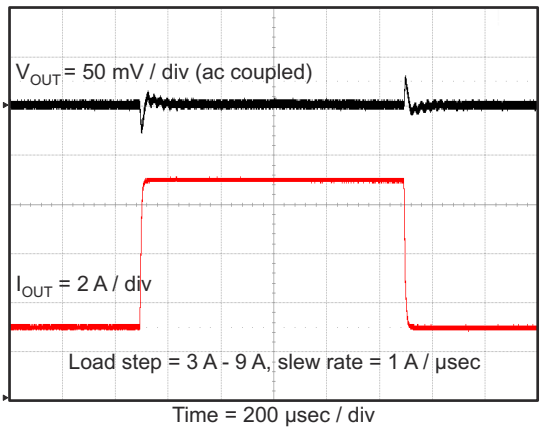


图 8-18. Transient Response

8.3 Power Supply Recommendations

The TPS56C215 is intended to be powered by a well regulated dc voltage. The input voltage range is 3.8 to 17 V. TPS56C215 is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS56215 circuit, some additional input bulk capacitance is recommended. Typical values are 100 µF to 470 µF.

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8.4 Layout

8.4.1 Layout Guidelines

- Recommend a four-layer or six-layer PCB for good thermal performance and with maximum ground plane. 3" × 3", four-layer PCB with 2-oz. copper used as example.
- Recommend having equal caps on each side of the IC. Place them right across VIN as close as possible.
- Inner layer 1 is ground with the PGND to AGND net tie
- Inner layer2 has VIN copper pour that has vias to the top layer VIN. *Place multiple vias under the device near VIN and PGND and near input capacitors* to reduce parasitic inductance and improve thermal performance
- Bottom later is GND with the BOOT trace routing.
- Reference feedback to the quite AGND and routed away from the switch node.
- Make VIN trace wide to reduce the trace impedance.

8.4.2 Layout Example

图 8-19 shows the recommended top side layout. Component reference designators are the same as the circuit shown in 图 8-1. Resistor divider for EN is not used in the circuit of 图 8-1, but are shown in the layout for reference.

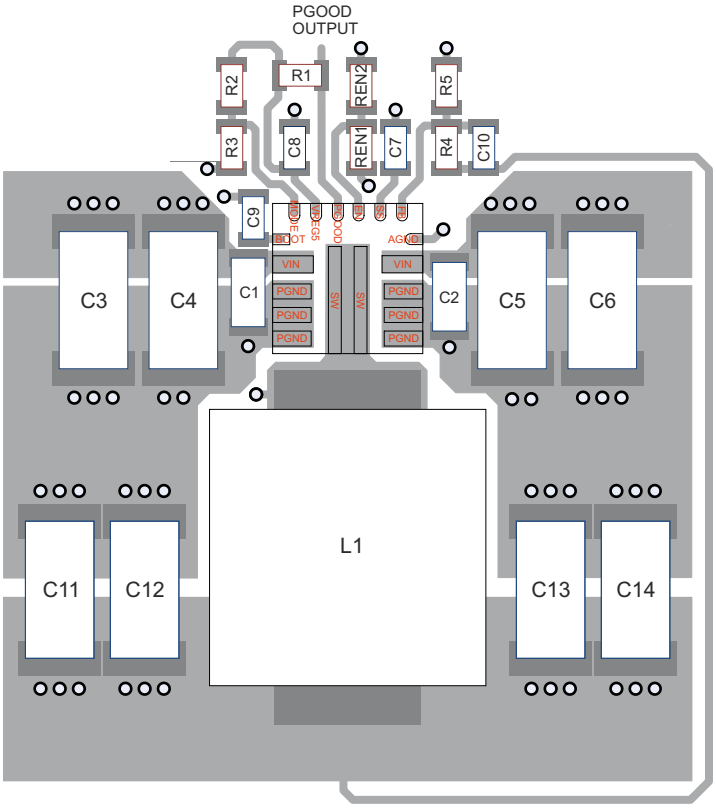


图 8-19. Top Side Layout

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图 8-20 shows the recommended layout for the first internal layer. It is comprised of a large PGND plane and a smaller ANGD island. AGND and PGND are connected at a single point to reduce circulating currents.

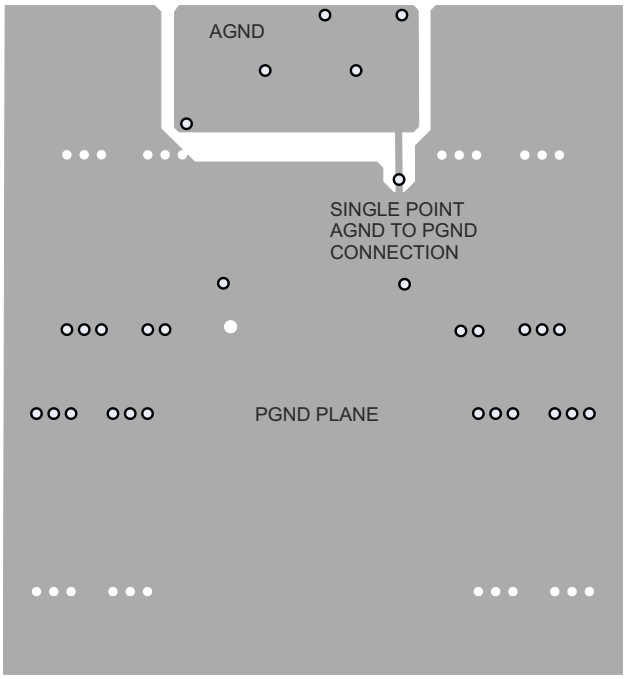


图 8-20. Mid Layer 1 Layout

图 8-21 shows the recommended layout for the second internal layer. It is comprised of a large PGND plane, a smaller copper fill area to connect the two top side V_{IN} copper areas and a second V_{OUT} copper fill area.

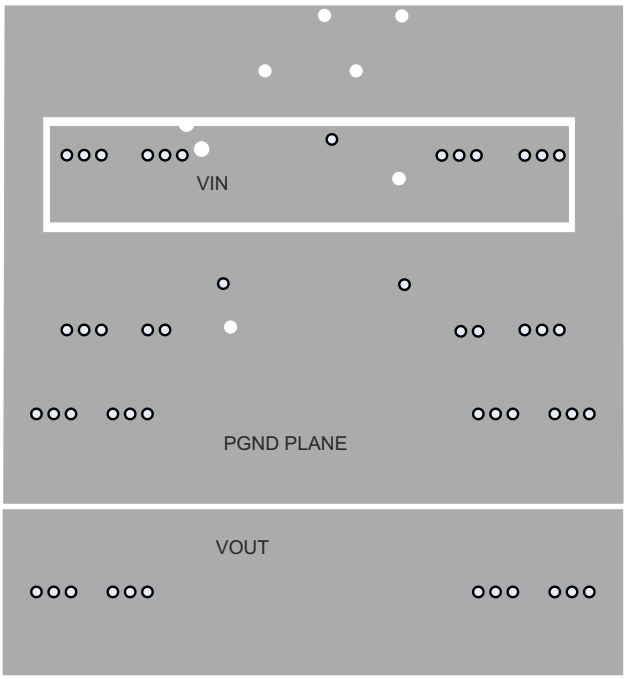


图 8-21. Mid Layer 2 Layout

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图 8-22 shows the recommended layout for the bottom layer. It is comprised of a large PGND plane and a trace to connect the BOOT capacitor to the SW node.

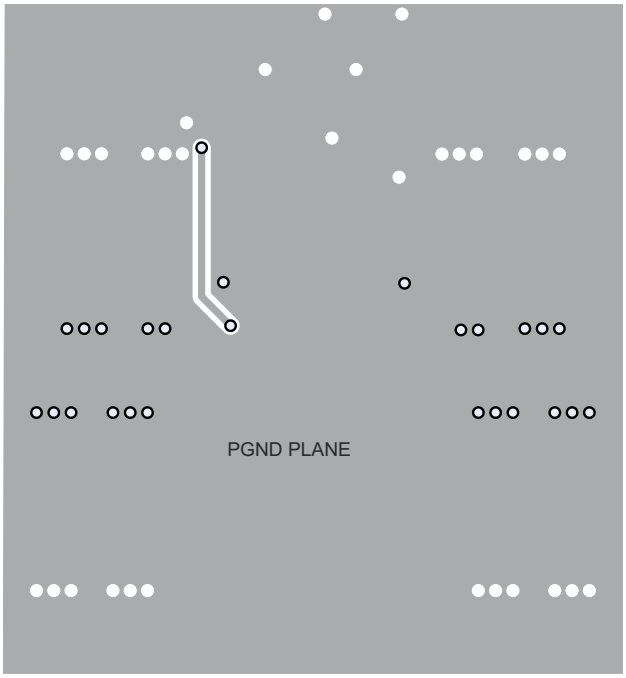


图 8-22. Bottom Layer Layout

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9 Device and Documentation Support

9.1 Device Support

9.1.1 第三方产品免责声明

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9.1.2 Development Support

The evaluation module for system validation in shown in 图 9-1.

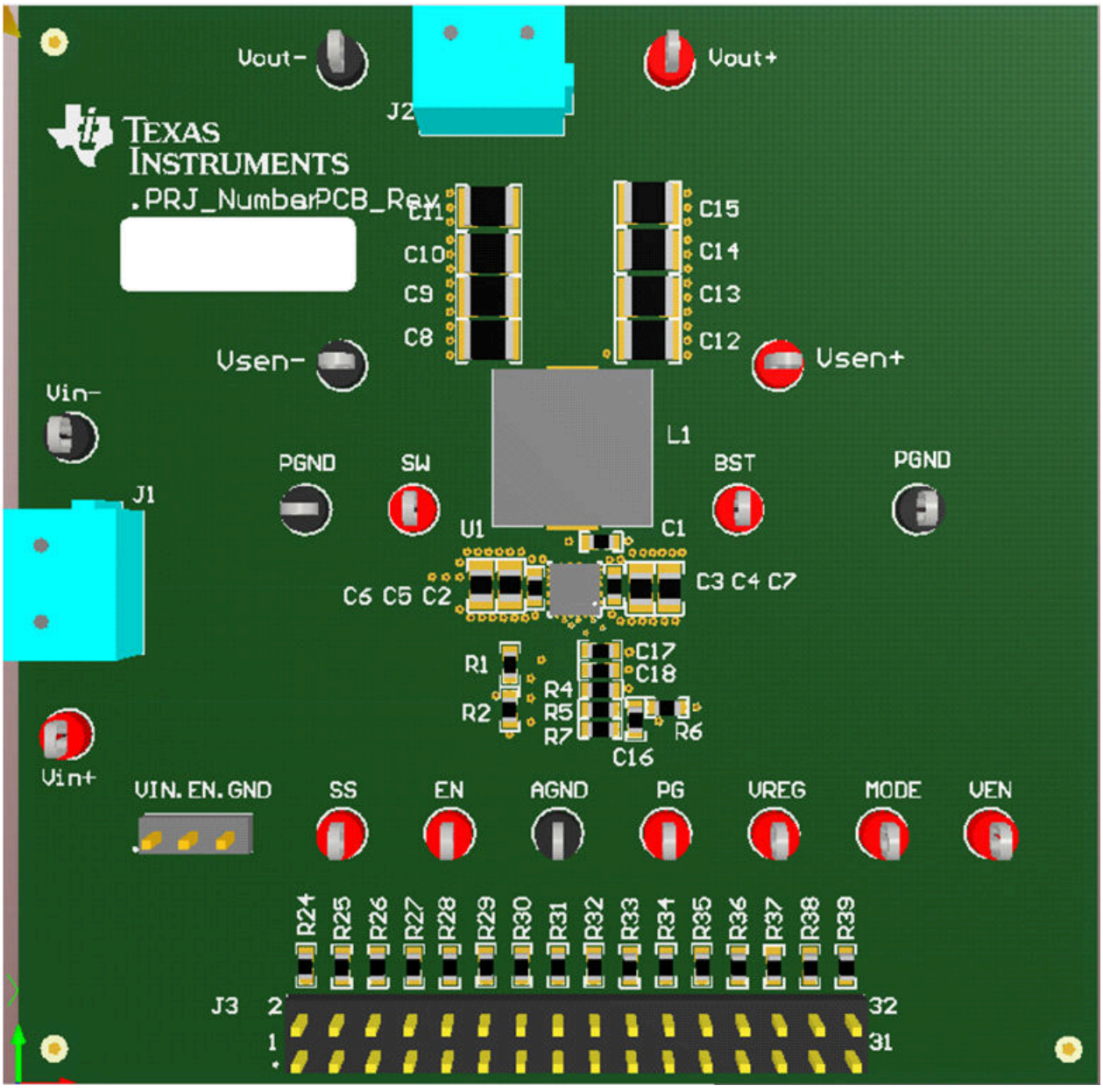


图 9-1. System Validation EVM Board

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

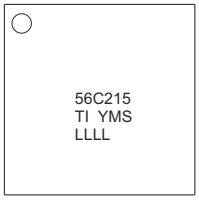
TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Package Marking



TI = TI Letters
YM = Year Month Date Code
S = Assembly Site Code
LLLL = Assembly Lot Code

Y : Year Code (1, 2, 3, 4, 5, 6, 7, 8, 9, 0)
M : Month Code (1, 2, 3, 4, 5, 6, 7, 8, 9, 0, A, B, C)

图 10-1. Symbolization

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS56C215RNNR	ACTIVE	VQFN-HR	RNN	18	3000	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR	-40 to 125	56C215	Samples
TPS56C215RNNT	ACTIVE	VQFN-HR	RNN	18	250	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR	-40 to 125	56C215	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

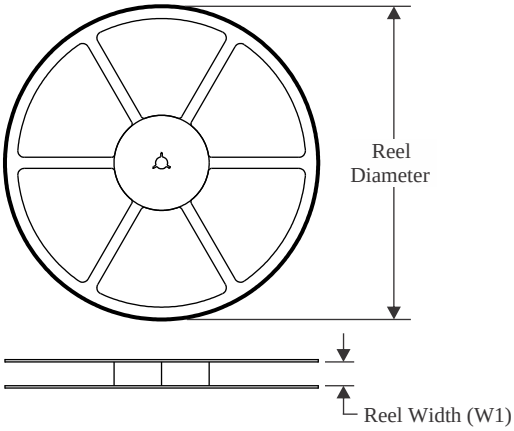
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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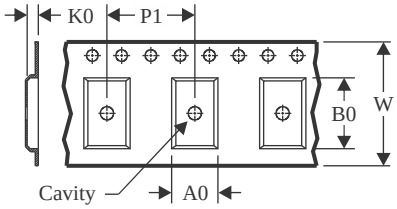
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

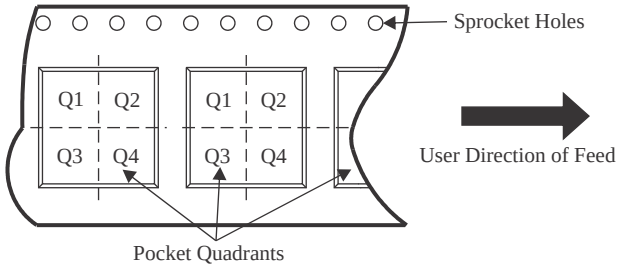


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

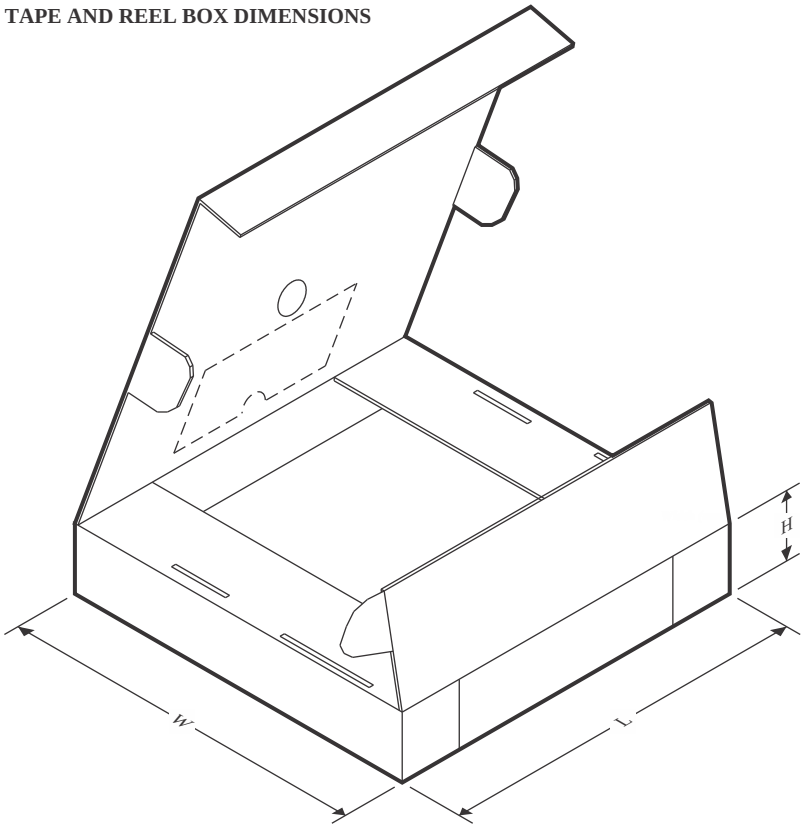
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56C215RNNT	VQFN-HR	RNN	18	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS56C215RNNT	VQFN-HR	RNN	18	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

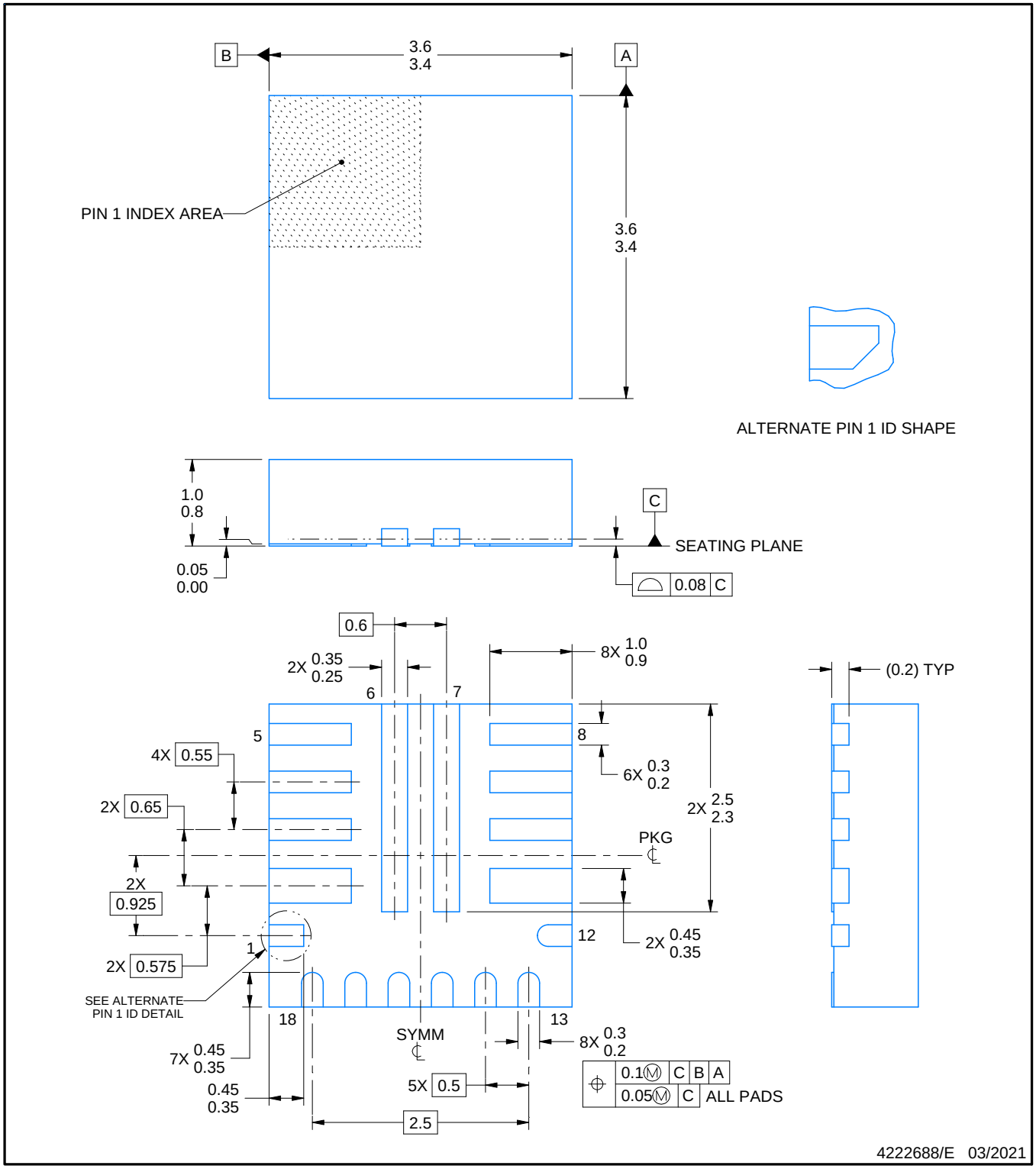
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56C215RNNT	VQFN-HR	RNN	18	250	210.0	185.0	35.0
TPS56C215RNNT	VQFN-HR	RNN	18	250	213.0	191.0	35.0

PACKAGE OUTLINE

RNN0018A

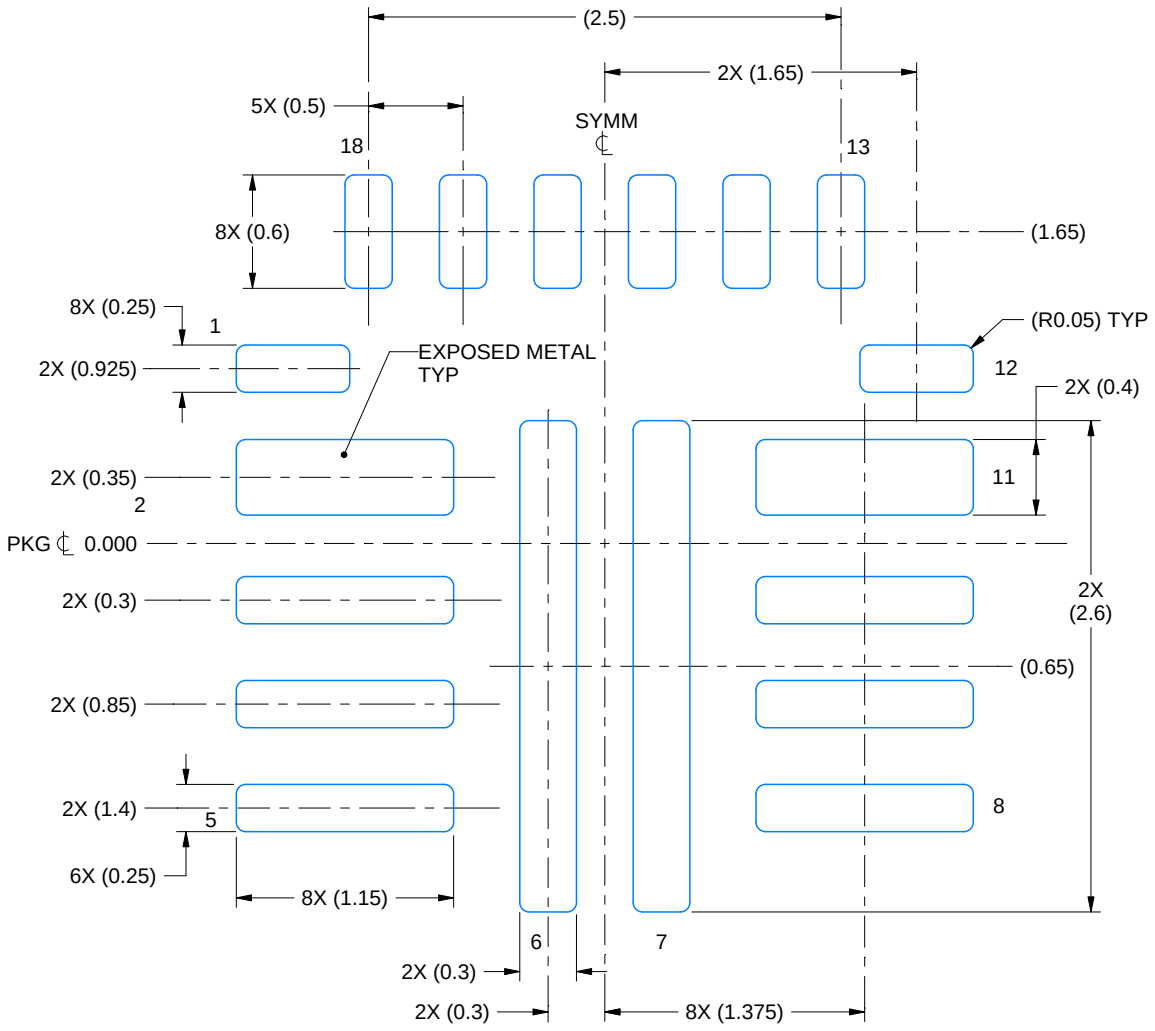
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

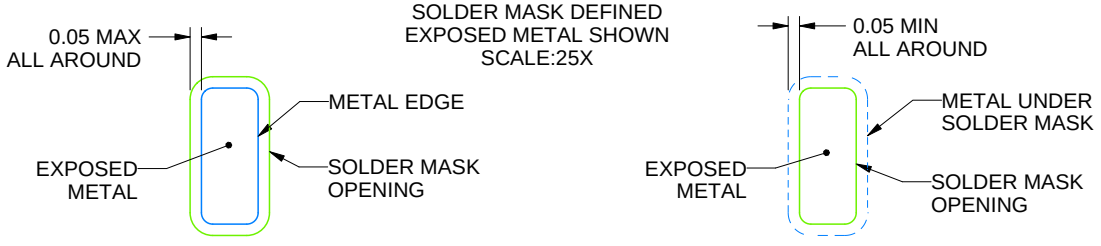


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
EXPOSED METAL SHOWN
SCALE:25X



NON SOLDER MASK DEFINED (PREFERRED)

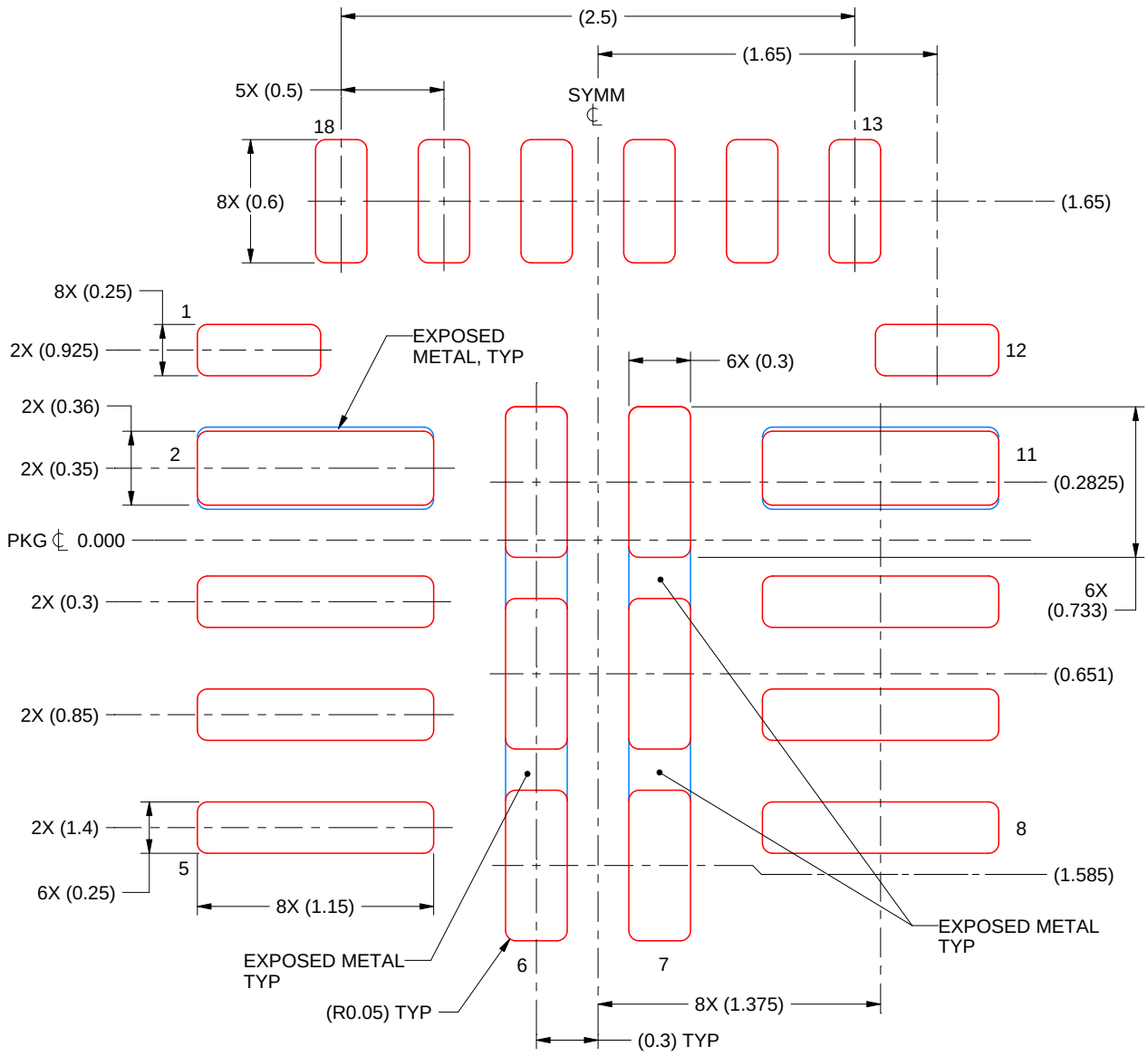
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4222688/E 03/2021

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 7: 83% - PADS 2 & 11: 90%
SCALE:30X

4222688/E 03/2021

NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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