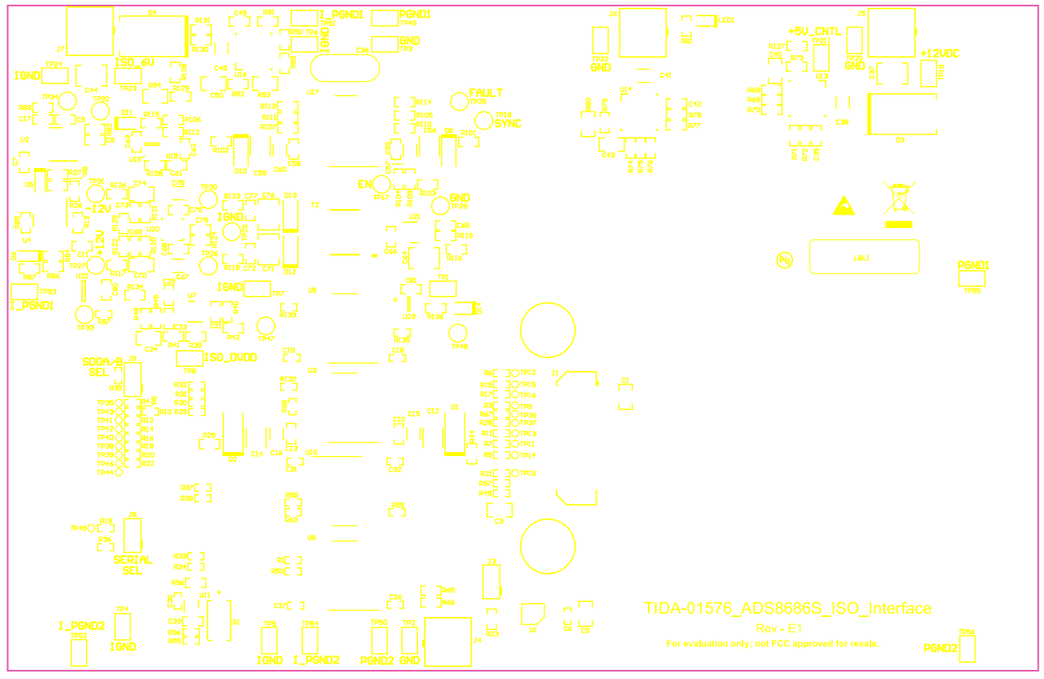
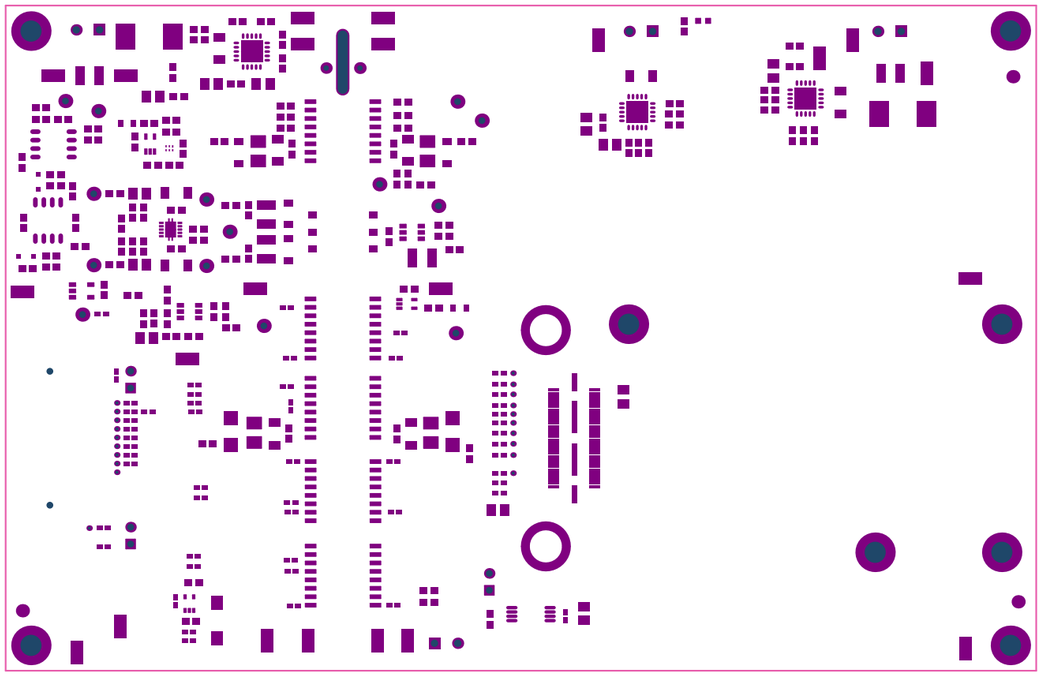
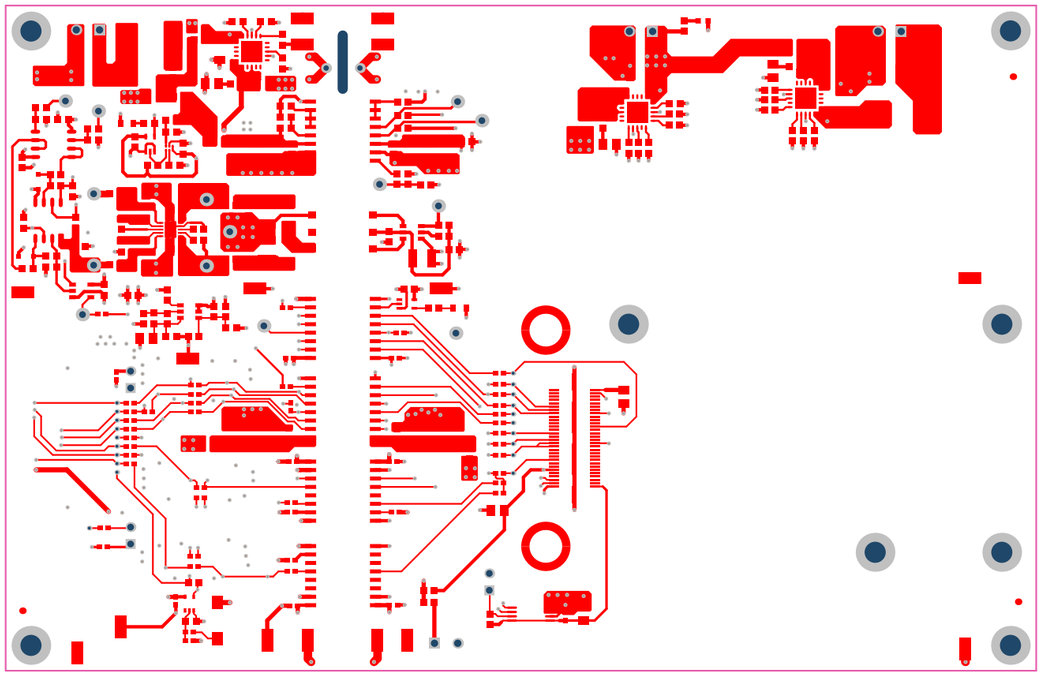


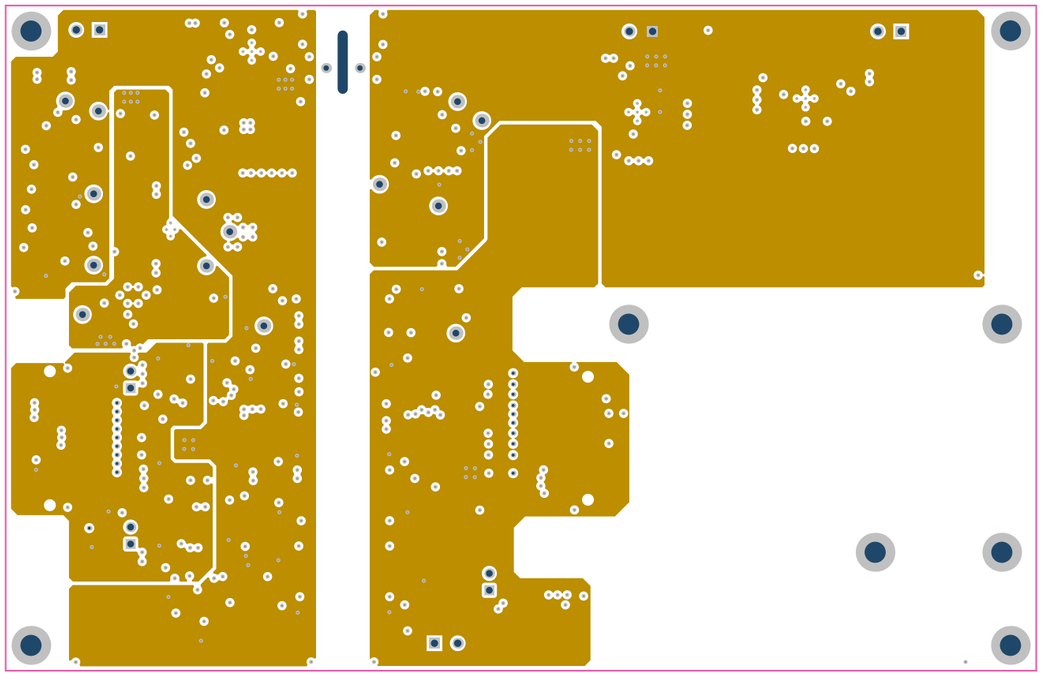
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01576_ADS8686S_ISO_Interface		SVN REV: Not In VersionControl
LAYER NAME = Top Overlay	TID #: 01576		
PLOT NAME = Top Overlay	GENERATED : 4/6/2020 3:41:38 PM		TEXAS INSTRUMENTS



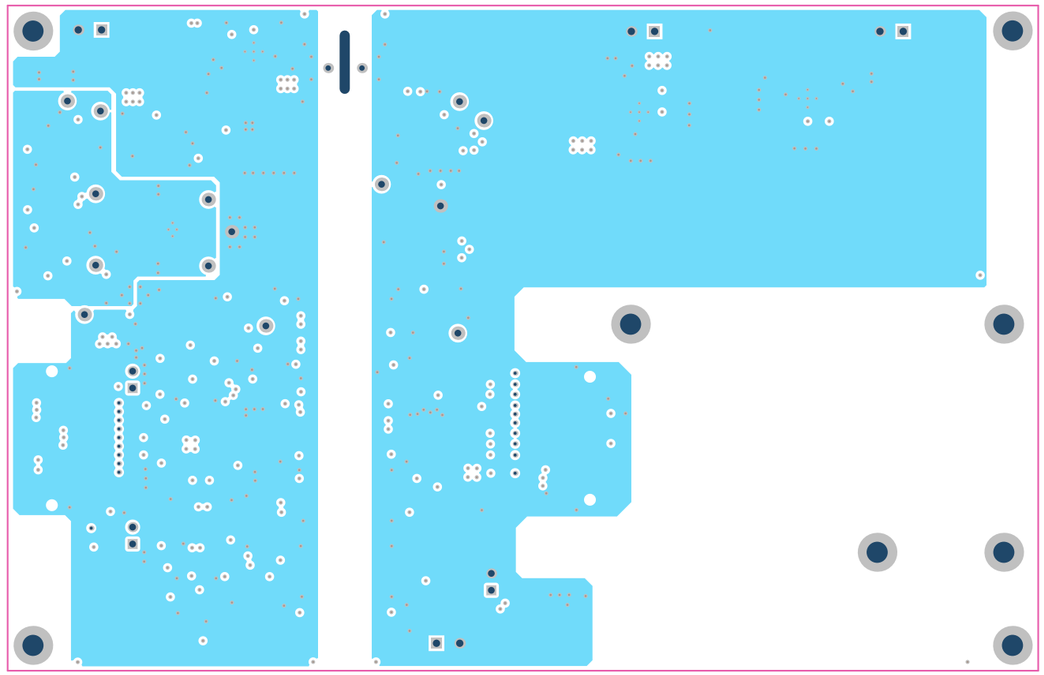
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01576_ADS8866EVM_ISO_Interface	SW REV: Not In VersionControl	
LAYER NAME = Top Solder	TID #: 01576		
PLOT NAME = Top Solder Mask	GENERATED : 4/6/2020 3:41:40 PM		TEXAS INSTRUMENTS



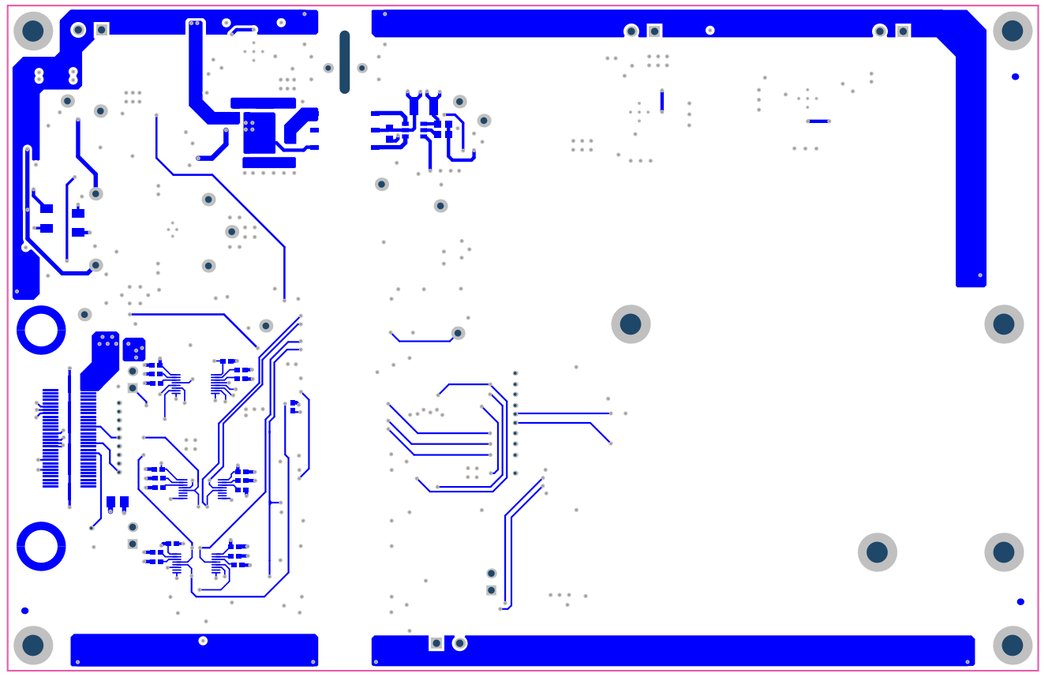
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01576_ADS8866SEVM_ISO_Interface	SVN REV: Not In VersionControl	
LAYER NAME = Top Layer	TID #: 01576		
PLOT NAME = Top Layer	GENERATED : 4/6/2020 3:41:41 PM		TEXAS INSTRUMENTS



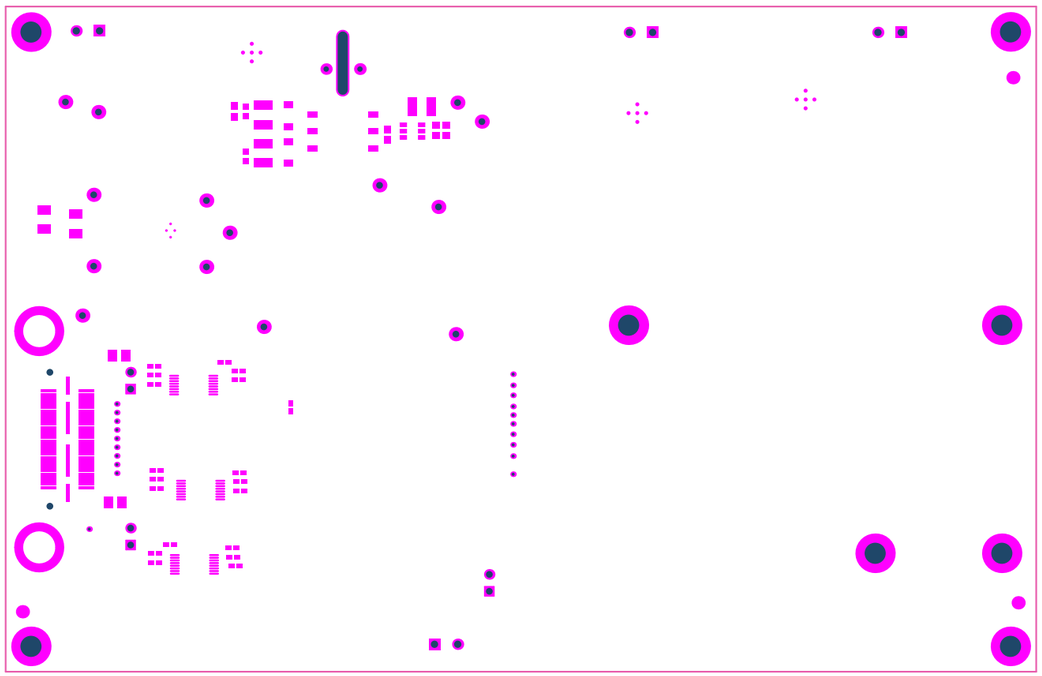
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01576_ADS8866EVM_ISO_Interface		REV: Not In VersionControl
LAYER NAME = VCC	TID #: 01576		
PLOT NAME = VCC Layer	GENERATED : 4/6/2020 3:41:43 PM		TEXAS INSTRUMENTS



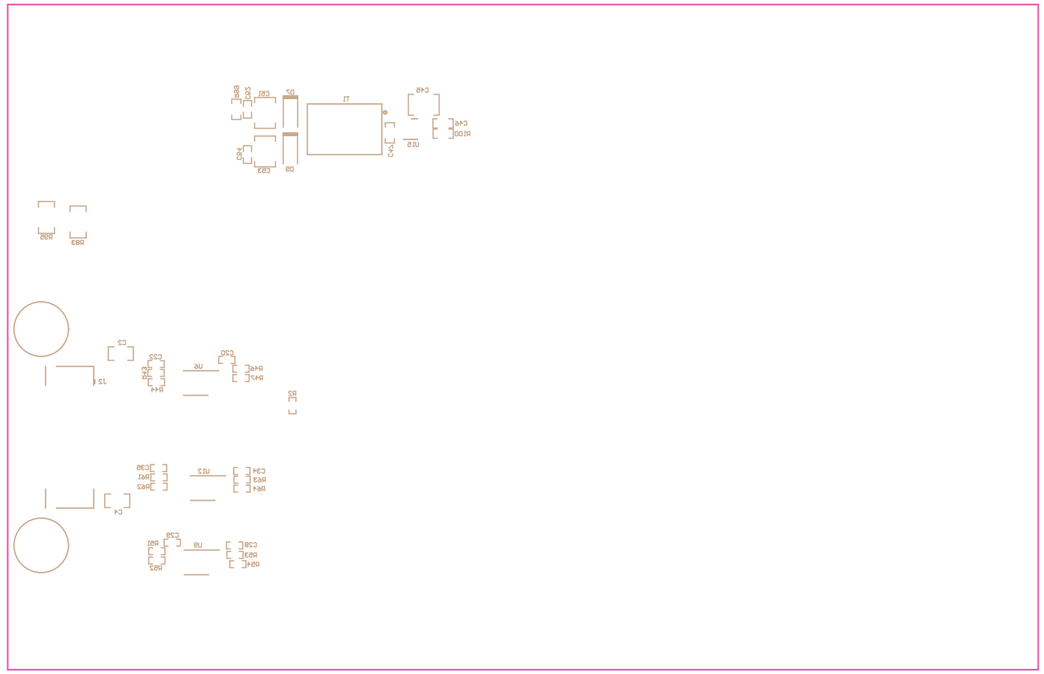
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01576_ADS8686S_ISO_Interface	SVN REV: Not In VersionControl	
LAYER NAME = GND	TID #: 01576		
PLOT NAME = GND Layer	GENERATED : 4/6/2020 3:41:45 PM		TEXAS INSTRUMENTS



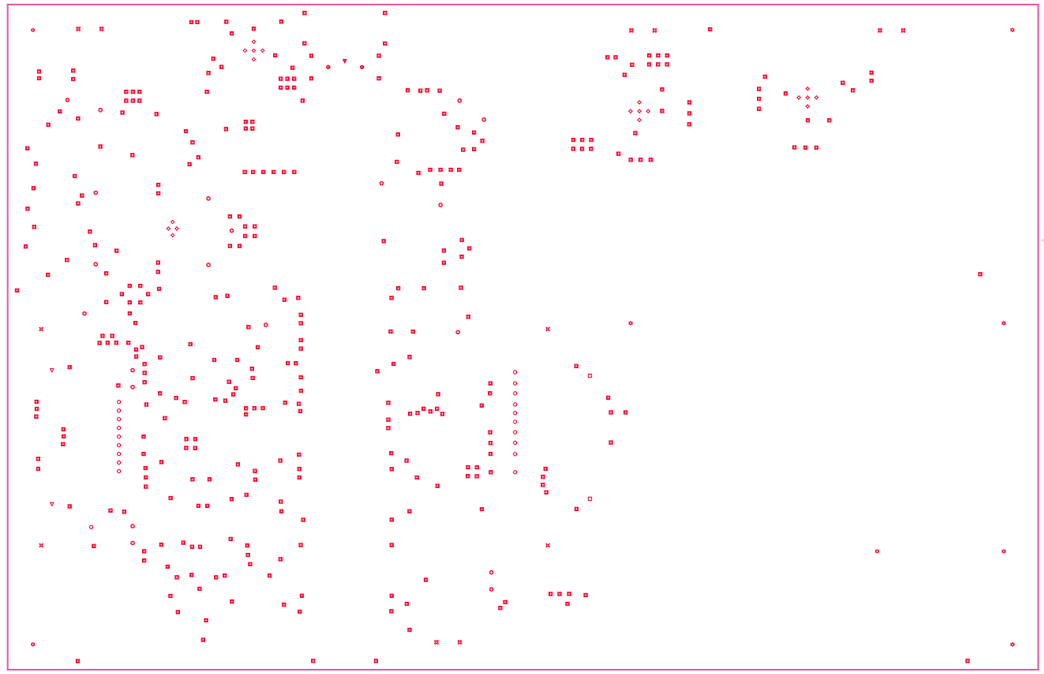
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01576_ADS8686S_ISO_Interface			$WCREV: Not In VersionControl
LAYER NAME = Bottom Layer	TID #: 01576			
PLOT NAME = Bottom Layer	GENERATED : 4/6/2020 3:41:47 PM			TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01576_ADS8686S_ISO_Interface	SW REV: Not In VersionControl	
LAYER NAME = Bottom Solder	TID #: 01576		
PLOT NAME = Bottom Solder Mask	GENERATED : 4/6/2020 3:41:48 PM		TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01576_ADS8686S_EISO_Interface	REV: Not In VersionControl	
LAYER NAME = Bottom Overlay	TID #: 01576		
PLOT NAME = Bottom Overlay	GENERATED : 4/6/2020 3:41:50 PM		TEXAS INSTRUMENTS



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4 High Tg	8.00mil	4.2	
5	VCC	Copper	1.40mil		
6	Dielectric2	FR-4 High Tg	40.00mil	4.8	
7	GND	Copper	1.40mil		
8	Dielectric3	FR-4 High Tg	8.00mil	4.8	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

FAB NOTES:

1. CORE THICKNESS BETWEEN LAYER VCC AND GND SHOULD BE 40 MIL(01 MM).

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
◇	19	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
◘	348	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer	
○	20	17.72mil (0.450mm)	PTH	Round	Top Layer - Bottom Layer	
◎	2	32.00mil (0.813mm)	PTH	Round	Top Layer - Bottom Layer	
□	2	40.00mil (1.016mm)	NPTH	Round	Top Layer - Bottom Layer	
✿	20	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
▽	2	40.16mil (1.020mm)	NPTH	Round	Top Layer - Bottom Layer	
⊠	8	43.31mil (1.100mm)	PTH	Round	Top Layer - Bottom Layer	
▼	1	60.00mil (1.524mm)	NPTH	Slot	Top Layer - Bottom Layer	
✡	8	125.00mil (3.175mm)	PTH	Round	Top Layer - Bottom Layer	
✖	4	173.23mil (4.400mm)	NPTH	Round	Top Layer - Bottom Layer	
	434 Total					

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Drill tolarence:
For 7.87 mil vias+0/-7.87mil
For 12 mil vias+0/-12mil
For PTH +/-3mil
For NPTH +/-2mil

ALL VIAS ARE TENTED EXCEPT THERMAL VIAS
THIS IS NOT AN IMPEDENCE CONTROLLED BOARD

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 5.8MIL EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 2 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 2 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: TIDA-01576_ADS8686S_ISO_Interface
DESIGNED FOR: Public Release
FILE NAME: TIDA-01576_ADS8686S_ISO_Interface.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01576_ADS8686S_ISO_Interface	REV: Not In VersionControl
LAYER NAME = Drill Drawing	TID #: 01576	
PLOT NAME = Drill Drawing	GENERATED : 4/6/2020 3:41:54 PM	TEXAS INSTRUMENTS

ENGINEER: SREENIVASA KALLIKUPPA	LAYOUT BY: Avinash
SCALE: 1.12	ALTIUM DESIGNER VERSION: 18.1.9.240

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01576_ADS8686S_ISO_Interface		REV: Not In VersionControl
LAYER NAME =	TID #: 01576		
PLOT NAME = Board Dimensions	GENERATED : 4/6/2020 3:41:57 PM		TEXAS INSTRUMENTS