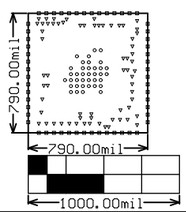
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		0.69mil		
	Dielectric 1	FR-4	3.70mil	4.1	
2	GND1		0.69mil		
	Dielectric 3	PP-006	2.80mil	4.1	
3	Signal Layer 1	CF-004	0.69mil		
	Dielectric1	FR-4	48.00mil	4.8	
4	Signal Layer 2	CF-004	0.69mil		
	Dielectric 4	PP-006	2.80mil	4.1	
5	PWR/GND2		0.69mil		
	Dielectric 2	FR-4	3.70mil	4.1	
6	Bottom Layer		0.69mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
○	37	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
▽	65	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer	
□	56	30.00mil (0.762mm)	PTH	Round	Top Layer - Bottom Layer	
	158 Total					



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 7.874 MIL
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER _____
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER_____
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER _____
☒ MATTE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____
ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: TMDSHSECDOCK NOR FLASH Board
DESIGNED FOR: Public Release
FILE NAME: PROC148_NORFLASH.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC148_NORFLASH REV: A	SVN REV: b1cc1e417ad80a14f3cd317cb353222d2d932ddc0 (Locally Modified)	
LAYER NAME = [illegible]	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 3/13/2023 4:04:55 PM	TEXAS INSTRUMENTS	

ENGINEER:	LAYOUT BY:
Brennan Hartigan	Brennan Hartigan
SCALE: 1.00	ALTIUM DESIGNER VERSION: 22.8.2.66