# TPS7A5201 PSPICE MODEL REPORT

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**Released by:** WEBENCH Design Center, Texas Instruments Inc.

**Simulator Name and Version:** PSPICE 16.2.0.s003

**Data sheet:**

**EVM User Guide:**

**Description of Model:**

**Document Revision History:**

| REVISION NO. | DESCRIPTION | REVISION DATE | REMARKS |
|---|---|---|---|
| 1 | Final Release | 30/10/17 | |

# Table of Contents

# 1. Start-up Response

## 1.1 Analysis Parameters

| PSPICE |
|---|
| .OPTIONS ABSTOL= 10n |
| .OPTIONS ITL1= 1500 |
| .OPTIONS ITL2= 400 |
| .OPTIONS ITL4= 400 |
| .OPTIONS VNTOL= 10u |
| .OPTIONS RELTOL= 1m |
| .OPTIONS CHGTOL= 0.01p |
| .OPTIONS GMIN= 1p |
| .OPTIONS TNOM= 27DEG |

Maximum Step size 20ns.

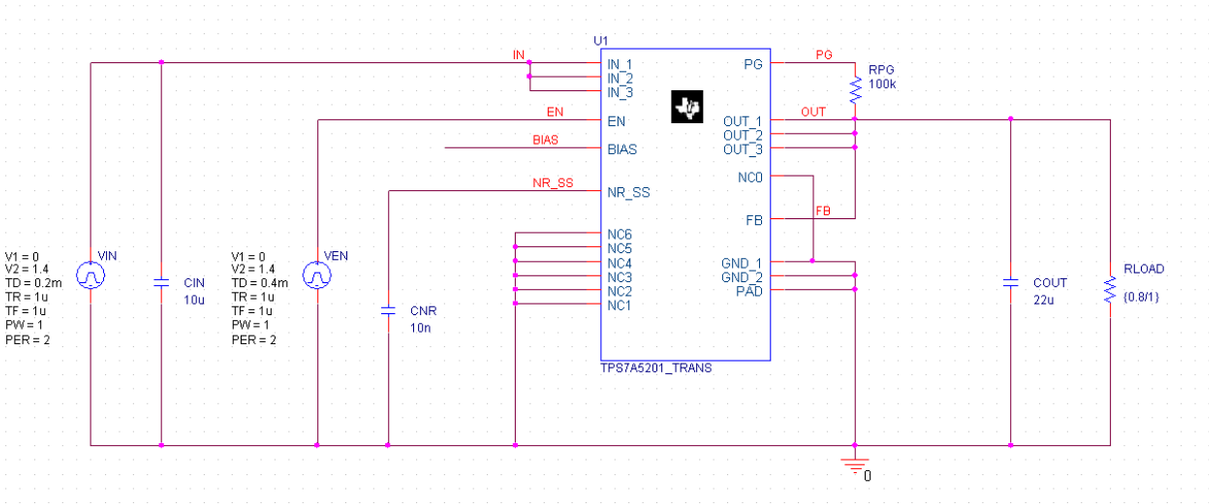
**Note:** All test cases are configured for above analysis parameters.

## 1.2 Machine specification

All the runs have been carried out on Intel(R) Core(TM) i5 CPU M430 @2.3GHz with 8GB RAM.

## 1.3 Schematic

## PSPICE Schematic:




## Description:

1. This test case is configured for VIN1=VEN=1.4V, VOUT= 0.8V, VBIAS=open, CIN=10uF, COUT=22uF , and ILOAD=1A.
2. This test case used to observe the start-up behavior of the model for CNR values of 0nF, 10nF, 47nF and 100nF.
3. Transient Analysis is done for 30m and takes ~2min simulation time.

## 1.4 Results

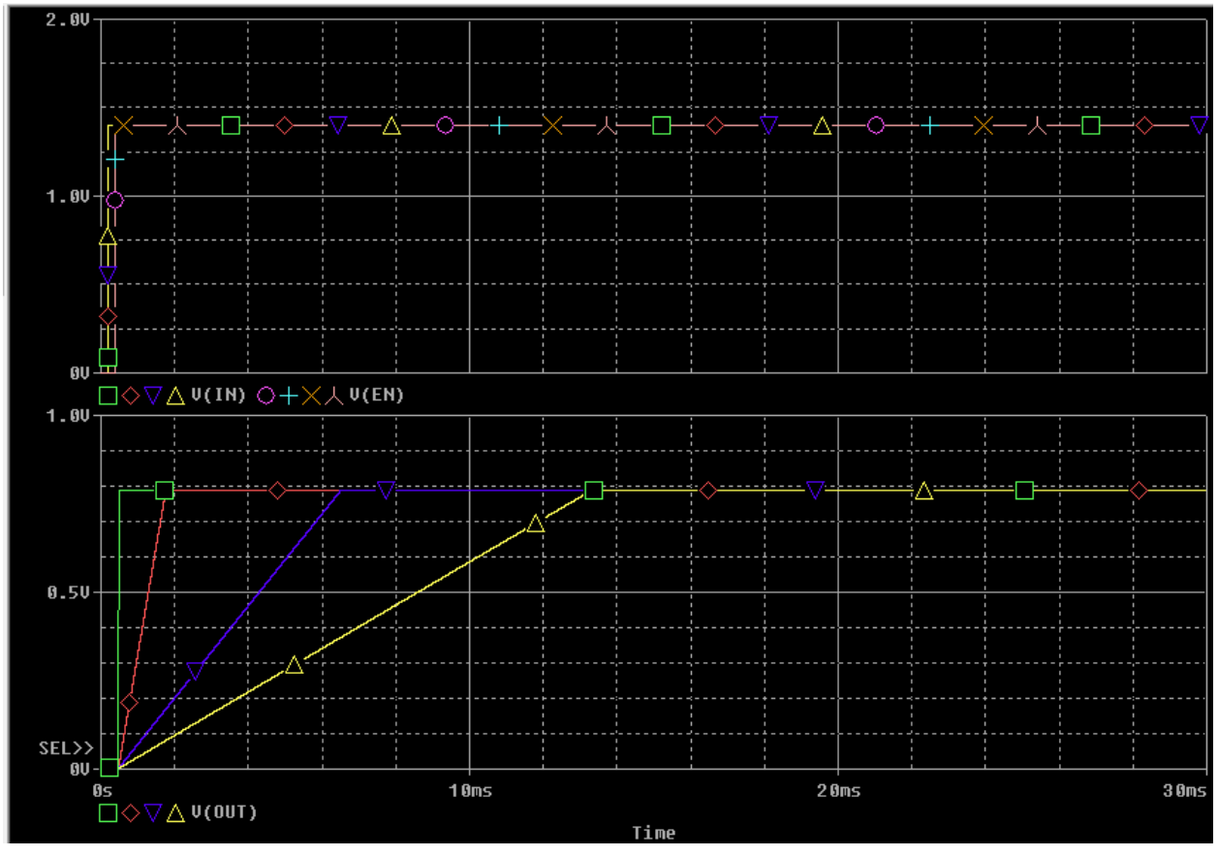



**Fig 1.4.1 Start-up response for CNR/SS=0nF, 10nF, 47nF and 100nF**

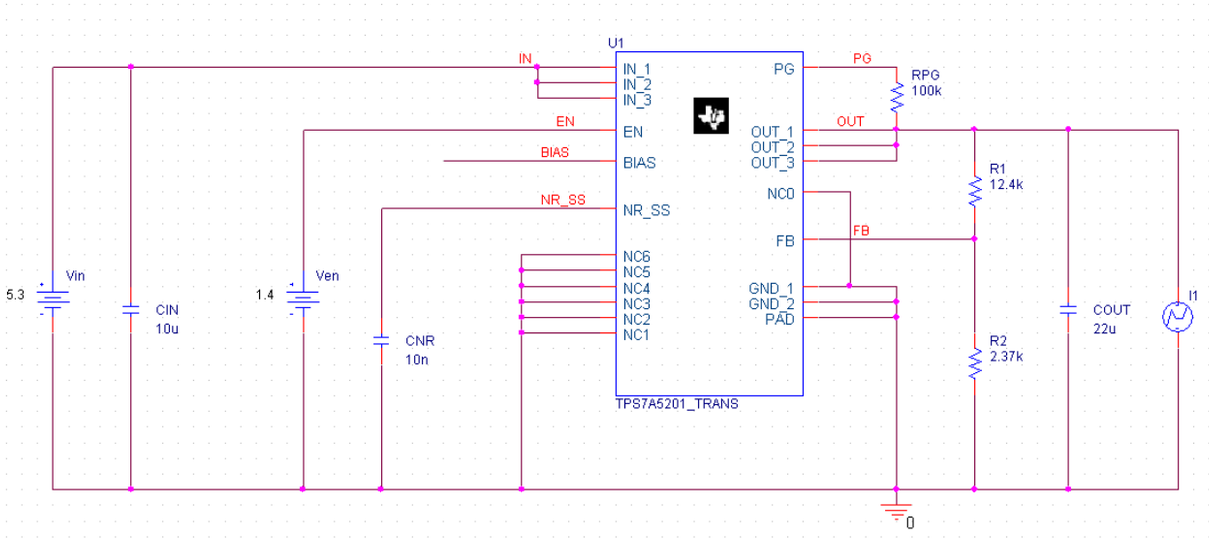
## 1.5 Tabulation of Results

| PARAMETER | | TEST CONDITIONS | DATASHEET | PSPICE | UNIT |
|---|---|---|---|---|---|
| VOUT | Output voltage | VIN=1.4V, EN=1.4V, CNR/SS1= 0nF,10nF,47nF and 100nF | NA | 0.786 | mV |
| tSTR **(for CNR/SS=0nF)** | Startup time | Time from EN to Vout | NA | 0.3 | ms |
| tSTR **(for CNR/SS=10nF)** | Startup time | Time from EN to Vout | NA | 1.5 | ms |
| tSTR **(for CNR/SS=47nF)** | Startup time | Time from EN to Vout | NA | 6.2 | ms |
| tSTR **(for CNR/SS=100nF)** | Startup time | Time from EN to Vout | NA | 13.2 | ms |

# 2. Load Transient Response

## 2.1 Schematic

### PSPICE Schematic




## Description:

1. This test case is configured for VIN=5.3V, VEN=1.4V, VOUT=5V, COUT=22uF, CIN=10uF, and Step load 100mA to 2A.
2. This test case is used to observe the load transient behavior of the model.

## 2.2 Results

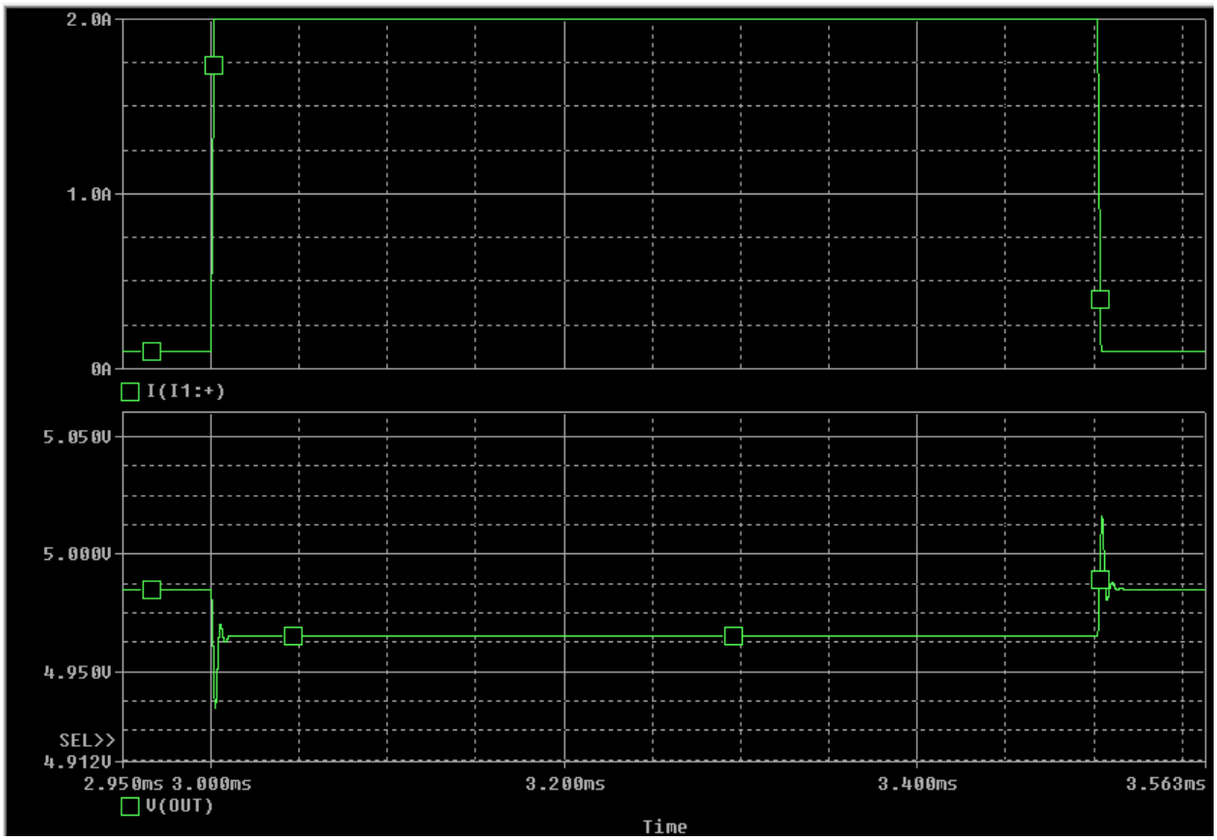



**Fig 2.2.1 Load transient response**

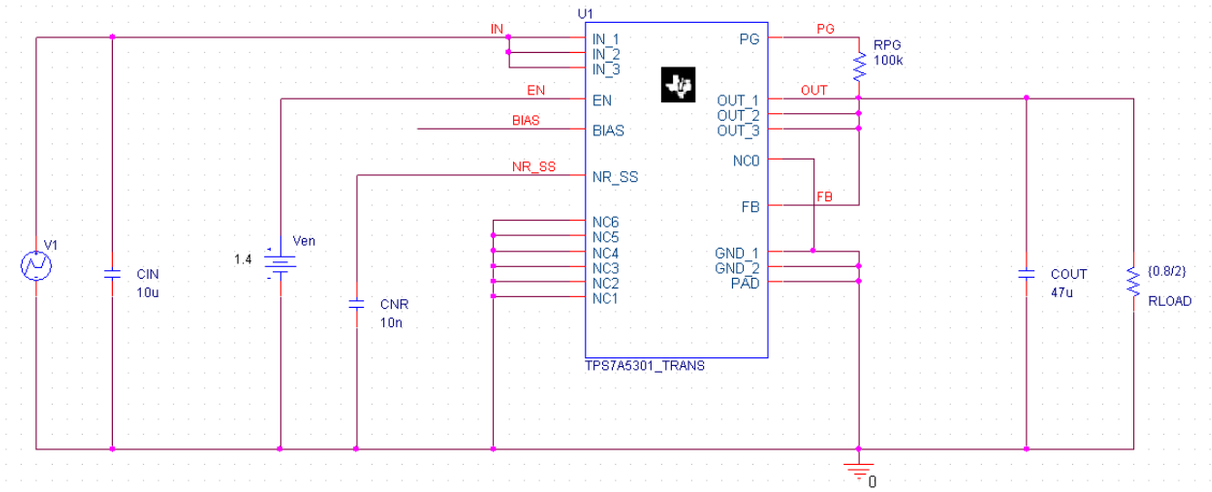
## 2.3 Tabulation of Results

| PARAMETER | Datasheet | PSPICE | UNIT |
|---|---|---|---|
| Undershoot | NA | 35.6 | mV |
| $T_{SETTLE(UNDER)}$ | NA | 16.08 | us |
| Overshoot | NA | 34.5 | mV |
| $T_{SETTLE(OVER)}$ | NA | 23.7 | us |

# 3. Line Transient Response

## 3.1 Schematic

### PSPICE Schematic




**Description:**

1. This test case is configured for step input VIN =1.4V-6.5V-1.4V, VEN=1.4, VOUT=0.8V, COUT=22uF, CIN=10uF, CNR/SS=10nF, and load 2A.
2. This test case is used to observe the line transient behavior of the model.

## 3.2 Results

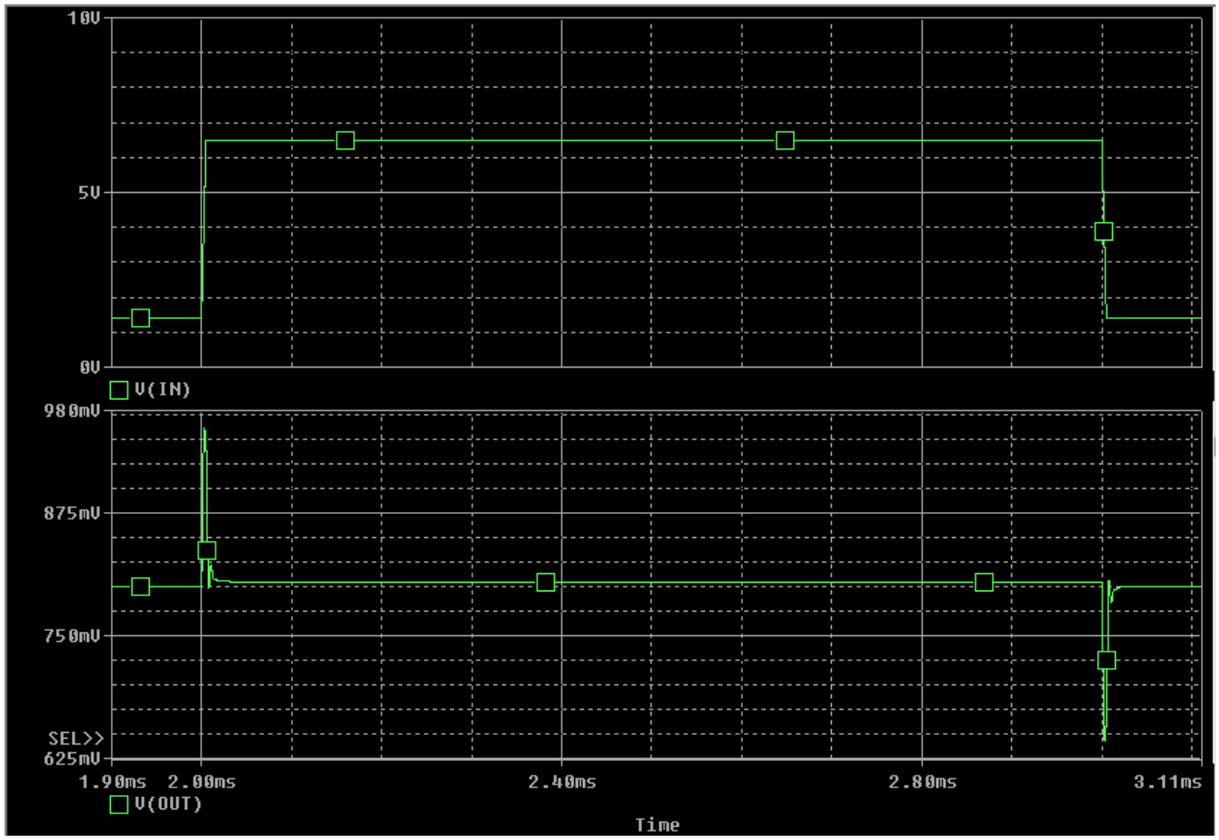



**Fig 3.2.2 Line transient response**

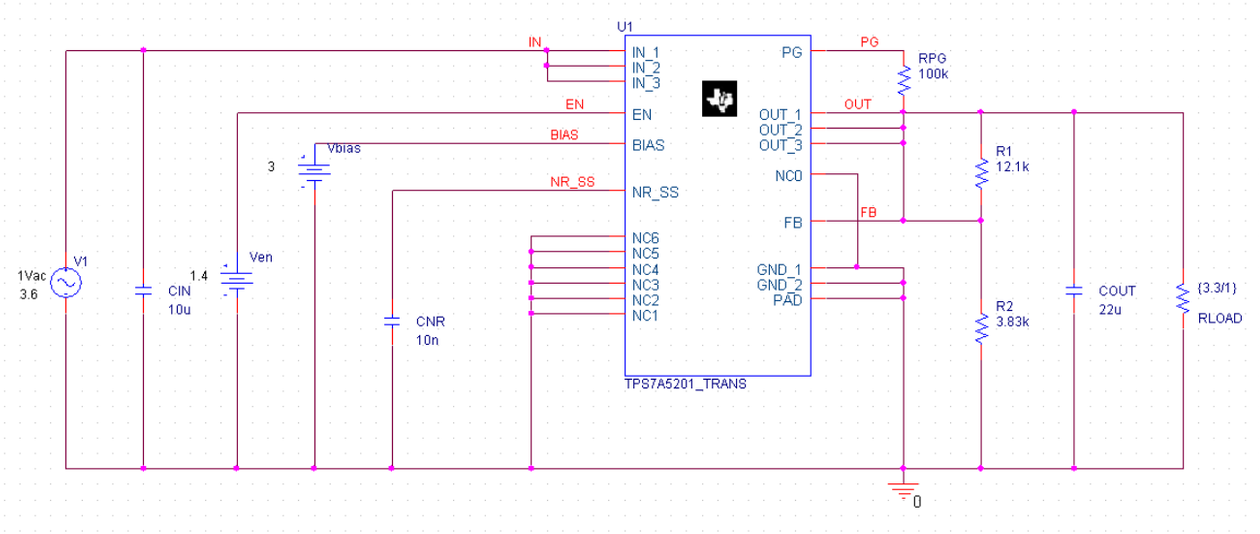
## 3.3 Tabulation of Results

| PARAMETER | Datasheet (Peak to peak) | PSPICE | UNIT |
|---|---|---|---|
| Undershoot | NA | 152 | mV |
| $T_{SETTLE(UNDER)}$ | NA | 38 | us |
| Overshoot | NA | 152 | mV |
| $T_{SETTLE(OVER)}$ | NA | 39 | us |

# 4. PSRR Response

## 4.1 Schematic

### PSPICE Schematic




## Description:

1. This test case is used to observe the Ripple Rejection vs Frequency behavior of the model.
2. This test case is configured for input Vin(dc)=3.6V, Vin(ac)=1V, VOUT=3.3V, COUT=22uF, CIN=10uF, CNR/SS=10nF, VBIAS=5V, CFF=10nF and 3A load and 40dB @500kHz

## 4.2 Results

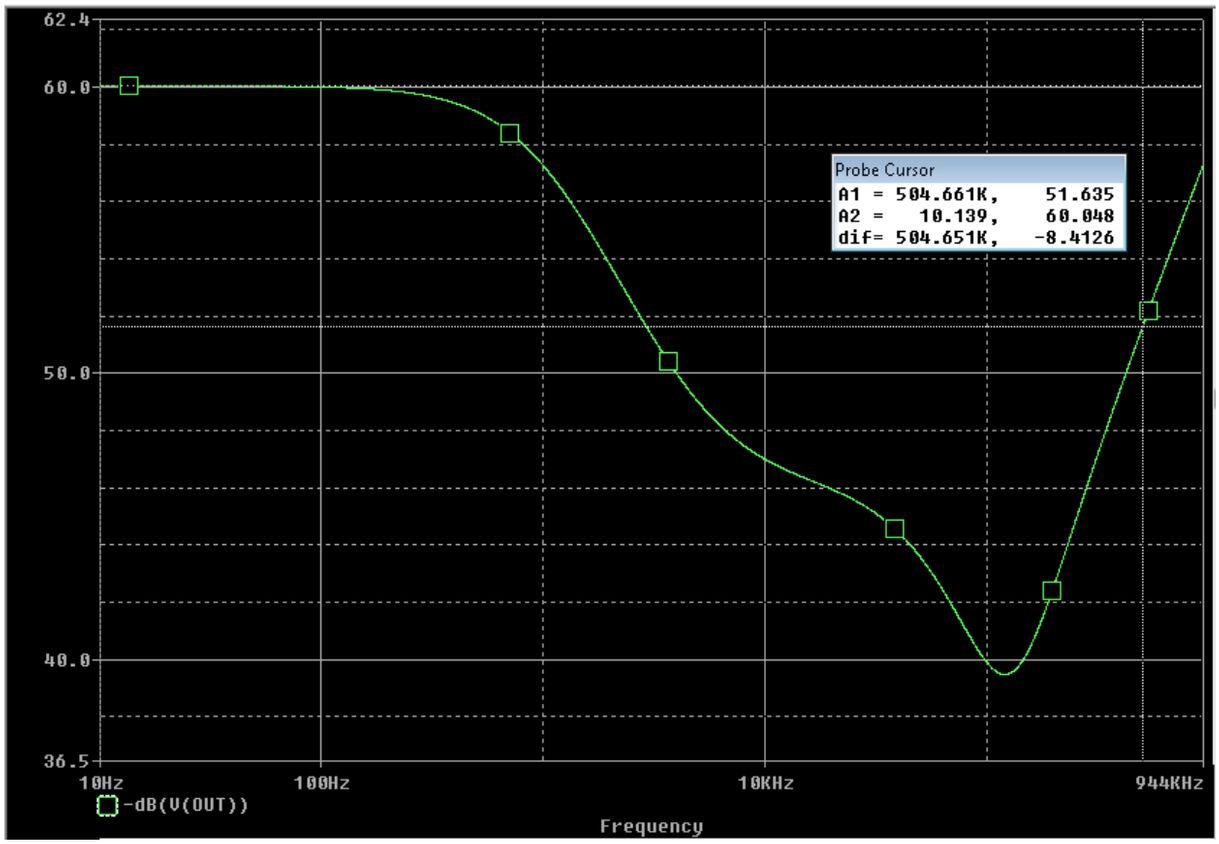
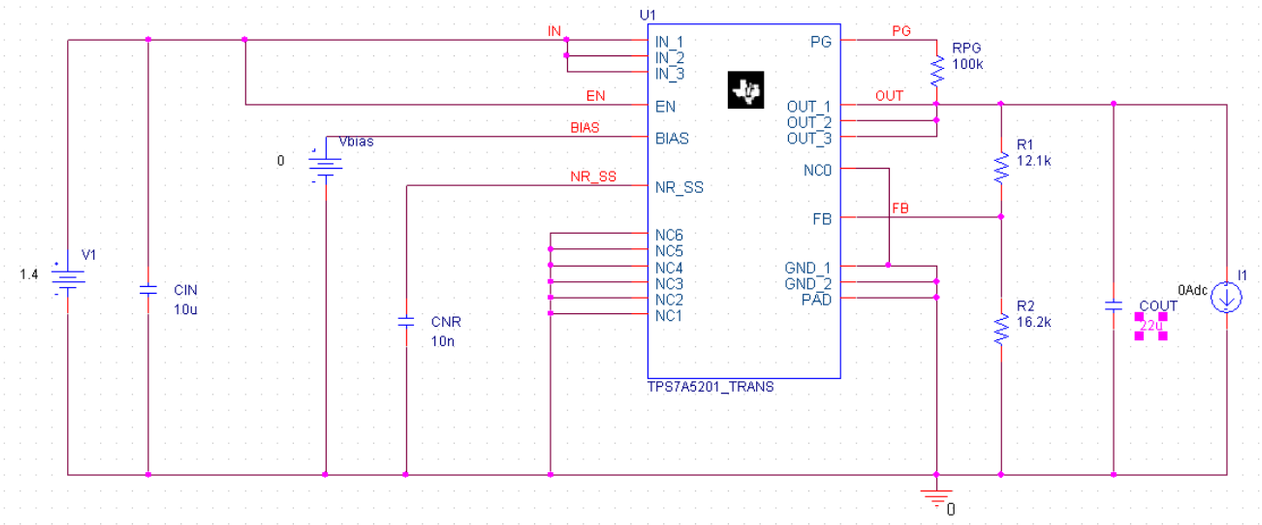



**Fig 4.2.1 Ripple Rejection vs Frequency response**

# 5. Dropout Voltage vs Iout Response

## 5.1 Schematic

### PSPICE Schematic




### Description:

1. This test case is configured for step input VIN=EN=VOUT=1.4V, CNR/SS=10nF, COUT=22uF, CIN=10uF and Load is varied from 0 to 2A.
2. This test case is used to observe the Dropout voltage vs Iout response of the model.

## 5.2 Results

***CASE1: 1.4<=VIN<=2.2 and Vbias=0***

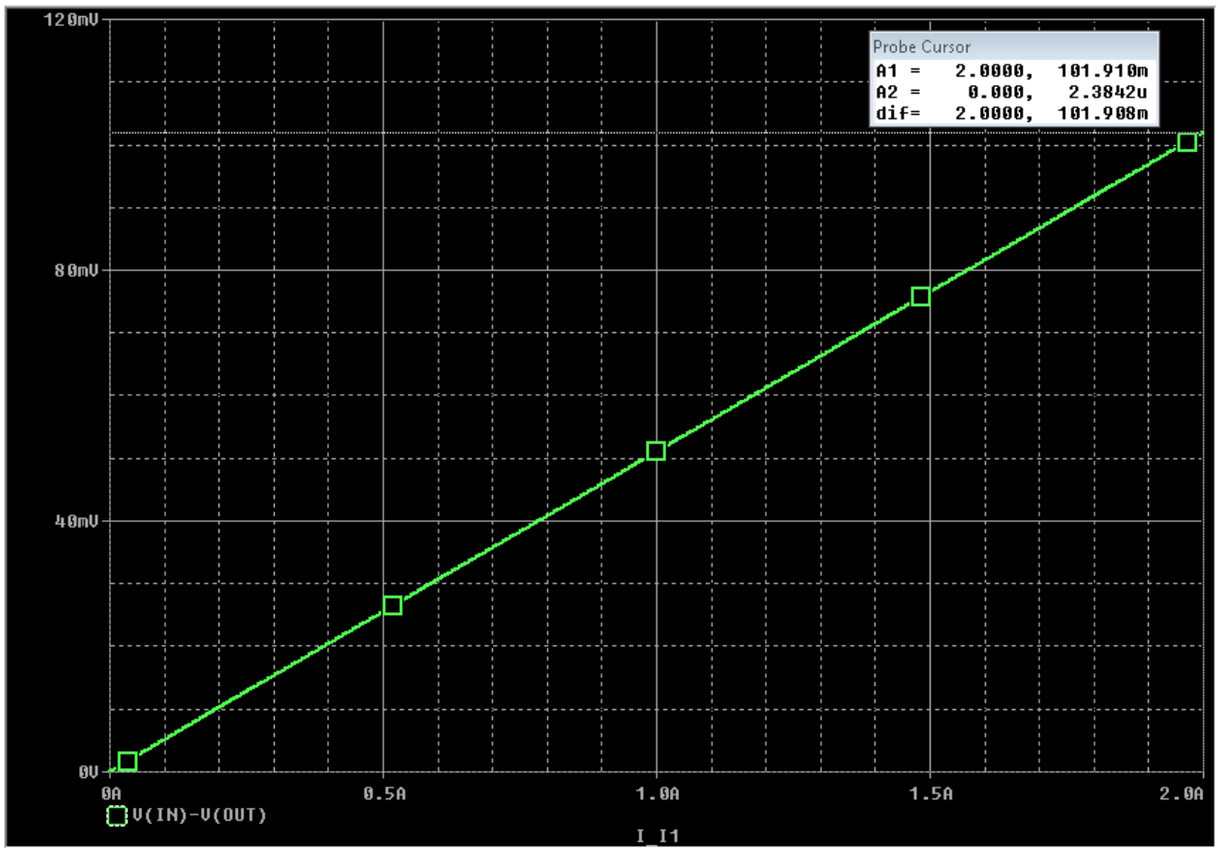



**Fig 5.2.1 Dropout voltage vs ILOAD response**

***CASE2: 1.1<=VIN<=5 and 3<=Vbias<=6.5***

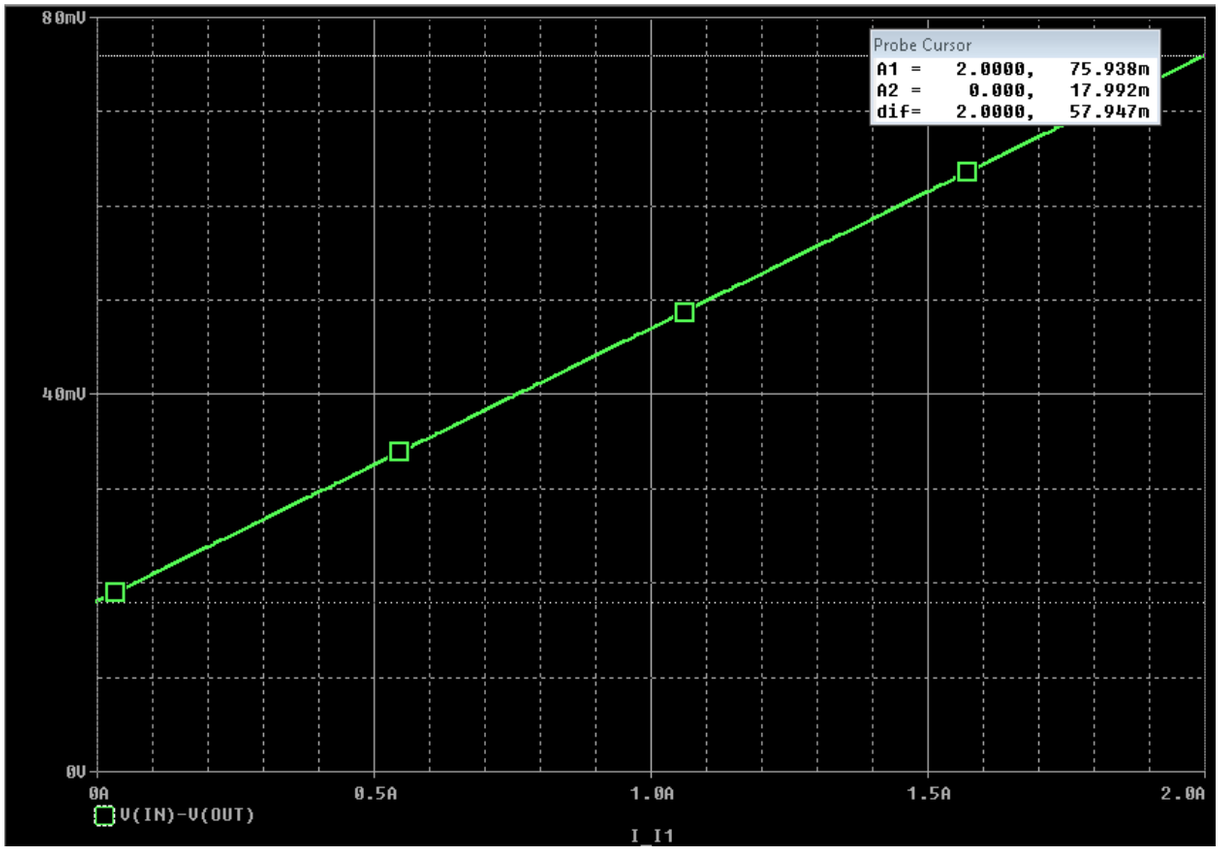



**Fig 5.2.2 Dropout voltage vs ILOAD response**

***CASE3: 5<=VIN<=6.5 and Vbias=0***

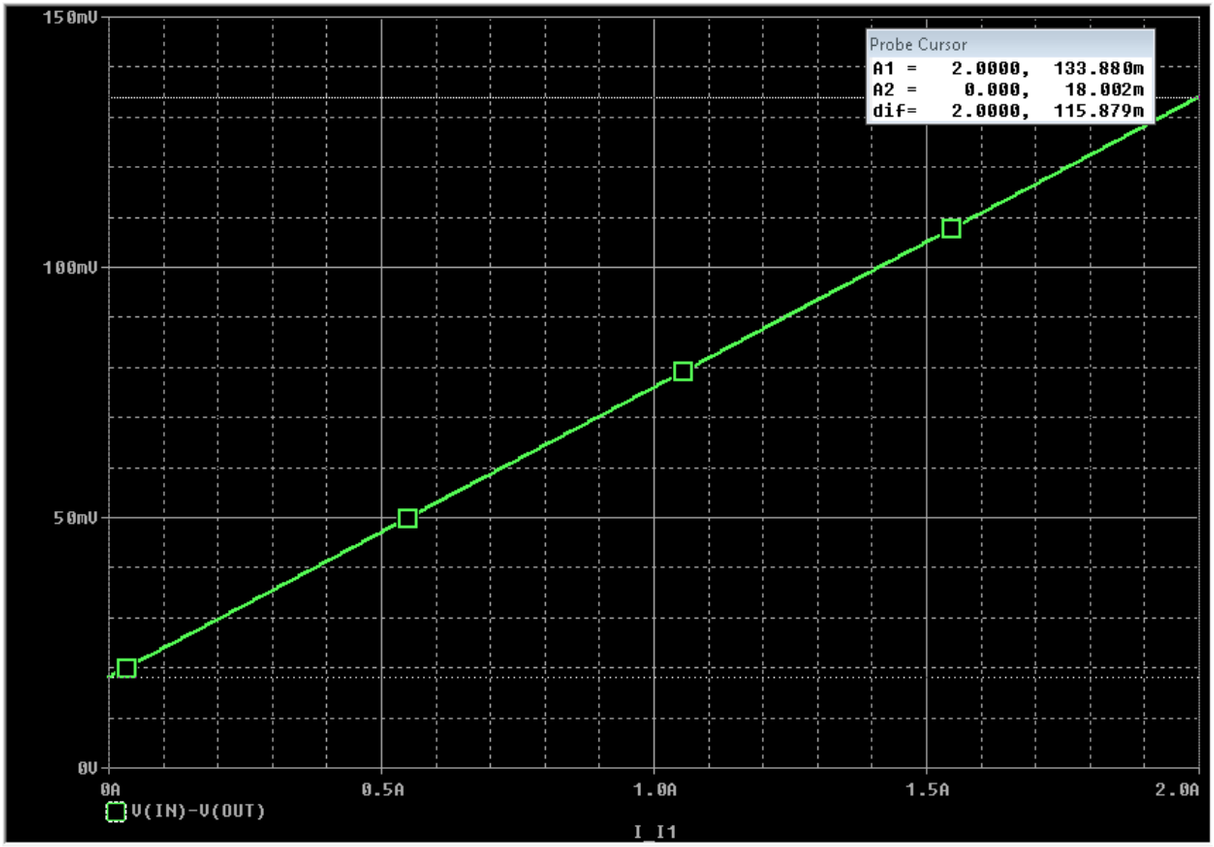
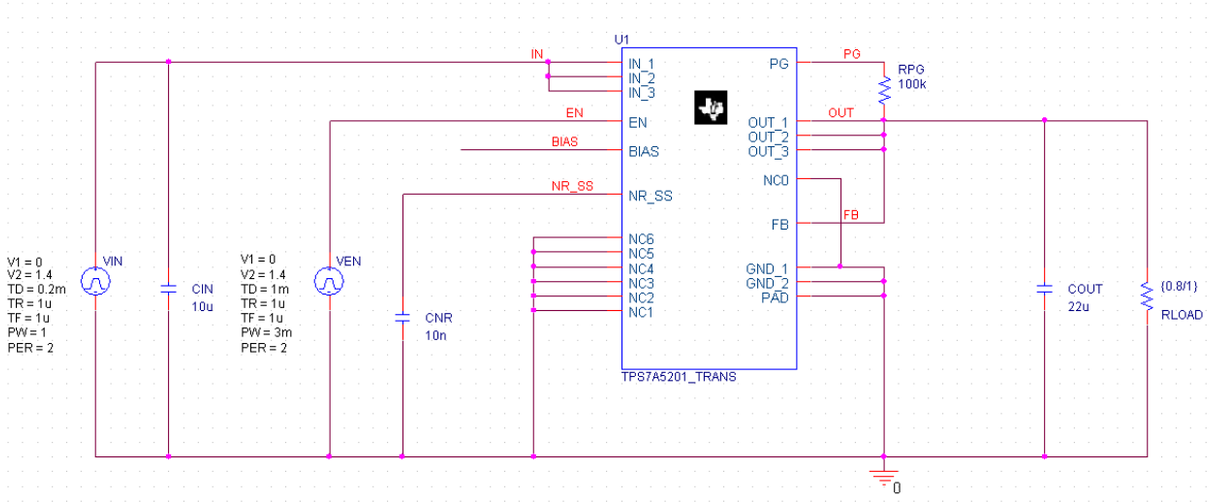



**Fig 5.2.3 Dropout voltage vs ILOAD response**

# 6. Enable Shutdown Response

## 6.1 Schematic

## PSPICE Schematic




## Description:

1. This test case is configured for step input VEN=1.4V, VOUT=0.8V, VBIAS=Open, CNR/SS=10nF, COUT=22uF, CIN=10uF and Load is 1A.
2. This test case is used to observe the Enable shutdown response of the model.

## 6.2 Results

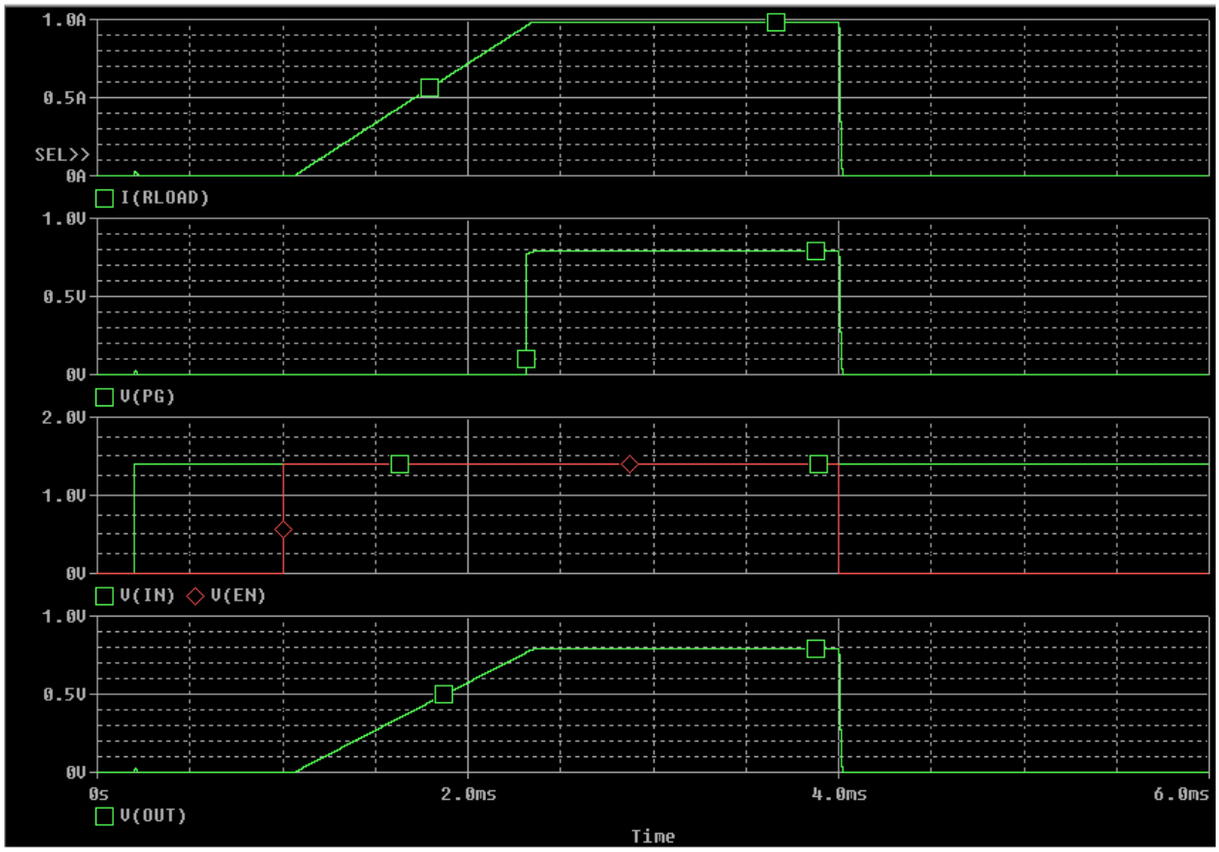
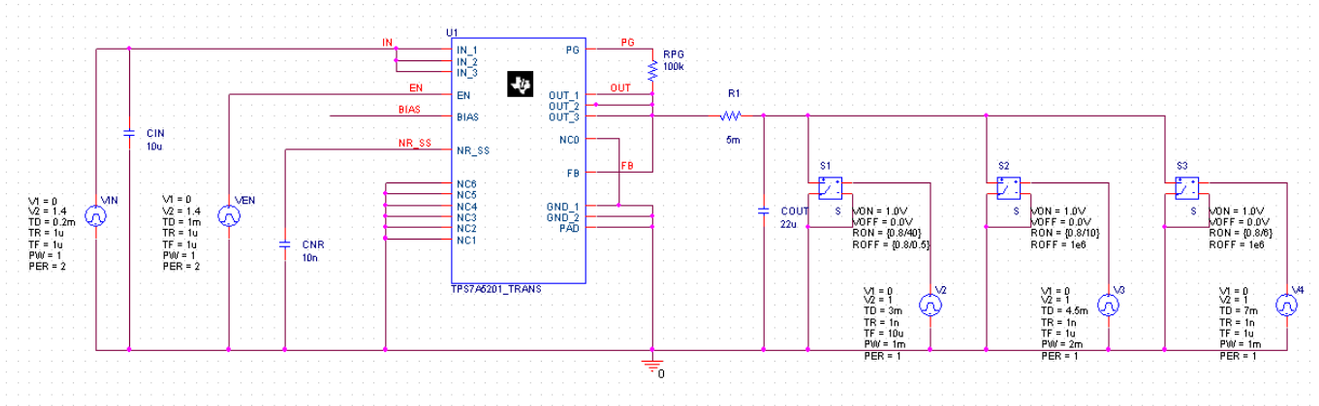



**Fig 6.2.1 Enable Shutdown response**

# 7. Output Circuit Limit

## 7.1 Schematic

## PSPICE Schematic




## Description:

1. This test case is configured for step input VIN=EN=1.4V, VOUT=0.8V, VBIAS=Open, CNR/SS=0nF, COUT=22uF, CIN=10uF and when S1 is ON RLOAD=20mOhm(ILOAD=40A) On, When S2 is ON then RLOAD= 0.08Ohm(ILOAD=10A) and when S3 is ON then RLOAD=0.13(ILOAD=6A).
2. This test case is used to observe the Output current limit response of the model.

## 7.2 Results

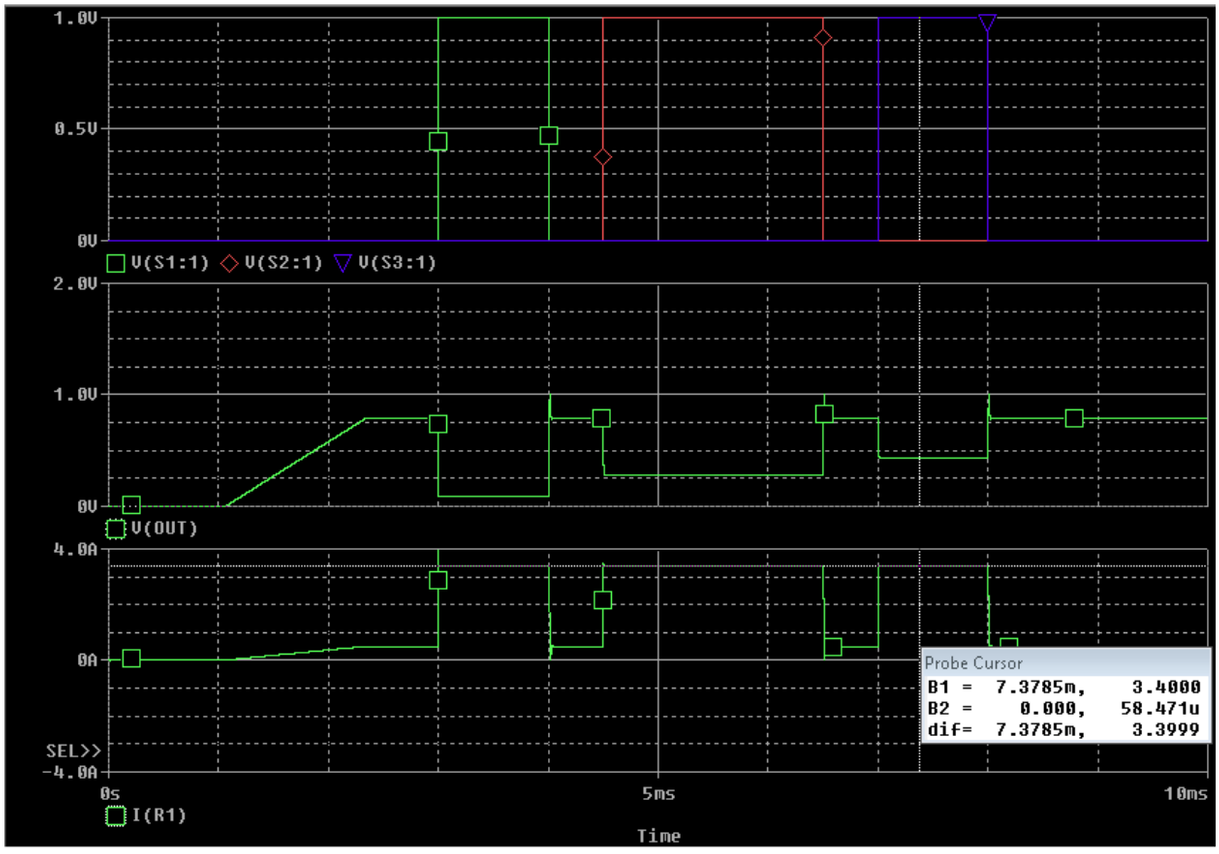



**Fig 6.2.1 Current limit Response**