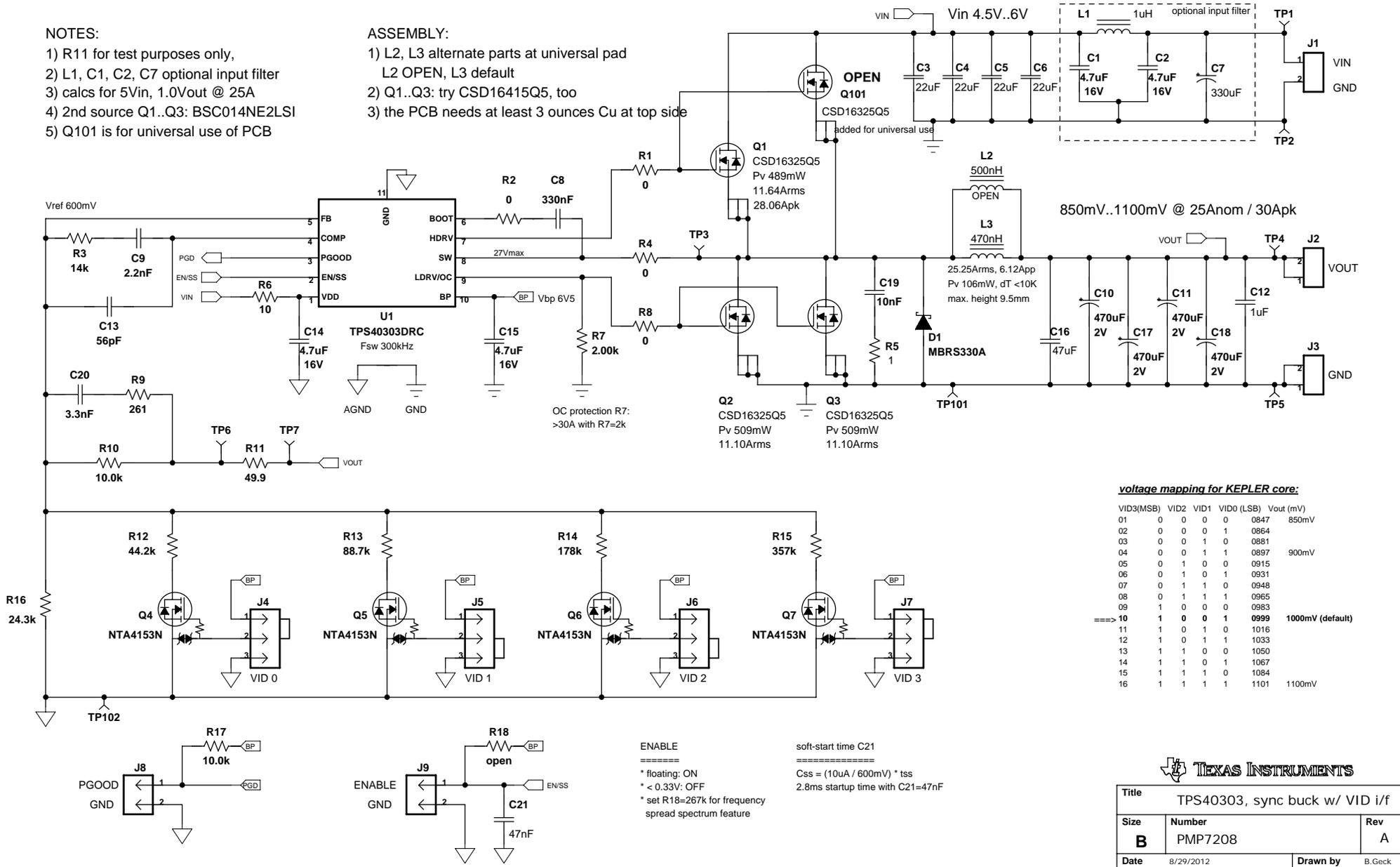


NOTES:

- 1) R11 for test purposes only,
- 2) L1, C1, C2, C7 optional input filter
- 3) calcs for 5Vin, 1.0Vout @ 25A
- 4) 2nd source Q1..Q3: BSC014NE2LSI
- 5) Q101 is for universal use of PCB

ASSEMBLY:

- 1) L2, L3 alternate parts at universal pad
L2 OPEN, L3 default
- 2) Q1..Q3: try CSD16415Q5, too
- 3) the PCB needs at least 3 ounces Cu at top side



850mV..1100mV @ 25Anom / 30Apk

voltage mapping for KEPLER core:

VID3(MSB)	VID2	VID1	VID0 (LSB)	Vout (mV)
01	0	0	0	0847
02	0	0	0	0864
03	0	0	1	0881
04	0	0	1	0897
05	0	1	0	0915
06	0	1	0	0931
07	0	1	1	0948
08	0	1	1	0965
09	1	0	0	0983
10	1	0	0	0999
11	1	0	1	1016
12	1	0	1	1033
13	1	1	0	1050
14	1	1	0	1067
15	1	1	1	1084
16	1	1	1	1101

ENABLE
 =====
 * floating: ON
 * < 0.33V: OFF
 * set R18=267k for frequency spread spectrum feature

soft-start time C21
 =====
 C_{ss} = (10uA / 600mV) * t_{ss}
 2.8ms startup time with C21=47nF



Title			TPS40303, sync buck w/ VID i/f		
Size	Number	Rev			
B	PMP7208	A			
Date	8/29/2012	Drawn by	B.Geck		
Filename	PMP7208RevA_pads.sch	Sheet	1	of	1

Engineer B.Geck

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