

Technical Article

Isolating a SEPIC



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If someone asked you what topology to use for an isolated, low-power output, chances are your first thought would be a flyback. Although a flyback is an excellent topology with benefits such as low cost, low component count and ease of adding additional outputs, it still has several drawbacks. The field-effect transistor (FET) and rectifier ringing associated with flyback transformer leakage inductance create electromagnetic interference (EMI), raise component stresses and lower efficiency. Additionally, obtaining well-regulated voltages can be a challenge when there are multiple outputs, especially with wide load variations. Let's see how isolating a single-ended primary-inductor converter (SEPIC) can provide an alternate approach and alleviate some of these issues.

The SEPIC is a nonisolated topology. However, as with a flyback, you can easily add additional transformer windings to create isolated outputs. The simplified schematic of Figure 1 shows a standard SEPIC converter generating a single nonisolated output on the left, with two additional isolated outputs on the right. The first isolated winding supplies a nominal 6V output as an input to a 5V linear regulator. The second isolated winding is stacked on top of the first to create a nonregulated 12V output.

You want tight coupling between the transformer winding of V_{OUT1} and the isolated windings (V_{OUT2} , V_{OUT3}), since energy in these windings simultaneously transfers to all three outputs. Leakage inductance between these windings only serves to degrade their voltage regulation. However, tight coupling is **not** required between the SEPIC's primary winding and the V_{OUT1} winding. Minimal FET ringing exists because capacitor C_{AC} provides a low impedance path for leakage energy into V_{OUT1} when the boost FET turns off. Since the SEPIC's primary winding voltage waveform has considerably less ringing than a flyback, this leads to improved output voltage regulation, especially under extreme crossload conditions where spike peak-detection often occurs.

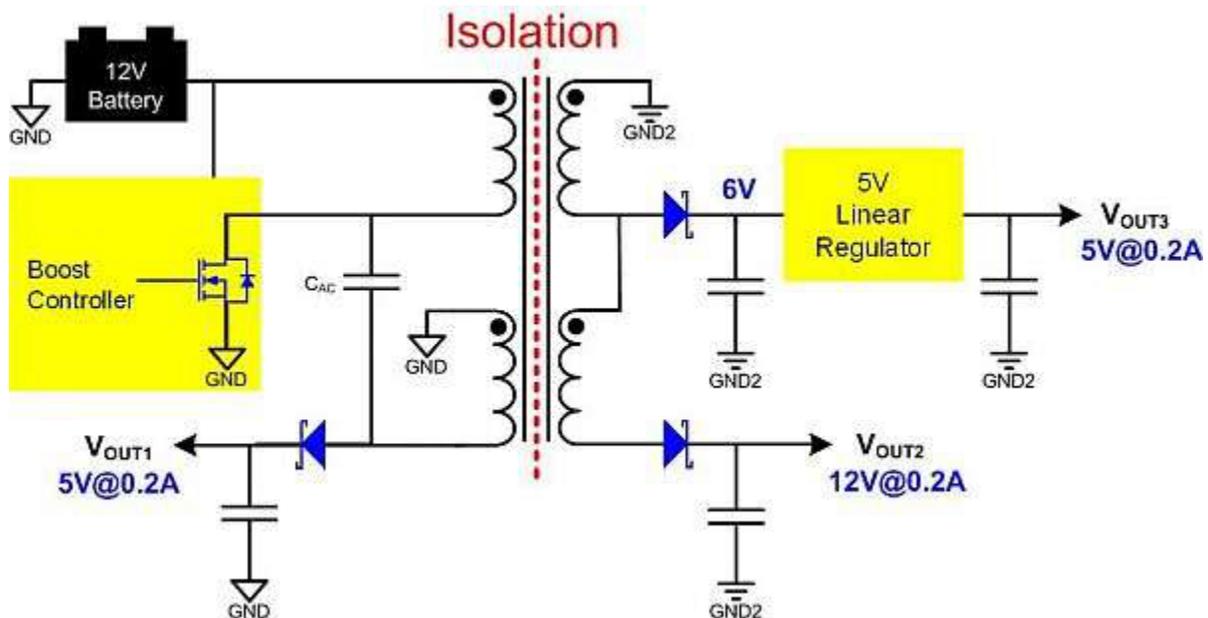


Figure 1. A SEPIC converter with additional windings provides isolated outputs.

As in all SEPICs, the turns ratio between the primary and V_{OUT1} must be 1-to-1. All other outputs are not bound to this turns ratio, however, and you can adjust them to provide any required output voltage, which you can easily calculate with [Equation 1](#):

$$\frac{N_x}{N_1} = \frac{V_{OUTx} + V_{diode\ x}}{V_{OUT1} + V_{diode\ 1}} \quad (1)$$

[Figure 2](#) shows the difference in FET voltage ringing between a SEPIC and a flyback. You can obtain the flyback FET voltage waveform from the SEPIC circuit simply by removing C_{AC} , which converts it into a flyback. The elimination of ringing on the FET significantly reduces the uncoupled energy conducted into the isolated outputs, improving regulation.



Figure 2. The voltage on a SEPIC FET rings less than a flyback, lowering stress and improving output voltage regulation.

[Figure 3](#) shows the test circuit schematic used to obtain the regulation data in [Figure 4](#), while [Figure 5](#) shows a photo of the actual hardware. This design uses primary-side feedback for a regulated voltage on V_{OUT1} . The isolated outputs rely on a combination of tight transformer coupling and small pre-loads to obtain reasonable voltage regulation. Since the linear regulator holds the isolated 5V output constant, its minimum and maximum inputs are of primary concern. If the input to the linear regulator is too low, the output voltage can drop out. Conversely, if the input to the linear regulator is too high, excess power will dissipate.

Regulation data for the isolated outputs show that their worst-case minimum and maximum voltages occur during extreme crossload conditions. You can see minimum voltages on the isolated windings while they are at maximum loads with V_{OUT1} unloaded. Maximum voltages on the isolated windings occur at no load with V_{OUT1} at maximum load. Based on the test data, I measured a variation in regulation of less than $\pm 4\%$. Although these results are not indicative of all designs, they suggest that similar designs can reasonably achieve $\pm 5\%$ voltage regulation, while flybacks are more likely to be at least several percent higher.

It's possible to greatly improve the cross-regulation of flybacks by implementing synchronous rectifiers, as Brian King described in [Power Tips #78](#). However, this improvement requires the use of higher-cost FETs and additional drive circuitry. You can apply this same technique to isolated SEPIC converters, but the rectifier for the nonisolated output would also need to be synchronous. I described how to easily implement a synchronous SEPIC in a previous [TI blog post](#).

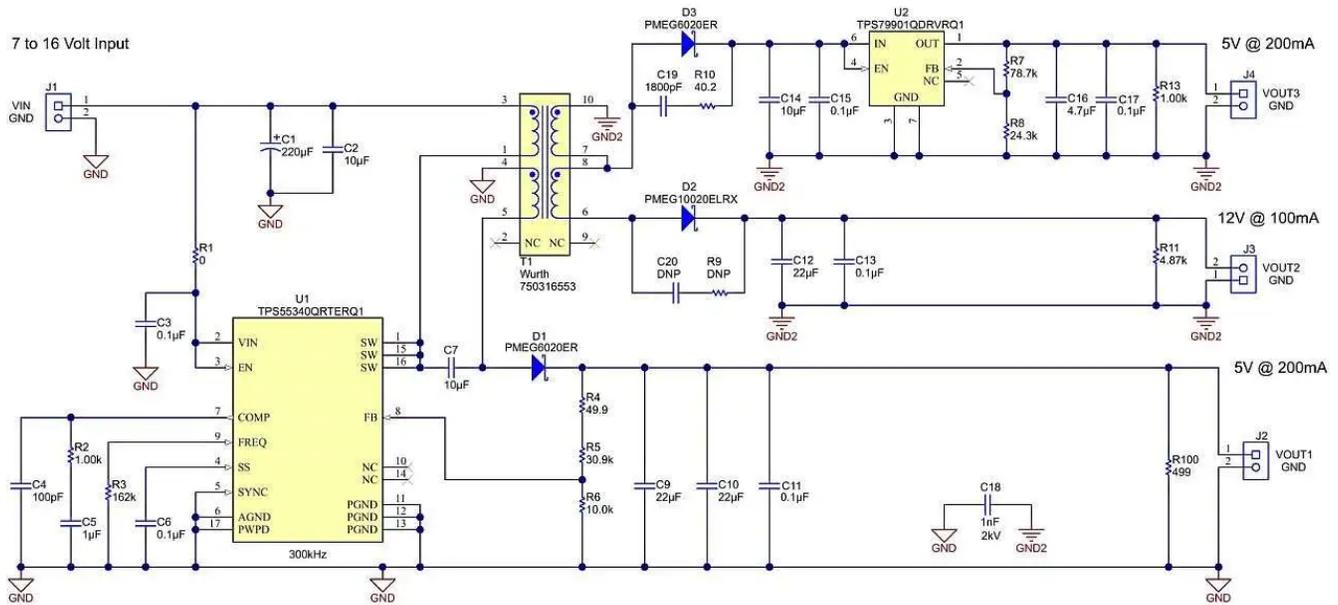


Figure 3. Actual SEPIC design with dual isolated outputs.

Voltage Regulation Data								
VIN (V)	VOUT 5V #1 (V)	IOUT 5V #1 (mA)	LDO In (V)	LDO out (V)	IOUT LDO (mA)	VOUT 12V (V)	IOUT 12V (mA)	
No Load Conditions								
7	5.04	0	6.07	5.06	0	11.88	0	
12	5.04	0	6.08	5.06	0	11.88	0	
16	5.04	0	6.08	5.06	0	11.89	0	
Full Load Conditions								
7	5.04	200	5.96	5.06	200	11.78	100	
12	5.04	200	6.02	5.06	200	11.85	100	
16	5.04	200	6.03	5.06	200	11.86	100	
Cross Loading								
7	5.04	0	5.77	5.06	200	11.39	100	
7	5.04	200	6.23	5.06	0	12.14	0	
12	5.04	0	5.82	5.06	200	11.46	100	
12	5.04	200	6.24	5.06	0	12.13	0	
16	5.04	0	5.86	5.06	200	11.54	100	
16	5.04	200	6.24	5.06	0	12.12	0	
			6.005	High/Low Avg (V)			11.765	High/Low Avg (V)
			-3.91	Percent Low (%)			-3.19	Percent Low (%)
			3.91	Percent High (%)			3.19	Percent High (%)

Figure 4. Measured voltage regulation data.

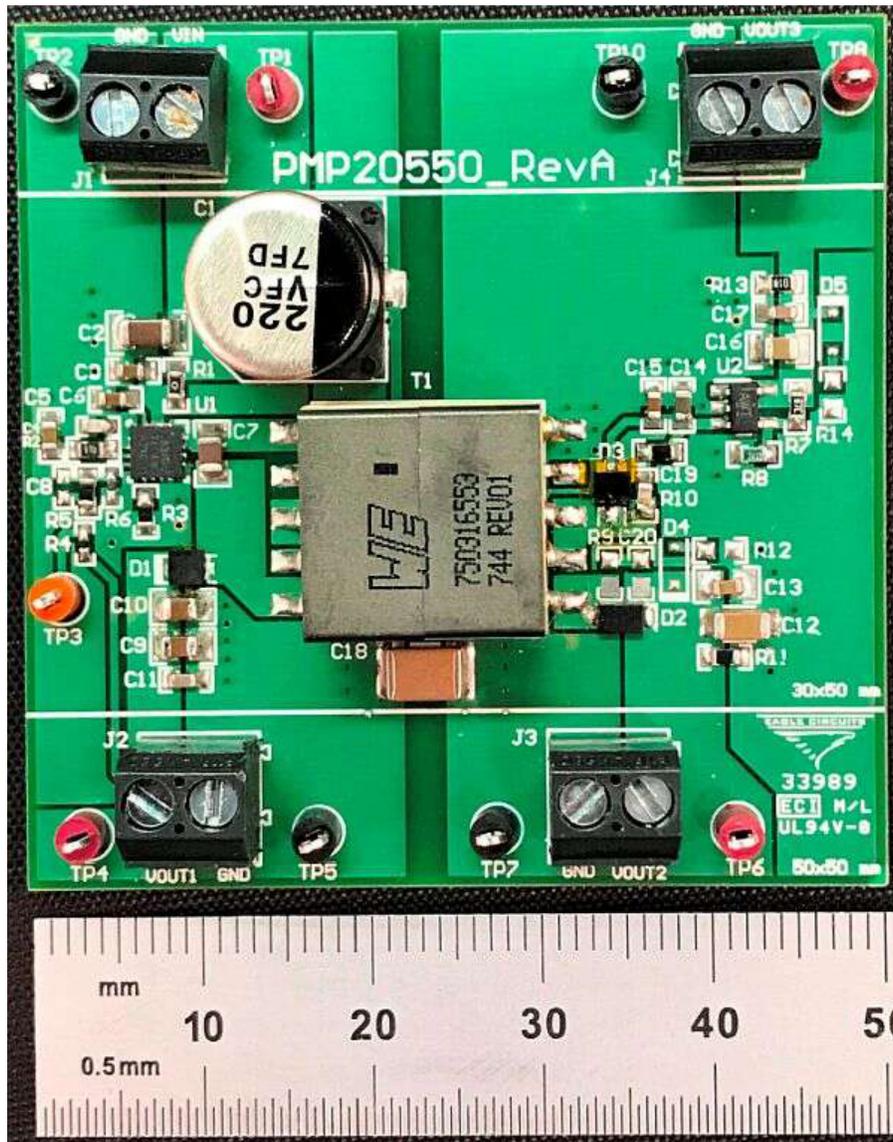


Figure 5. Prototype circuit hardware.

An isolated SEPIC converter may not be your first choice for adding an isolated output voltage, but it offers higher immunity to leakage inductance associated ringing than a flyback, which can improve output voltage regulation. This may eliminate the need for additional post regulation, resulting in cost savings.

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