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For over a decade, power-supply industries have widely applied the inductor-inductor-capacitor (LLC) series resonant converter (LLC-SRC) shown in Figure 1 with two resonant inductors (two “Ls”: L_m and L_r) and one resonant capacitor (one “C”: C_r) as a low-cost, high-efficiency isolated power stage. An LLC-SRC has a soft-switching nature without a complicated control scheme. Its soft-switching feature enables the use of components with lower voltage ratings and also provides high converter efficiency. Its simple control scheme – variable frequency modulation with a fixed 50% duty cycle – requires a lower controller cost when compared to controllers used for other soft-switching topologies, like phase-shift full-bridge converters.

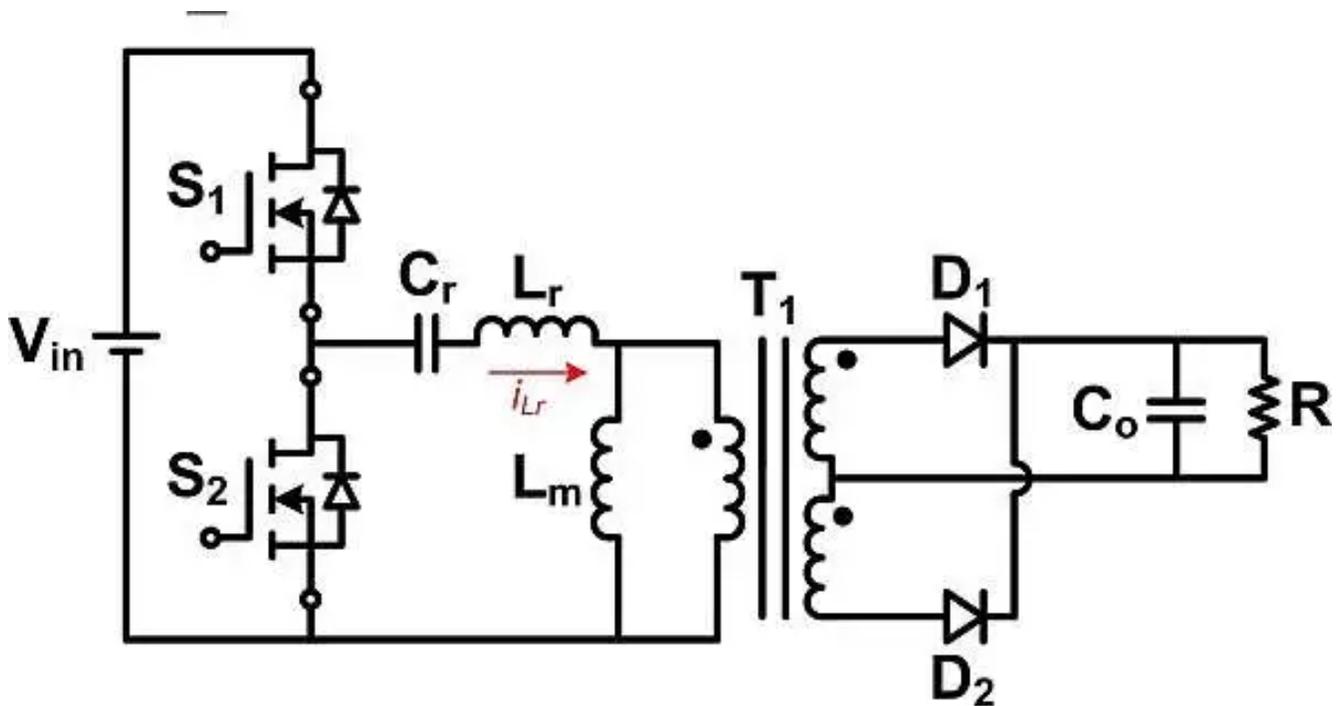


Figure 1. An LLC-SRC

Although an LLC-SRC can achieve much higher efficiency than hard-switching flyback and forward converters, there are still a couple of design challenges if you want to achieve the best efficiency. First, the ratio of two resonant inductors – L_m -to- L_r – will probably have to be smaller than 10 in an LLC-SRC design in order to allow a wide-enough controllable range. At the same time, you’ll need a large inductance on L_m to lower the circulating current – which implies that you’ll need to keep the L_r inductance large to keep the resonant inductor ratio low.

It’s interesting to note that the current in a series resonant inductor L_r is fully AC without any DC content – which means high magnetic flux density variations (ΔB is high). High ΔB means high AC-related inductor losses. If the inductor is wound on a ferrite-based core, you’ll have a high winding loss from the fringing effect near the air gap of the core.

A large inductance on L_r means more turns on the inductor and higher AC winding losses. That is why many LLC-SRC designs apply a powder-iron-based core to the resonant inductor as a trade-off between winding loss and core loss. Nevertheless, high ΔB generates considerable losses on the resonant inductor – either a high winding loss or a high core loss.

A second challenge in an LLC-SRC design is how to best optimize synchronous rectifier (SR) control. LLC-SRC rectifier current-conduction timing depends on the load condition and the switching frequency. The most promising method for LLC-SRC SR control is to sense the SR field-effect transistor (FET) drain-to-source voltage (V_{DS}) and turn the SR on and off when V_{DS} is below or above certain levels. The V_{DS} sensing method requires millivolt levels of accuracy, and therefore can only be realized in an integrated circuit. Self-driven or other low-cost SR control schemes are not applicable to LLC-SRCs because of their current-fed capacitor-loaded output configuration. Thus, the cost of an LLC-SRC SR controller circuit is generally higher than it is for other topologies.

To address these two challenges – high inductor losses and SR control – and yet still harness most of the benefits that a resonant converter can provide, consider using a modified CLL multiresonant converter (CLL-MRC), shown in [Figure 2](#).

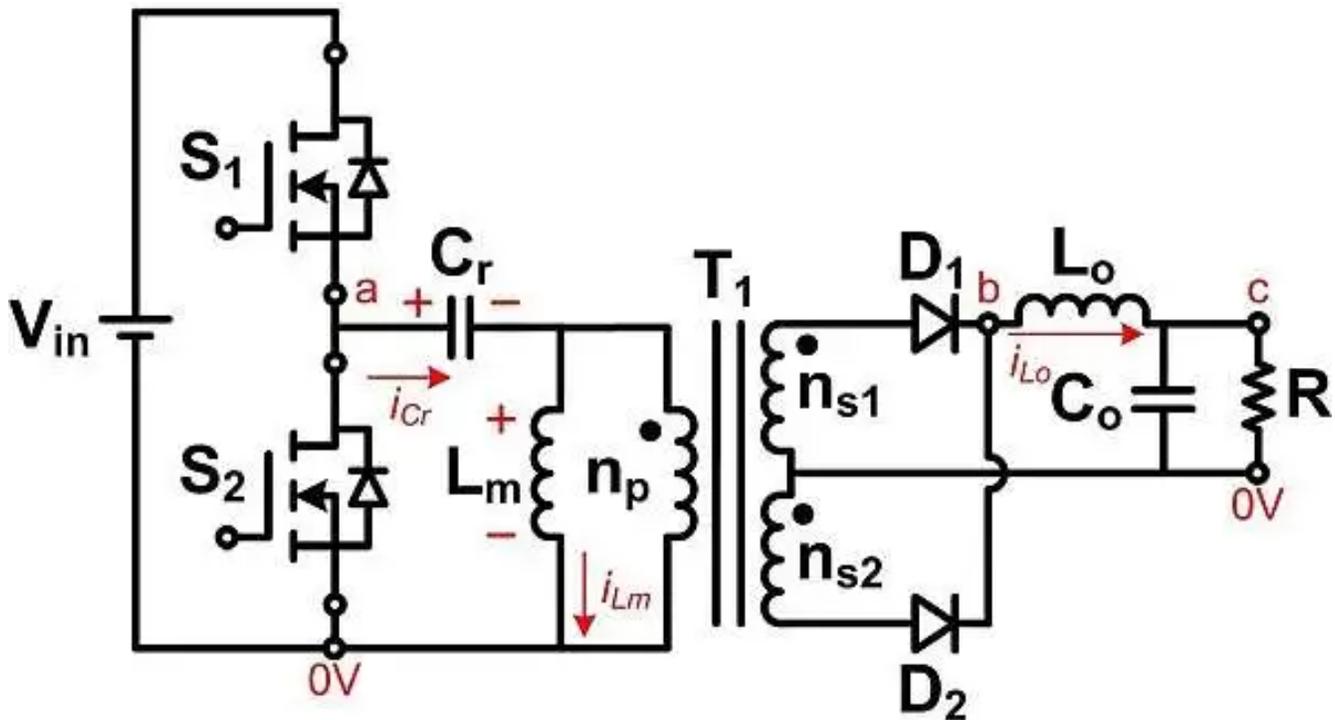


Figure 2. A modified CLL-MRC

Unlike a CLL-MRC, where all three resonant elements (one capacitor and two inductors) are on the input side, a modified CLL-MRC moves one inductor from the input side to the output side and has the inductor placed after the rectifier – L_o , as shown in [Figure 2](#). This modification allows DC current content on the resonant inductor, which implies less ΔB and possibly lower magnetic losses.

[Figure 3](#) illustrates the operation of the modified CLL-MRC, where f_{sw} is the converter switching frequency and $f_{r1} = \{2\pi[C_r(L_{r1} // L_{r2})]\}^{-0.5}$ is one of the two resonant frequencies. When f_{sw} is lower than f_{r1} , the output winding current drops to zero before the end of a switching period, just like the output winding current in an LLC-SRC. Now you have an inductor at the output. A simple capacitor and resistor set can sense the output inductor voltage. Every time a large rate of voltage change (dV/dt) occurs, it is the timing to turn the SRs on or off. Hence, the SR control scheme costs less than the V_{DS} sensing scheme.

When f_{sw} is higher than f_{r1} , the output inductor current operates in continuous conduction mode. In other words, ΔB becomes less, the inductor AC losses can be much smaller, and the converter efficiency is possibly higher than in an LLC-SRC.

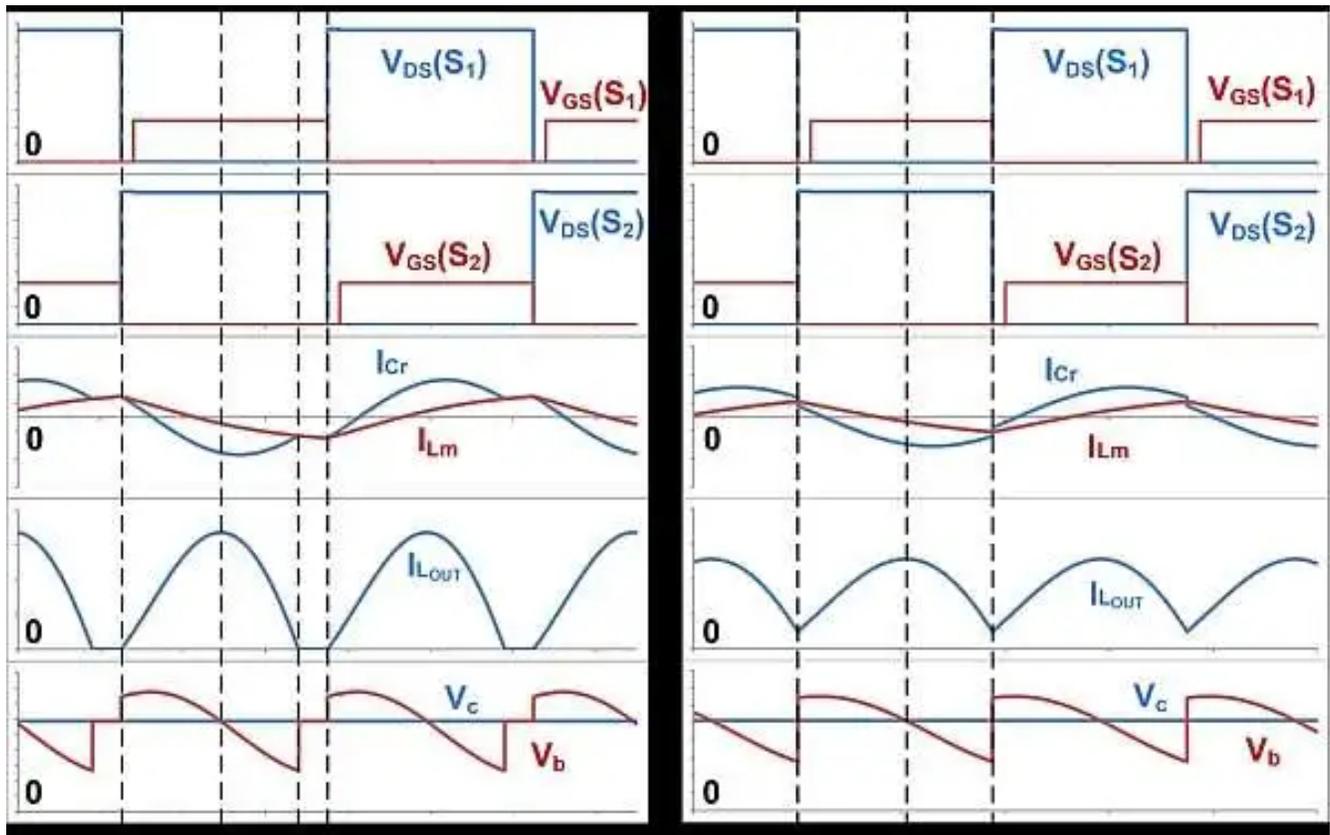


Figure 3. Modified CLL-MRC key waveforms: $f_{sw} < f_{r1}$ (left); $f_{sw} > f_{r1}$ (right)

To verify these performance assumptions, I have built an LLC-SRC and a modified CLL-MRC power stage with the exact same components and parameters. The only difference is the application of a $72\mu\text{H}$ inductor as the LLC-SRC resonant inductor and a $1\mu\text{H}$ inductor as the modified CLL-MRC output inductor.

Figure 4 shows the efficiency measurements of both power stages. With a lower input voltage, f_{sw} is less than f_{r1} – thus the L_o current in the modified CLL-MRC is still in discontinuous conduction mode with large ΔB . Therefore, there isn't an efficiency benefit on the modified CLL-MRC in this operational condition.

When the input voltage goes higher, f_{sw} is higher than f_{r1} and the L_o current is in continuous conduction mode. With a 430-V input, the modified CLL-MRC's efficiency is 1% higher than the LLC-SRC. This comparison shows that if you design the modified CLL-MRC to always operate in a frequency higher than f_{r1} , its efficiency performance can be better than an LLC-SRC over the entire range.

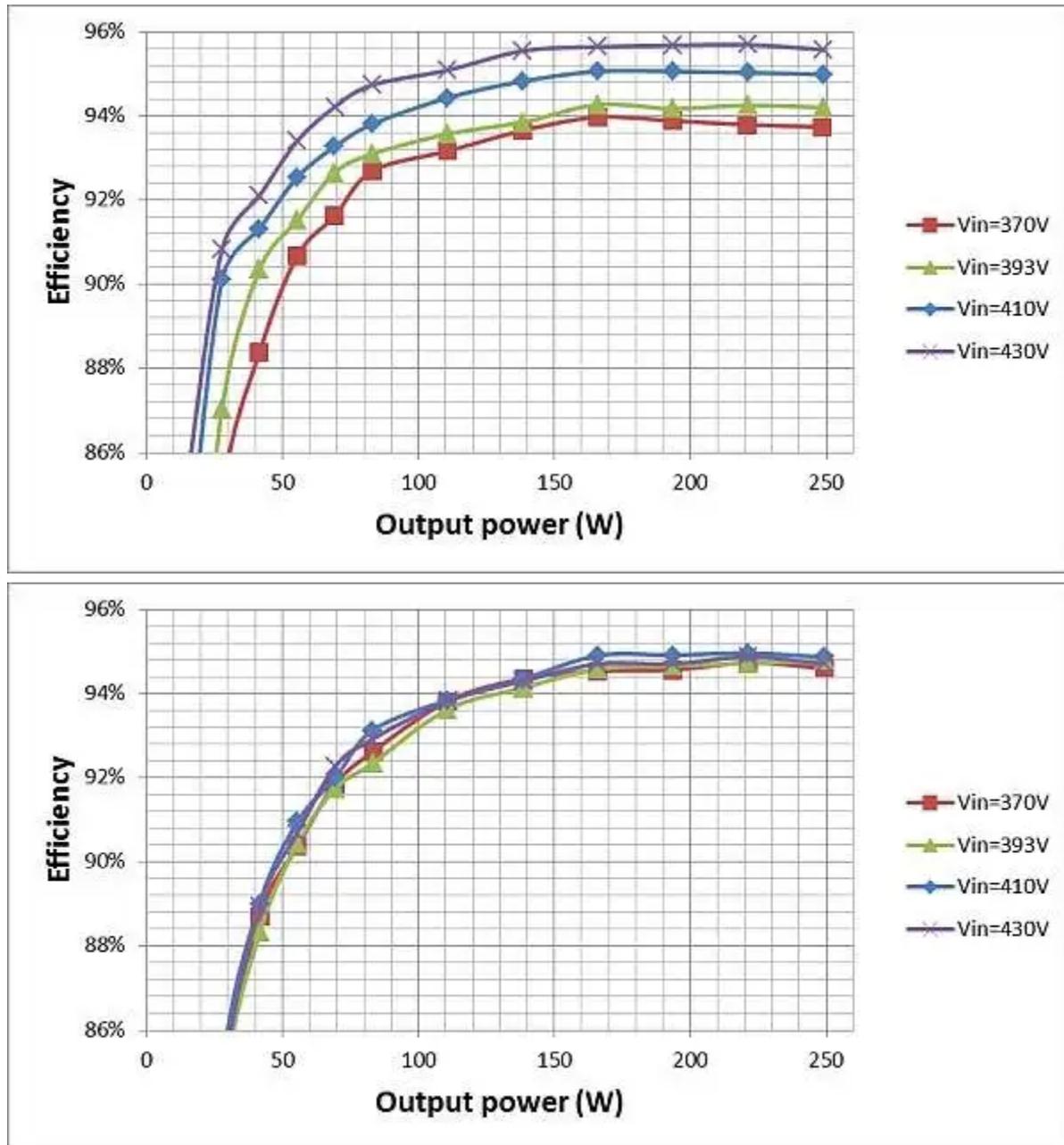


Figure 4. Converter efficiencies with different input voltage levels: modified (top) CLL-MRC; LLC-SRC (bottom)

An LLC-SRC is indeed a good topology and provides many attractive features. But depending on the application, it might not be the best solution. From time to time, you need to think outside the box to achieve better efficiency with a lower circuit cost.

Additional resources

- Read these papers from Texas Instruments Power Supply Design Seminar:
 - [“Designing an LLC Resonant Half-Bridge Power Converter.”](#)
 - [“Survey of Resonant Converter Topologies.”](#)
 - [“Control and Design Challenges of Synchronous Rectifiers.”](#)
- Check out the [400VDC Input to 28V/9A Output Compact, High Efficiency CLL Resonant Converter Reference Design](#).

Related articles

- [LLC resonant topology lowers switching losses, boosts efficiency](#)
- [High efficiency resonant mode implementation using digital control](#)
- [Design considerations when selecting half bridge resonant LLC converters and primary side MOSFETs](#)
- [Using quasi-resonant and resonant converters](#)
- [Power Tips #77: Designing a CCM flyback converter](#)

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