Power management integrated buck controllers for distant point-of-load applications

Sujan Manohar
Design Engineer

Bhaskar Ramachandran
Design Engineer

Puneet Sehgal
Marketing Manager

Kae Wong
Design Engineer

Integrated power group,
High volume analog and logic,
Texas Instruments

Power management integrated circuits (PMICs) are capable of powering multiple processors and FPGAs with flexibility and programmability in individual supply voltages for efficient power management in aggressive dynamic voltage scaling (DVS) environments.

The power-management integrated circuit (PMIC) is a cost-effective power-supply solution for applications that requires multiple power-supply rails. PMICs are commonly used to for system level power including processor, FPGA and peripheral power. Typical applications include personal electronics devices, industrial devices, automotive devices and much more. PMICs typically consist of multiple supply rails powered by buck/boost converters, buck controllers, low-dropout regulators and others. Because PMICs combine multiple supply rails into a single IC, external components required by individual regulators such as capacitors, inductors and power MOSFETs need to be well-managed in a printed circuit board (PCB) design and layout. Along with the PMIC, you need to identify potential solutions close to specific bias power requirements. References to sample designs and resources are provided in this paper to get designers up and running with isolated power solutions for their systems.

There is a common misperception regarding placement in that all external components need to be placed close to the PMIC. This leads to a belief that design with PMICs are restrictive and inflexible, especially for very-high-power integrated power controllers used for distant point-of-load (POL) applications. However, in reality, this is not necessarily true. This paper discusses PCB design and layout strategies for integrated buck controllers to better manage external-component placement and enable a more cost-effective solution for distant POL conditions.

Buck controller

Figure 1 shows a typical buck controller block diagram. External components typically consist of single or multiple input capacitors (C_{IN}), single or multiple output capacitors (C_{OUT}), and an output inductor (L_{OUT}). Additionally, it requires two external power MOSFETs (M_{HSD} and M_{LSD}) and a bootstrap capacitor (C_{BOOT}) for the high-side drive. Since buck controllers are typically designed for high-power applications, it is best to keep the power train (M_{HSD}, M_{LSD} C_{IN}, L_{OUT}, and C_{OUT}) very close to the POL to achieve optimal efficiency. However, the controller IC need not be placed very close to the power train to achieve good performance.

Based on the application, certain layout strategies can achieve less-restrictive placement of the IC. The following section discusses the function and placement of the external components and IC along with PCB layout strategies.

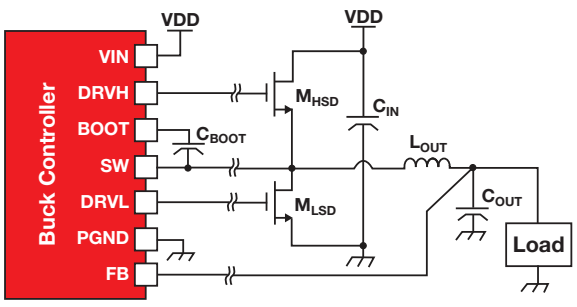

Figure 1. Typical buck controller block diagram and external components.

Power MOSFETs, input capacitor, output inductor and output capacitor considerations

Power MOSFETs, input capacitors, output inductors, and output capacitors form the power train of a buck controller. The input capacitor acts as a local power supply, the output inductor and capacitor function as a low-frequency filter, and power MOSFETs perform switching power conversion. All of these components need to be placed close together on the PCB to achieve reliable and efficient performance. As mentioned earlier, buck controllers are typically used for high-power applications. Therefore, it's best to keep the power train close to the POL to minimize power loss. However, the controller IC can be placed relatively further away from these components, as long as proper layout guidelines are followed to route the high-side driver (DRVH), low-side driver (DRVL) and switching (SW) signals.

Layout routing strategies

The route length of DRVH and DRVL signals determines how far away the PMIC can be placed from the POL. As long as the integrity of these two signals are maintained, the controller will not experience any performance degradations. In particular, if the DRVH and DRVL signals are distorted enough to turn on the high-side-drive (HSD) FET and low-side-drive (LSD) FET at the same time, there will be reliability or power loss issues due to cross-conduction. Since DRVH and DRVL are high-speed gate drive signals with fast slew rates, their routings have to be treated as transmission lines in the PCB layout to maintain good signal integrity.

DRVH and DRVL signal routings can be modeled as shown in **Figure 2**. Note that the return path for the DRVH signal is the SW signal; for the DRVL signal the return path is the power ground (PGND).

In the case of long transmission-line routings, the most straightforward and cost-effective strategy is to adopt a microstrip-line layout technique, or strip-line layout technique, to control the line impedance.

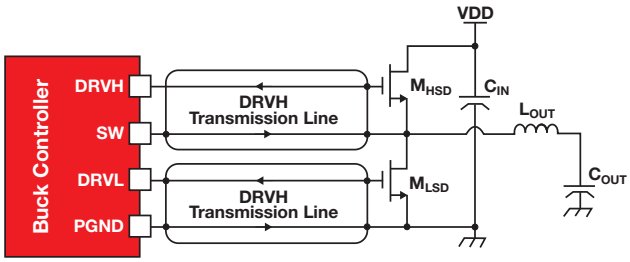

Figure 2. High-side drive (DRVH) and low-side drive (DRVL) as transmission lines.

Figure 3 illustrates PCB cross-sections for microstrip-line and strip-line routings. The microstrip-line method is good for routing signals at the top PCB layer, while the strip-line method is good for routing signals in the inner layer of the PCB. **Table 1** shows typical PCB parasitics for a microstrip line.

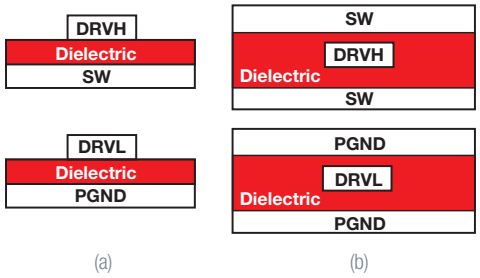

Figure 3. High-side drive (DRVH) and low-side drive (DRVL) PCB routing cross-section (a) microstrip line (b) strip line.

In order to demonstrate the effectiveness of the layout strategies discussed here, the TPS650860, a PMIC with three controllers and three converters is used to simulate a typical use case scenario. Simulation with estimated PCB parasitics from **Table 1** and the power FET model for the CSD87381P confirm that the PMIC controller can be easily placed 11 inches away from the POL.

Figure 4 depicts transmission-line models for DRVH and DRVL, where the SW plane is modeled to be four times wider than the DRVH line, and the PGND is modeled as a low-impedance ground plane. Simulation results shown in **Figure 5** compare the gate-source voltages of the power FETs in two scenarios. In the first case, power-train components are placed very close to the PMIC (<1 inch). In the second case, power-train components are placed close to the POL and 11 inches away from the PMIC. In this scenario, 11-inch microstrip lines are used to route gate-drive signals.

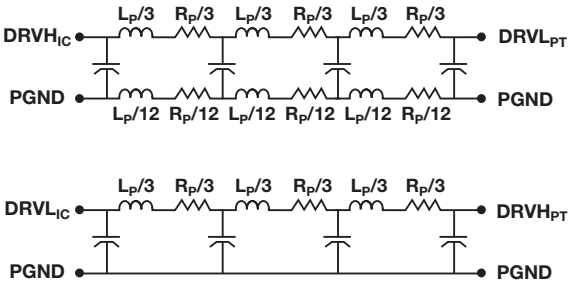

Figure 4. Transmission-line model used in the simulation.

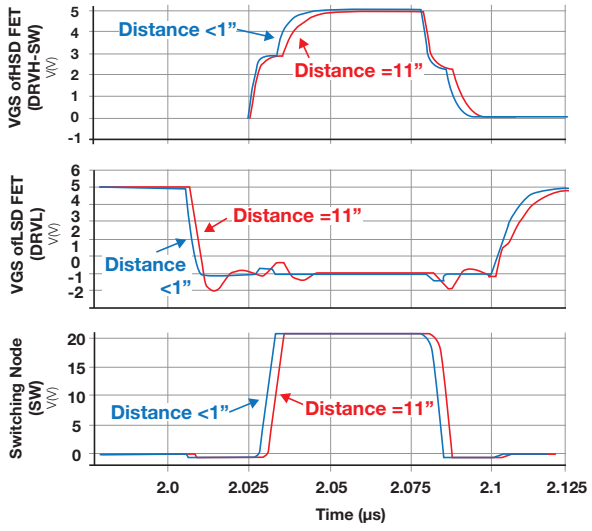

Figure 5. Simulation results of the controller placed less than one inch from the power train and POL, versus 11 inches.

Based on the simulation results, scenario two (**Figure 3b**) has a few more nanoseconds delay versus scenario one (**Figure 3a**), which has very short routing for gate-drive signals. This extra delay time is caused by the delay experienced by the gate-drive signals through the transmission line. Further, the rise and fall times for the HSD gate signal (DRVH-SW) of the second scenario are slightly higher, but not significantly different from scenario one. The DRVL signal has minor overshoots and undershoots; these are as expected when a signal travels through a long transmission line. These overshoot levels are not severe enough to turn on the LSD MOSFET to pose any significant performance issues.

Length (inches)	Width (mils)	Copper thickness	Inductance LP (nH)	Capacitance CP (pF)	Resistance RP (mΩ)
4	20	1/2 oz	1.5	200	200
7	20	1/2 oz	2.6	300	290
11	20	1/2 oz	4.0	560	550

Table 1. Typical microstrip line parasitic with return path modeled as a plane.

Bootstrap capacitor consideration

The function of the bootstrap capacitor is to act as a floating local power supply for the DRVH driver; therefore, the preferred placement is close to the controller IC. The routing resistance of the bootstrap capacitor will affect the charging time of the DRVH signal, so the routing resistance has to be maintained at around 100 mΩ. **Figure 6** illustrates the parasitic routing resistance, where RPARA is a model of parasitic resistance and DRVH is the current drawn to turn on the HSD MOSFET.

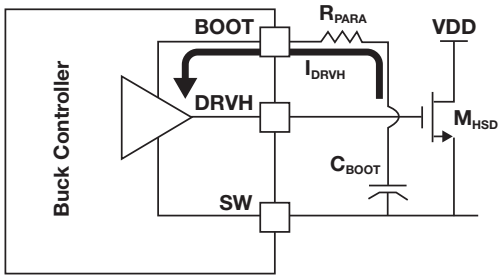

Figure 6. DRVH buffer with bootstrap capacitor with PCB routing parasitic.

Summary

Not all external components for an integrated buck controller need to be placed close to the PMIC. The power-train components can be placed close to the POL, as long as the layout guidelines presented in this paper are implemented. Texas Instruments PMICs with integrated buck controllers include the TPS65911 and TPS650680.

To use controllers as an effective solution for distant POL applications, key PCB layout concerns include:

- Placing the input capacitor and power FETs close to each other to achieve maximum reliable performance.
- Placing the inductor and output capacitor close to the FETs and input capacitor to achieve maximum power efficiency.
- Placing power-train components, including power FETs, inductors and input/ output capacitors at the POL.
- Treating DRVH and DRVL routings as transmission lines. Microstrip-line and strip-line layout techniques achieve the best performance.
- Placing the bootstrap capacitor close to the PMIC to maintain drive capability for DRVH.

References

Learn more about power management multi-channel IC (PMIC) solutions

Product folders: CSD87381P, TPS65911, TPS650860

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265